MWCT2xxxS

MWCT2xxxS

Supports MWCT2014S, MWCT2015S, MWCT2016S, MWCT2D16S and MWCT2D17S

Rev. 4 — 09/2024 Data Sheet: Product Preview

- Operating characteristics
  - Voltage range: 2.97 V to 5.5 V
  - Ambient temperature range: -40 °C to 125 °C for all power modes
- Arm™ Cortex-M7 core, 32-bit CPU
  - M7 supports up to 160 MHz frequency with 2.14 DMIPS / MHz
  - Arm Core based on the Armv7 and Thumb®-2 ISA
  - Integrated Digital Signal Processor (DSP)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single Precision Floating Point Unit (FPU)
- Clock interfaces
  - 8 - 40 MHz Fast External Oscillator (FXOSC)
  - 48 MHz Fast Internal RC oscillator (FIRC)
  - 32 kHz Low Power Oscillator (SIRC)
  - 32 kHz Slow External Oscillator (SXOSC)
  - System Phased Lock Loop (SPLL)
- I/O and package
  - LQFP48, HDQFP100, HDQFP172
- Up to 32-channel DMA with up to 128 request sources using DMAMUX
- Memory and memory interfaces
  - Up to 4 MB program flash memory with ECC
  - Up to 128 K of flexible program or data flash memory
  - Up to 512 KB SRAM with ECC, includes 192 KB of TCM RAM ensuring maximum CPU performance of fast control loops with minimal latency
  - Data and instruction cache for each core to minimize performance impact of memory access latencies
  - QuadSPI support
- Mixed-signal analog
  - Up to three 12-bit Analog-to-Digital Converters (ADC) with up to 24 channel analog inputs per module
  - One Temperature Sensor (TempSense)
  - Up to three Analog Comparators (CMP), with each comparator having an internal 8-bit DAC
- Human-Machine Interface (HMI)
  - Non-Maskable Interrupt (NMI)
  - Up to 60 pins with wakeup capability
  - Up to 32 pins with interrupt support

- Power management
  - — Low-power Arm Cortex-M7 core with excellent energy efficiency, balanced with performance
  - — Power Management Controller (PMC) with simplified mode management (RUN and STANDBY)
  - — Supports peripheral specific clock gating. Only specific peripherals remain working in low power modes.
- Communications interfaces
  - — Up to 16 serial communication interface (LPUART) modules, with LIN, UART and DMA support
  - — Up to six Low Power Serial Peripheral Interface (LPSPI) modules with DMA support
  - — Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support
  - — Up to six FlexCAN modules (with optional CAN-FD support)
  - — FlexIO module for flexible and high performance serial interfaces
  - — Up to two Ethernet module
- Reliability, safety and security
  - — Hardware Security Engine (HSE_B) -
  - — Up to two Internal Software Watchdog Timers (SWT)
  - — Error-Correcting Code (ECC) on all memories
  - — Error Detection Code (EDC) on data path
  - — Cyclic Redundancy Check (CRC) module
  - — 120-bit Unique Identification (ID) number
  - — Extended Cross domain Domain Controller (XRDC), providing protection for master core access rights
  - — Virtualization Wrapper (VIRT_WRAPPER), providing I/O protection
- Debug functionality
  - — Serial Wire JTAG debug Port (SWJ-DP), with 2 pin Serial Wire Debug (SWD) for external debugger
  - — Debug Watchpoint and Trace (DWT), with four configurable comparators as hardware watchpoints
  - — Serial Wire Output (SWO)-synchronous trace data support
  - — Instrumentation Trace Macrocell (ITM) with software and hardware trace, plus time stamping
  - — CoreSight AHB Trace Macrocell (HTM)
  - — Flash Patch and Breakpoints (FPB) with ability to patch code and data from code space to system space
  - — Serial Wire Viewer (SWV): A trace capability providing displays of reads, writes, exceptions, PC Samples and print
  - — Full data trace for up to 16 output wide
  - — Embedded Cross Trigger (ECT) is used for multicore run-control and trace cross triggering, using CoreSight Cross Trigger Interface (CTI)
- Timing and control
  - — Up to three enhanced modular I/O system (eMIOS), offering up to 72 timer channels (IC/OC/PWM)
  - — Up to two System Timer Modules (STM)
  - — Up to two Logic Control Units (LCU)
  - — Full cross triggering support for ADC / timer (BCTU)
  - — One Trigger MUX Control (TRGMUX) module
  - — Up to three Periodic Interrupt Timer (PIT) modules
  - — 32-bit Real Time Counter (RTC) with autonomous periodic interrupt (API) function

Contents

1 Overview

The MWCT2xxxS product series further extends the highly-scalable portfolio of Arm ® Cortex ® - M0+/M4F MWCT1xxS chips in the automotive industry with the Arm Cortex-M7 core at higher frequency, more memory, ASIL-B rating and advanced security module. With a focus on automotive environment robustness, the MWCT2xxxS product series devices are well suited to a wide range of applications in electrical harsh environments, and are optimized for cost-sensitive applications offering new, space saving package options. The MWCT2xxxS series offers a broad range of memory, peripherals and performance options. Devices in this series share common peripherals and pin-out, allowing developers to migrate easily within a chip series or among other chip series to take advantage of more memory or feature integration.

2 Block diagram

The following figures show the MWCT2xxxS product series block diagrams

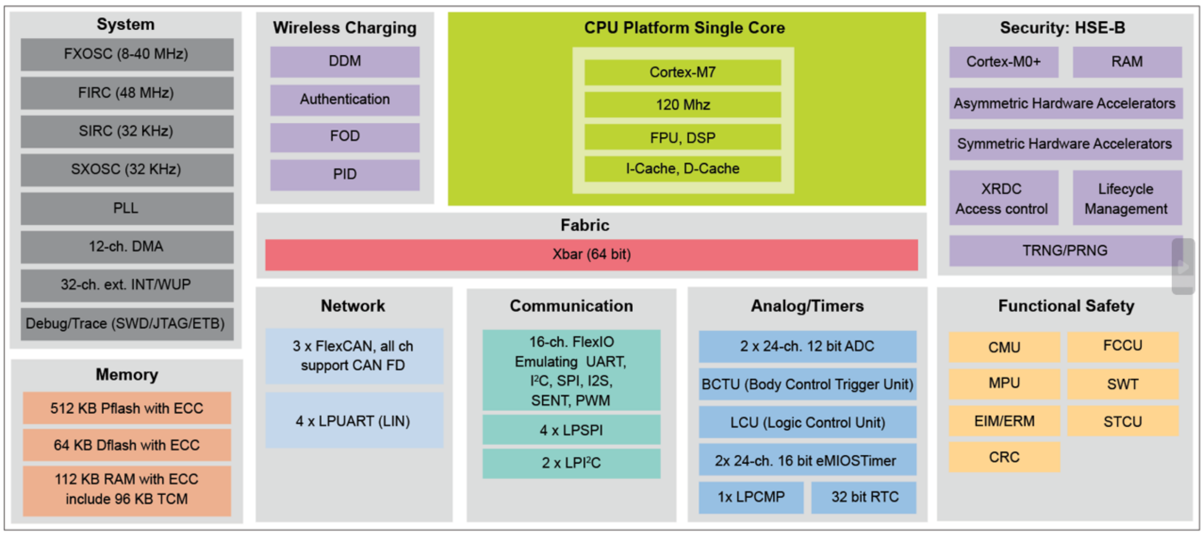


Figure 1. MWCT2014S: ASIL B Single Core 512 KB General Purpose MCU

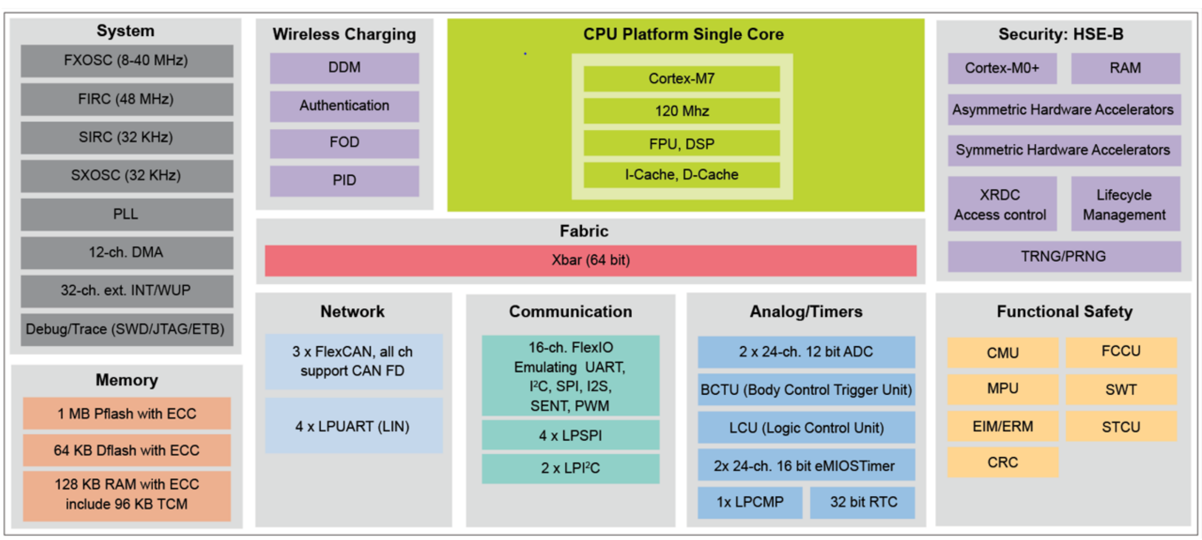


Figure 2. MWCT2015S: ASIL B Single Core 1MB General Purpose MCU

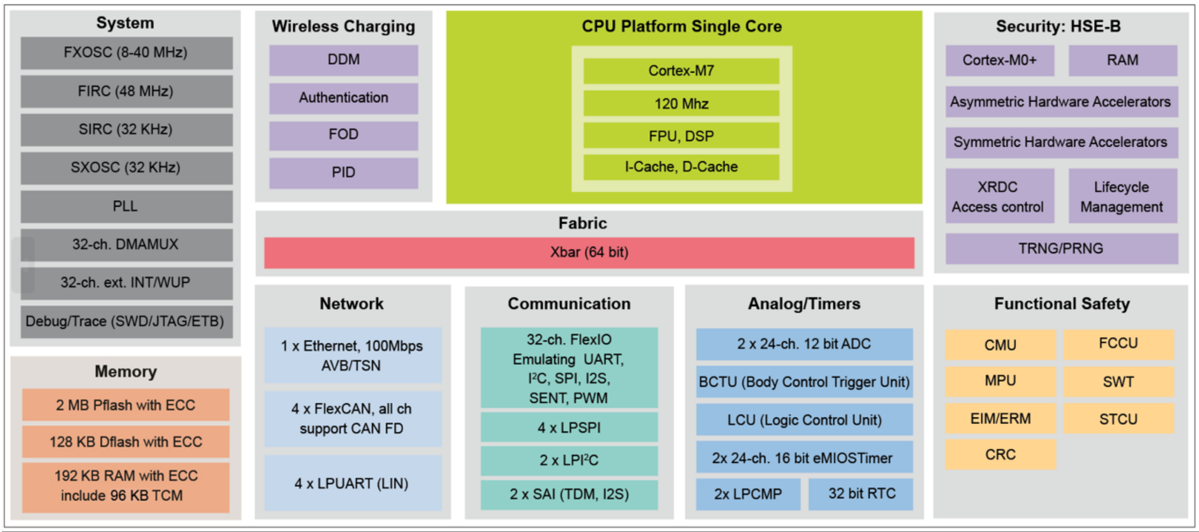


Figure 3. MWCT2016S: ASIL B Single Core 2MB General Purpose MCU

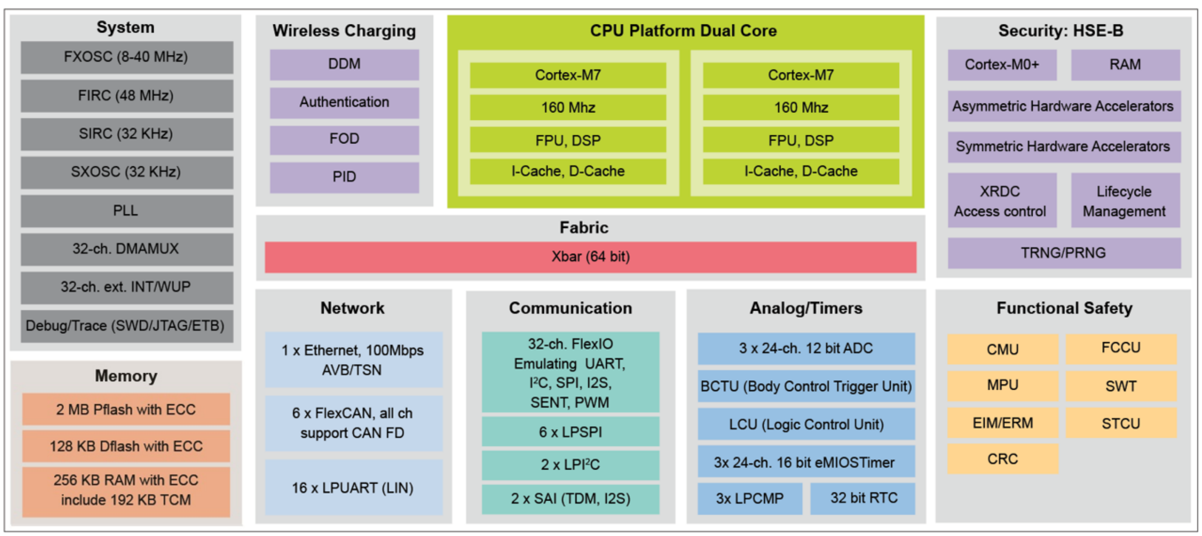


Figure 4. MWCT2D16S: ASIL B Dual Core 2MB General Purpose MCU

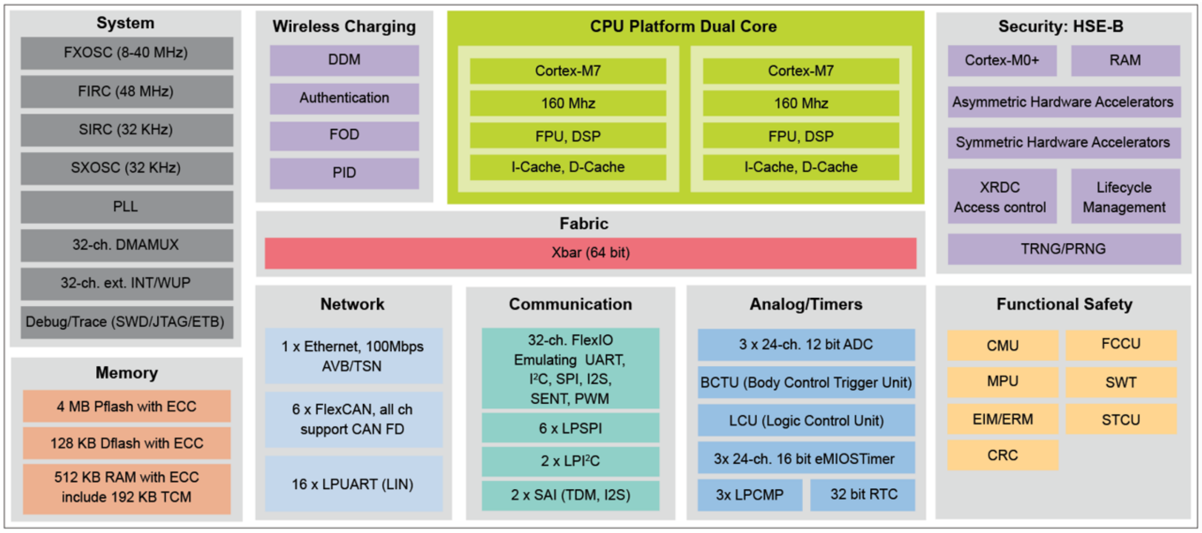


Figure 5. MWCT2D17S: ASIL B Dual Core 4MB General Purpose MCU

3 Feature comparison

The following table compares some of the prominent features related to memory and package options of these chips from the MWCT2xxxS family/product series:

- MWCT2014S
- MWCT2015S
- MWCT2016S
- MWCT2D16S
- MWCT2D17S

Table 1. MWCT2xxxS chip's feature comparison

Feature	Chip				
	MWCT2014S	MWCT2015S	MWCT2016S	MWCT2D16S	MWCT2D17S
Safety/ASIL	B	B			
Program flash memory	512 KB	1 MB	2 MB		4 MB
Data flash memory (KB)	64	64	128		
Total RAM (KB)	112KB (incl. 96KB TCM)	128KB (incl. 96KB TCM)	192KB (incl. 96KB TCM)	256KB (incl. 192KB TCM)	512KB (incl. 192KB TCM)
Standby RAM	32KB				
Security	HSE_B				
Core quantity	1 x M7			2 x M7	2 x M7
Frequency (MHz)	120			160	
DMA channels	12			32	
ASIL–B DMIPS[1]	277–387			739–1033	739–1033
ASIL–D DMIPS[1]	—	—			
ASIL–B CoreMark score[2]	634			1692	1692
ASIL–D CoreMark score[2]	—	—			
FlexCAN instances	3		6	4	6
EMAC instances	—	0		1	
GMAC instances	—	0			
SAI instances	—	0		2	
LPUART instances	4		8	4	16
LPSPI instances	4				6
I^2C instances	2				
FlexIO (incl. SENT support) channels	16		32		
QuadSPI instances	—			1[3]	

Table continues on the next page...

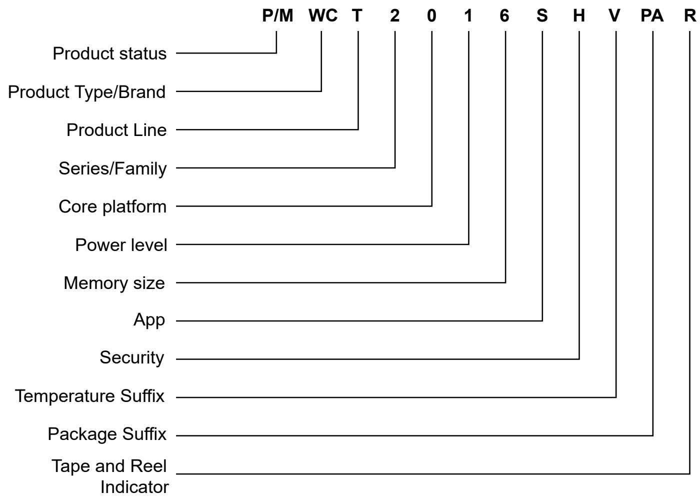
Table 1. MWCT2xxxS chip's feature comparison (continued)

Feature	Chip				
	MWCT2014S	MWCT2015S	MWCT2016S	MWCT2D16S	MWCT2D17S
uSDHC instances	—				
ADC instances	2				3
LPCMP instances	1		2		3
PIT instances	2			3	
SWT instances	1			2	2
STM instances	1			2	
LCU instances	2				
BCTU instances	1				
TRGMUX instances	1				
eMIOS instances	2				3
RTC instances	1				
172-HDQFP package[4]	No		Yes		
100-HDQFP package	Yes				No
48-pin LQFP package	Yes	No	No		

1. Final DMIPS is in range based on compiler setting. Low number is using "ground rules" laid out in the Dhrystone documentation. High number is using inlining of functions.
2. Result depends on specific compiler version, contact NXP sales representative for more details.
3. 4-bit data width
4. 172-HDQFP-EP (exposed pad)

4 Ordering information

Figure 6. Ordering information



Product status

P: Prototype
M: Qualified ordering P/N

Product Type/Brand

WC: Wireless charging MCU

Product Line

T: Transmitter MCU

Series/Family

2: Second gen/ARM CortexM7 based

Core platform

1: 1 x M7 Core
D: 2 x M7 Coress

Power level

1: 15W+

Memory Size

	4	5	6	7
P-FLASH	512KB	1MB	2MB	4MB

App

S: Standard Family SW Package, including:

- Real time driver including combined SDK & Autosar MCAL (ISO26262, crypto driver included)
- Standard Security Firmware
- Wireless charging CDD

Security

HSE B Standard Security	Customized Security
H	G= customized firmware for GM HSE

Temperature Suffix

V: -40 °C to 105 °C
M: -40 °C to 125 °C

Package Suffix

pins	HDQFP	LQFP
48	-	LF
100	PA	-
172	PB	-

Tape and Reel Indicator

R: Tape & Reel

4.1 Determining valid orderable parts

To determine the orderable part numbers for this device, please contact NXP sales representative.

5 General

5.1 Absolute maximum ratings

CAUTION

When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage. Functional operation of the chip under conditions - specified as absolute maximum ratings - is not implied.

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions. Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device. All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation. Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

The VDD_HV_B and V15 voltage supply domains are only present in certain devices and packages (MWCT2D17S and MWCT2S16S).

Table 2. Absolute maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	Main I/O and analog supply voltage [1, 2]	-0.3	—	6.0	V	—	—
VDD_HV_B	Secondary I/O supply voltage [1, 2]	-0.3	—	6.0	V	—	—
VDD_DCDC	Supply voltage for the SMPS gate driver [1, 2]	-0.3	—	6.0	V	—	—
V15	High-current logic supply voltage [1, 2]	-0.3	—	6.0	V		—
V25	Flash memory supply (2.5 V), internally regulated [1]	-0.3	—	2.9	V	—	—
V11	Core logic voltage supply (1.1 V), internally regulated [1]	-0.3	—	1.26	V		—
VREFH	ADC high reference voltage [1, 2]	-0.3	—	6.0	V	—	—
VREFL	ADC low reference voltage [1]	-0.3	—	0.3	V	—	—

Table continues on the next page...

Table 2. Absolute maximum ratings (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VGPIO_trans	Transient overshoot voltage allowed on I/O pin [1, 2, 3]	-	—	6.0	V	—	—
I_INJPAD_DC_ABS	Continuous DC input current (positive/negative) that can be injected into an I/O pin [4]	-3	—	3	mA	—	—
I_INJSUM_DC_ABS	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [4]	—	—	30	mA	—	—
TSTG	Storage ambient temperature [5]	-55	—	150	°C	—	—

1. All voltages are referred to VSS unless otherwise specified.
2. 6.0 V maximum for 10 hours over lifetime; 7.0 V maximum for 60 seconds over lifetime.
3. Absolute max rating must be honored under all conditions, including current injection.
4. When input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B) or VSS, practically no current injection is possible. See application note AN4731 for a description of injection current on NXP automotive microcontrollers.
5. TSTG specifies the storage temperature range. It is not the operating temperature range. Please refer to the Thermal operating characteristics table.

5.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed down to the LVR assert level, however electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics will be degraded when voltage drops below 2.97 V.

The VDD_HV_B and V15 voltage supply domains are only present in certain devices and packages (MWCT2D17S and MWCT2D16S).

Table 3. Voltage and current operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	Main I/O and analog supply voltage [1]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_HV_B	Secondary I/O supply voltage [1]	2.97	3.3 or 5.0	5.5	V	—	—
VDD_DCDC	Supply voltage for the SMPS gate driver [1]	2.97	3.3 or 5.0	5.5	V	—	—

Table continues on the next page...

Table 3. Voltage and current operating requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	High-current logic supply input voltage [1]	1.425	1.5	1.65	V		—
V15_extended	High-current logic supply input voltage, extended range [1, 2, 3]	1.425	3.3 or 5.0	5.5	V	For MWCT2D17S and MWCT2D16S	—
VREFH	ADC high reference voltage [1, 4]	2.97	3.3 or 5.0	5.5	V	—	—
VREFL	ADC low reference voltage [1]	-0.1	0	0.1	V	—	—
VSS_DCDC	Power ground for the SMPS gate driver [1]	-0.1	0	0.1	V	—	—
V25	Flash memory and clock supply (2.5 V), internally regulated [1]	—	2.5	—	V	—	—
V11	Core logic supply (1.1 V), internally regulated [1]	—	1.14	—	V		—
VGPIO	Input voltage range at any I/O or analog pin [1]	-0.3	—	VDD_HV_A/B + 0.3	V	—	—
VODPU	Open-drain pull-up voltage [1, 5]	—	—	VDD_HV_A/B	V	—	—
IINJPAD_DC_OP	Continuous DC input current (positive/ negative) that can be injected into an I/O pin [6]	-3	—	3	mA	VDD_HV_A >= 3.6V	—
IINJPAD_DC_OP	Continuous DC input current (positive/ negative) that can be injected into an I/O pin [6]	-2	—	3	mA	VDD_HV_A >= 2.97V	—
IINJSUM_DC_OP	Sum of absolute value of injected currents on all the I/O pins (continuous DC limit) [6]	-30	—	30	mA	VDD_HV_A >= 3.6V	—
IINJSUM_DC_OP	Sum of absolute value of	-20	—	30	mA	VDD_HV_A >= 2.97V	—

Table continues on the next page...

Table 3. Voltage and current operating requirements (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	injected currents on all the I/O pins (continuous DC limit) [6]						
Vramp_slow	Supply ramp rate (slow) [1, 7]	0.5	—	—	V/min	—	—
Vramp_fast	Supply ramp rate (fast) [1, 7]	—	—	100	V/ms	—	—

1. All voltages are referred to VSS unless otherwise specified.
2. If total power dissipation and maximum junction temperature allows. Please refer to Thermal operating characteristics table for the maximum junction temperature, and Thermal characteristics table for the thermal characteristics, to determine the maximum power dissipation allowed for a given package.
3. You must ensure that the junction temperature in the application must not exceed the maximum specified Tj.
4. VREFH should always be equal to or less than VDD_HV_A +0.1. Any positive differential voltage between VREFH and VDD_HV_A i.e., VDD_HV_A < VREFH <= VDD_HV_A + 0.1V) is for RF-AC only. Appropriate decoupling capacitors should be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.
5. Open-drain outputs must be pulled respectively to their supply rail (VDD_HV_A or VDD_HV_B).
6. When input pad voltage levels are close to VDD_HV_A (respectively to VDD_HV_B) or VSS, practically no current injection is possible.
7. The MCU supply ramp rate parameter must be applicable to the MCU input/external supplies. The ramp rate assumes that the MWCT2xxxS HW design guidelines available on www.nxp.com are followed.

5.3 Thermal operating characteristics

Table 4. Thermal operating characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tamb	Ambient temperature	-40	—	105	°C	V- Grade	—
Tamb	Ambient temperature	-40	—	125	°C	M- Grade	
TJ	Junction temperature	-40	—	150	°C	—	—

5.4 ESD and Latch-up Protection Characteristics

Table 5. ESD and Latch-up Protection Characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Vhbm	Electrostatic discharge voltage, human body model (HBM) [1, 2, 3]	-2000	—	2000	V	—	—
Vcdm	Electrostatic discharge voltage, charged-device	-500	—	500	V	—	—

Table continues on the next page...

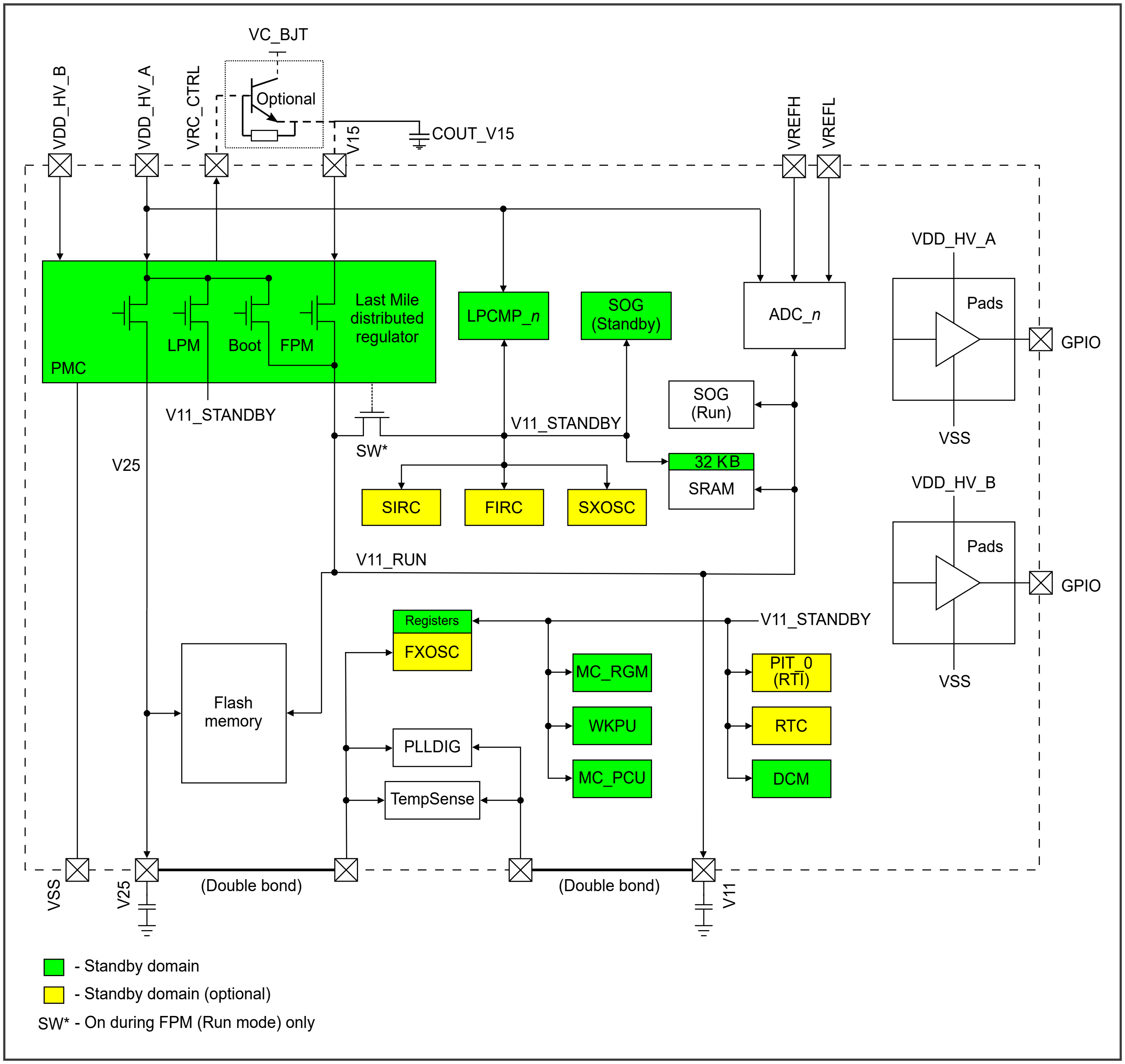
Table 5. ESD and Latch-up Protection Characteristics (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	model (CDM), all pins except corner [1, 3, 4]						
Vcdm	Electrostatic discharge voltage, charged-device model (CDM), corner pins [1, 3, 4]	-750	—	750	V	—	—
Ilat	Latch-up current at ambient temperature of 125°C [5]	-100	—	100	mA	—	—

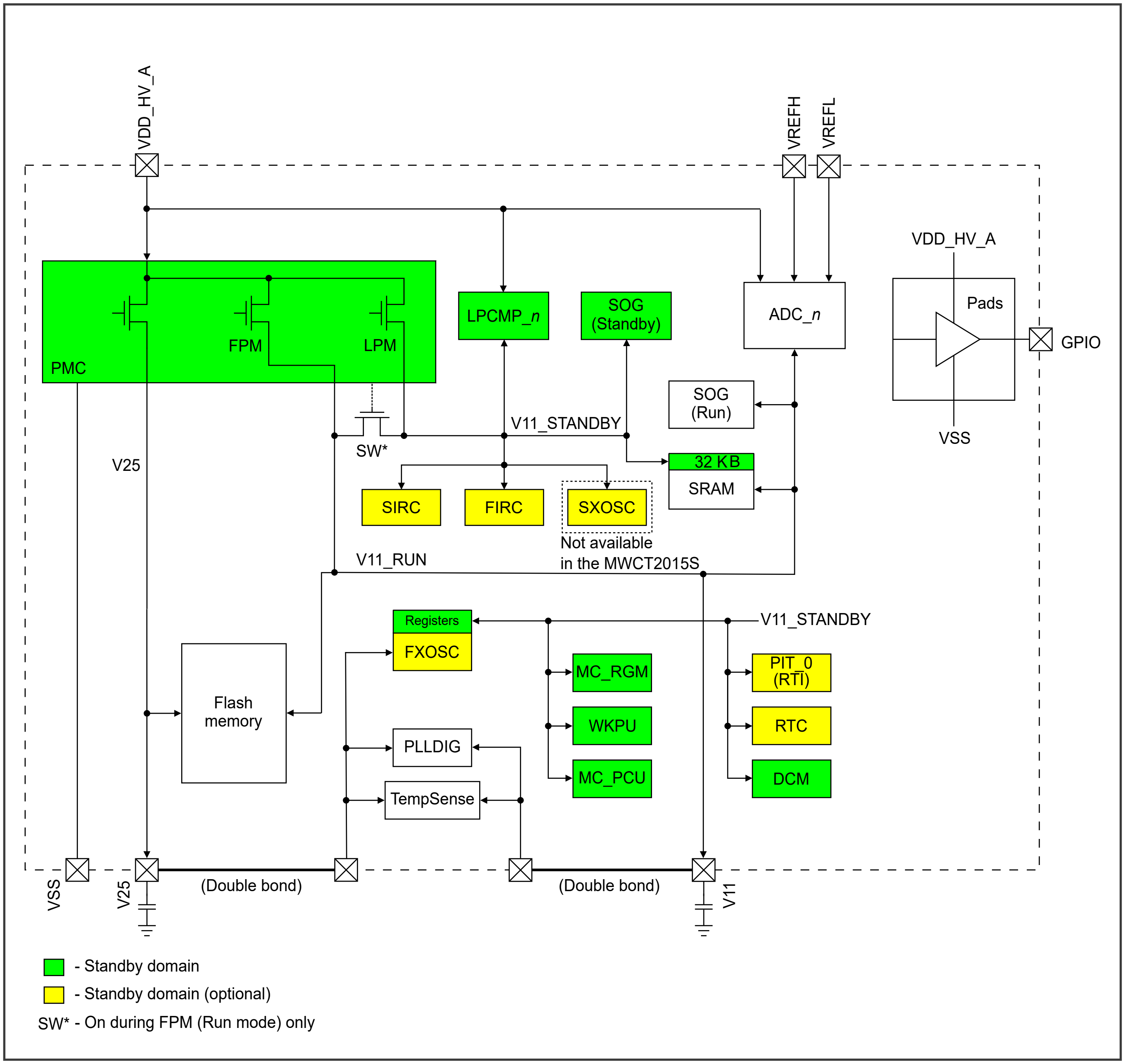
1. Device failure is defined as: "If after exposure to ESD pulses, the device does not meet specification requirements."
2. This parameter is tested in conformity with AEC-Q100-002.
3. All ESD testing conforms with AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
4. This parameter is tested in conformity with AEC-Q100-011.
5. This parameter is tested in conformity with AEC-Q100-004.

6 Power management

6.1 Power management system - MWCT2D17S and MWCT2D16S.



6.2 Power management system - MWCT2016S, MWCT2015S



6.3 Power mode transition operating behaviors

6.3.1 Power mode transition operating behavior

The values in the table below are provided for reference only.

Table 6. Power mode transition operating behavior

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tMODE_ STDBYENTRY	RUN --> STANDBY transition time	—	955	—	ns	—	—
tMODE_ STDBYEXIT_FAST	STANDBY --> RUN transition time, fast standby exit	—	53	—	us	FIRC ON @48MHz in Standby mode	—
tMODE_ STDBYEXIT	STANDBY --> RUN transition time, normal standby exit	—	80	—	us	—	—

6.3.2 Boot time, HSE firmware not installed

Table 7. Boot time, HSE firmware not installed

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBOOT_noHSE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is not installed. (HSE FW feature flag is disabled)	—	2	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—

6.3.3 Boot time, HSE firmware installed

The following table provides the boot time of the MWCT2S SBAF and Firmware initialization. To obtain the total boot time, the corresponding user code verification time must be added.

Table 8. Boot time, HSE firmware installed

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tBOOT_HSE_ NONSECURE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed BOOT SEQ = 0 Default configuration: CORE_CLK @ 48 MHz (source = FIRC	—	—	3	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tBOOT_HSE	After a POR event, amount of time to	—	12.36	—	ms	Device running from FIRC (clocking option	—

Table continues on the next page...

Table 8. Boot time, HSE firmware installed (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	execution of the first instruction of the application core, when HSE firmware is installed. Default configuration: CORE_CLK @ 48 MHz (source = FIRC)					D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	
tBOOT_HSE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed. Optional configuration: CORE_CLK @ 120 MHz (source = PLL)	—	9.51	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tBOOT_HSE	After a POR event, amount of time to execution of the first instruction of the application core, when HSE firmware is installed. Optional configuration: CORE_CLK @ 80 MHz (source = PLL)	—	10.91	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—

6.3.4 HSE firmware memory verification time examples

Table 9. HSE firmware memory verification time examples

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tCMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 CMAC cipher.	—	11.3	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tCMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 CMAC cipher.	—	176	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tGMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 GMAC cipher.	—	3.2	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tGMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 GMAC cipher.	—	46.8	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tHMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 HMAC cipher.	—	1.74	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tHMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 HMAC cipher.	—	22.87	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz.	—
tRSA_64KB	Memory verification of 64 KB of application firmware, using RSA 2048 cipher.	—	TBC	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tRSA_1024KB	Memory verification of 1024 KB of application firmware, using RSA 2048 cipher.	—	TBC	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tECDSA_64KB	Memory verification of 64 KB of application firmware, using ECDSA 521 bits cipher.	—	TBC	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tECDSA_1024KB	Memory verification of 1024 KB of application firmware, using ECDSA 521 bits cipher.	—	TBC	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tSHA2_256_64KB	Memory verification of 64 KB of application firmware,	—	1.62	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	using SHA2 256 bits bits cipher.					MHz; HSE_CLK = 48 MHz	
tSHA2_256_ 1024KB	Memory verification of 1024 KB of application firmware, using SHA2 256 bits bits cipher.	—	22.73	—	ms	Device running from FIRC (clocking option D). CORE_CLK = 48 MHz; HSE_CLK = 48 MHz	—
tCMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 CMAC cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tCMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 CMAC cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz	—
tGMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 GMAC cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz	—
tGMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 GMAC cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz	—
tHMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 HMAC cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz	—
tHMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 HMAC cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tRSA_64KB	Memory verification of 64 KB of application firmware, using RSA 2048 cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tRSA_1024KB	Memory verification of 1024 KB of	—	TBC	—	ms	Device running from PLL (clocking option	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
	application firmware, using RSA 2048 cipher.					A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz	
tECDSA_64KB	Memory verification of 64 KB of application firmware, using ECDSA 521 bits cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tECDSA_1024KB	Memory verification of 1024 KB of application firmware, using ECDSA 521 bits cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tSHA2_256_64KB	Memory verification of 64 KB of application firmware, using SHA2 256 bits bits cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tSHA2_256_ 1024KB	Memory verification of 1024 KB of application firmware, using SHA2 256 bits bits cipher.	—	TBC	—	ms	Device running from PLL (clocking option A). CORE_CLK = 160 MHz; HSE_CLK = 80 MHz.	—
tCMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 CMAC cipher.	—	4.5	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tCMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 CMAC cipher.	—	69.9	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tGMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 GMAC cipher.	—	1.3	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tGMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 GMAC cipher.	—	18.7	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—

Table continues on the next page...

Table 9. HSE firmware memory verification time examples (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tHMAC_64KB	Memory verification of 64 KB of application firmware, using AES-128 HMAC cipher.	—	0.7	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tHMAC_1024KB	Memory verification of 1024 KB of application firmware, using AES-128 HMAC cipher.	—	9.12	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tRSA_64KB	Memory verification of 64 KB of application firmware, using RSA 2048 cipher.	—	15.4	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tRSA_1024KB	Memory verification of 1024 KB of application firmware, using RSA 2048 cipher.	—	23.8	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tECDSA_64KB	Memory verification of 64 KB of application firmware, using ECDSA 521 bits cipher.	—	19.42	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tECDSA_1024KB	Memory verification of 1024 KB of application firmware, using ECDSA 521 bits cipher.	—	TBC	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tSHA2_256_64KB	Memory verification of 64 KB of application firmware, using SHA2 256 bits bits cipher.	—	0.64	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—
tSHA2_256_1024KB	Memory verification of 1024 KB of application firmware, using SHA2 256 bits bits cipher.	—	9.07	—	ms	Device running from PLL (clocking option B). CORE_CLK = 120 MHz; HSE_CLK = 120 MHz.	—

6.4 Supply Monitoring

Certain monitors are present on certain devices. See Power Management chapter in reference manual.

Table 10. Supply Monitoring

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
LVD_V15	Low Voltage Detect (LVD) on V15, deassert threshold (in FPM)	1.34	1.38	1.42	V	—	—
HVD_V15	High Voltage Detect (HVD) on V15, assert threshold (in FPM)[1]	—	2.5	—	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_A	LVR on VDD_HV_A, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—
—	VDD_HV_A LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_A	HVD on VDD_HV_A, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_A HVD monitor hysteresis	—	37.5	—	mV	—	—
LVR_VDD_HV_B	LVR on VDD_HV_B, assert threshold (in FPM)	2.77	2.85	2.93	V	—	—
LVR_VDD_HV_B	LVR on VDD_HV_B, assert threshold (in RPM)	2.77	2.85	2.93	V	—	—
—	VDD_HV_B LVR monitor hysteresis	—	18.75	—	mV	—	—
HVD_VDD_HV_B	HVD on VDD_HV_B, assert threshold (in FPM)	5.787	5.887	5.987	V	—	—
—	VDD_HV_B HVD monitor hysteresis	—	37.5	—	mV	—	—
LVD_VDD_HV_A	Low Voltage Detect (LVD5A) on VDD_HV_A, assert threshold (in FPM)	4.33	4.41	4.49	V	—	—
—	VDD_HV_A LVD monitor hysteresis	—	37.5	—	mV	—	—

Table continues on the next page...

Table 10. Supply Monitoring (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VPOR_VDD_HV_A	Power-On-Reset (VPOR) on VDD_HV_A, deassert threshold	0.9	1.5	2.2	V	—	—
VREF12	Bandgap reference, trimmed	1.18	1.2	1.22	V	—	—

1. The HVD_V15 monitor is provided to indicate if the V15 rail is far above the standard V15 operating range , to ensure failures in the V15 regulator are detected.

6.5 Recommended Decoupling Capacitors

Table 11. Recommended Decoupling Capacitors

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
CDEC	Decoupling capacitor (one per supply pin) [1, 2, 3]	70	100	—	nF	—	—
CBULK	Input supply bulk capacitor [2, 4, 5, 6]	—	4.7	—	µF	—	—
COUT_V15_NPN	V15 (1.5V Regulator) output capacitor [2, 7]	—	2.2	—	µF	—	—
COUT_V11	V11 (1.1V Regulator) output capacitor (all chips, except MWCT2015S, MWCT2016S & MWCT2014S) [2]	—	2.2	—	µF	—	—
COUT_V11	V11 (1.1V Regulator) output capacitor (MWCT2015S, MWCT2016S & MWCT2014S) [2]	—	1	—	µF	—	—
COUT_V25	V25 (2.5V Regulator) output capacitor [2, 3]	140	220	—	nF	—	—

1. Optionally, 1 nF capacitors can be added in parallel to the decoupling capacitors.
2. All capacitors must be low ESR ceramic capacitors (for example, X7R). The minimum recommendation is after considering component aging and tolerance.
3. These capacitors must be placed as close as possible to the corresponding supply and ground pins. For BGA packages, the capacitors must be placed on the other side of the PCB to minimize the trace lengths.
4. For devices where the VDD_HV_B domain is present, if the VDD_HV_B supply is different supply from VDD_HV_A, a dedicated bulk capacitor is needed.

5. It is also possible to use higher capacitance values (for example, 10 µF) in place of the 4.7 µF capacitor.
6. These capacitors must be placed close to the source.
7. For devices where V15 is present, the V15 regulator output capacitor and the filter capacitors are required when using an NPN bipolar ballast transistor for the regulation stage. When V15 is supplied from an external regulator, these capacitance recommendations can be followed in addition to the capacitance requirements of the external voltage regulator.

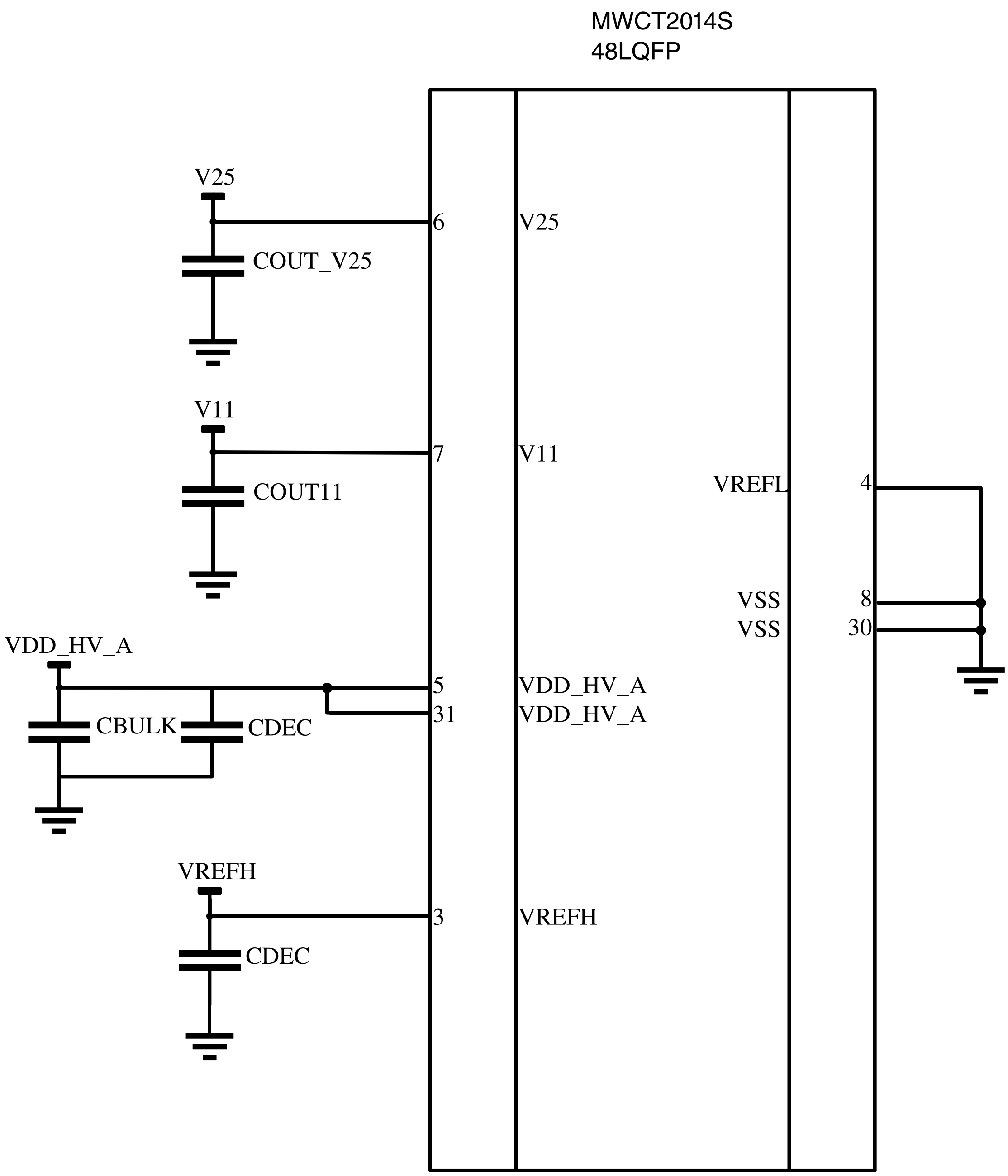


Figure 7. 48-pin LQFP decoupling capacitor pinout diagram (MWCT2014S)

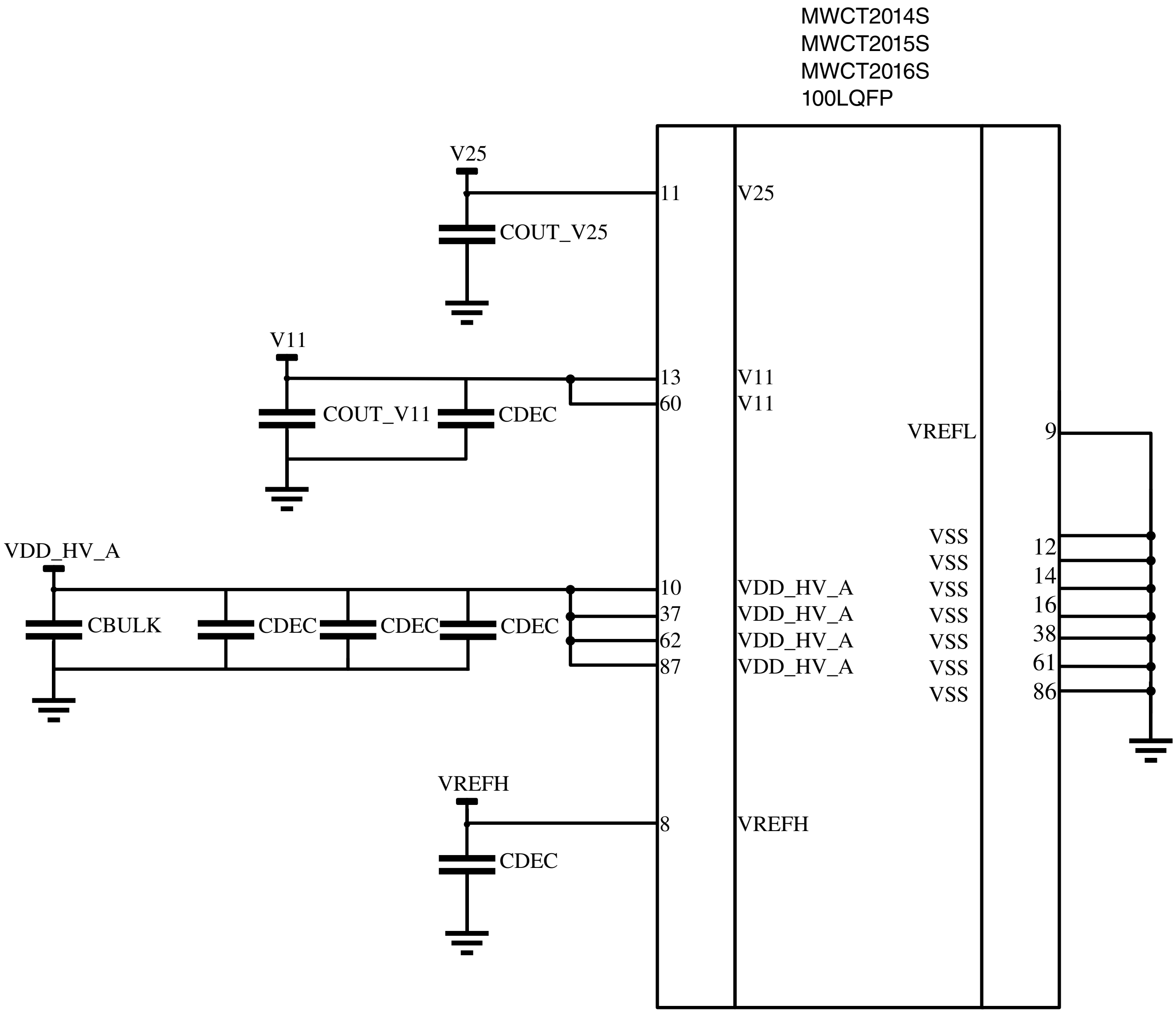


Figure 8. 100-pin HDQFP decoupling capacitor pinout diagram (MWCT2014S, MWCT2015S, MWCT2016S)

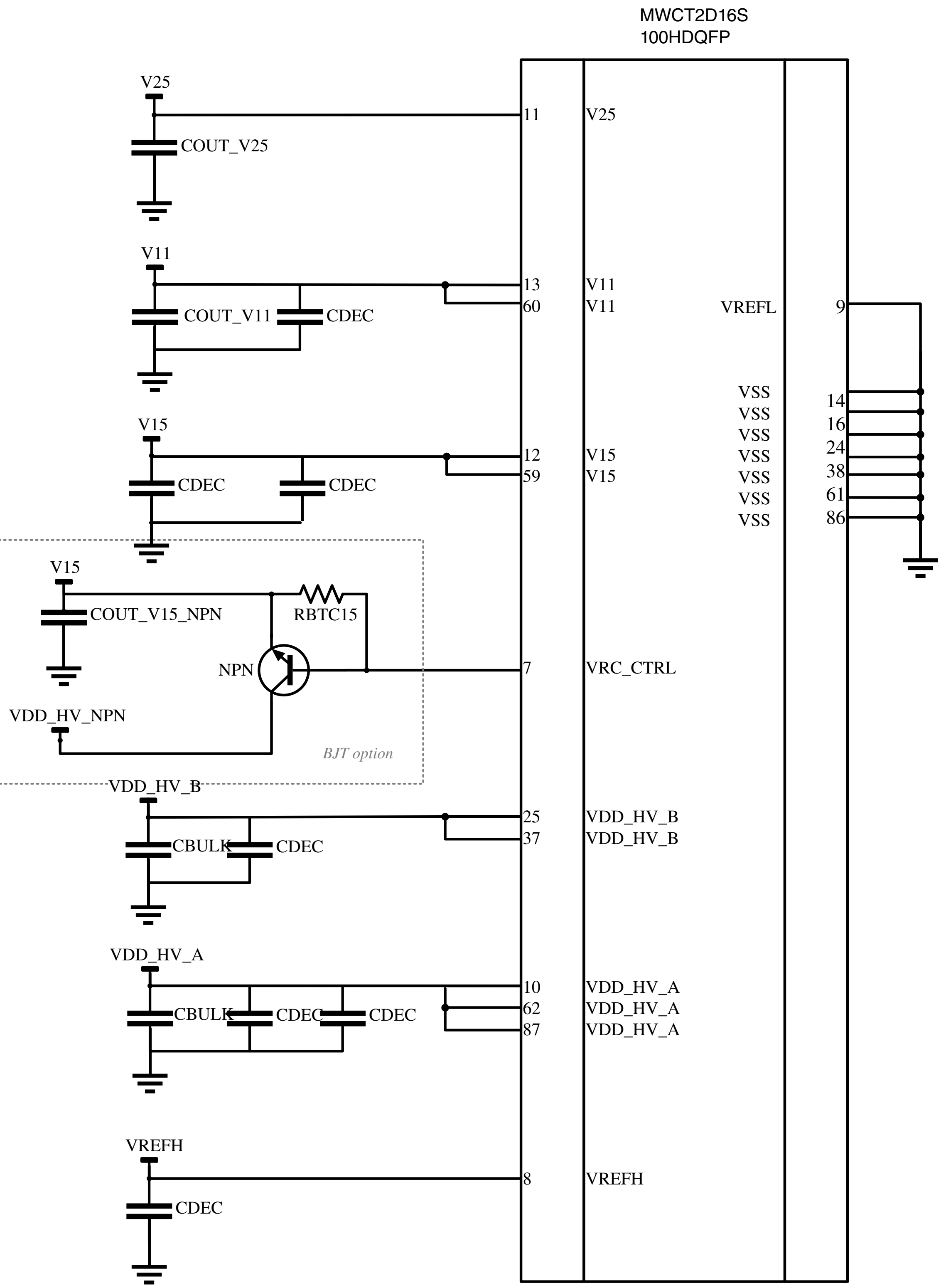


Figure 9. 100-pin HDQFP decoupling capacitor pinout diagram (MWCTD16S)

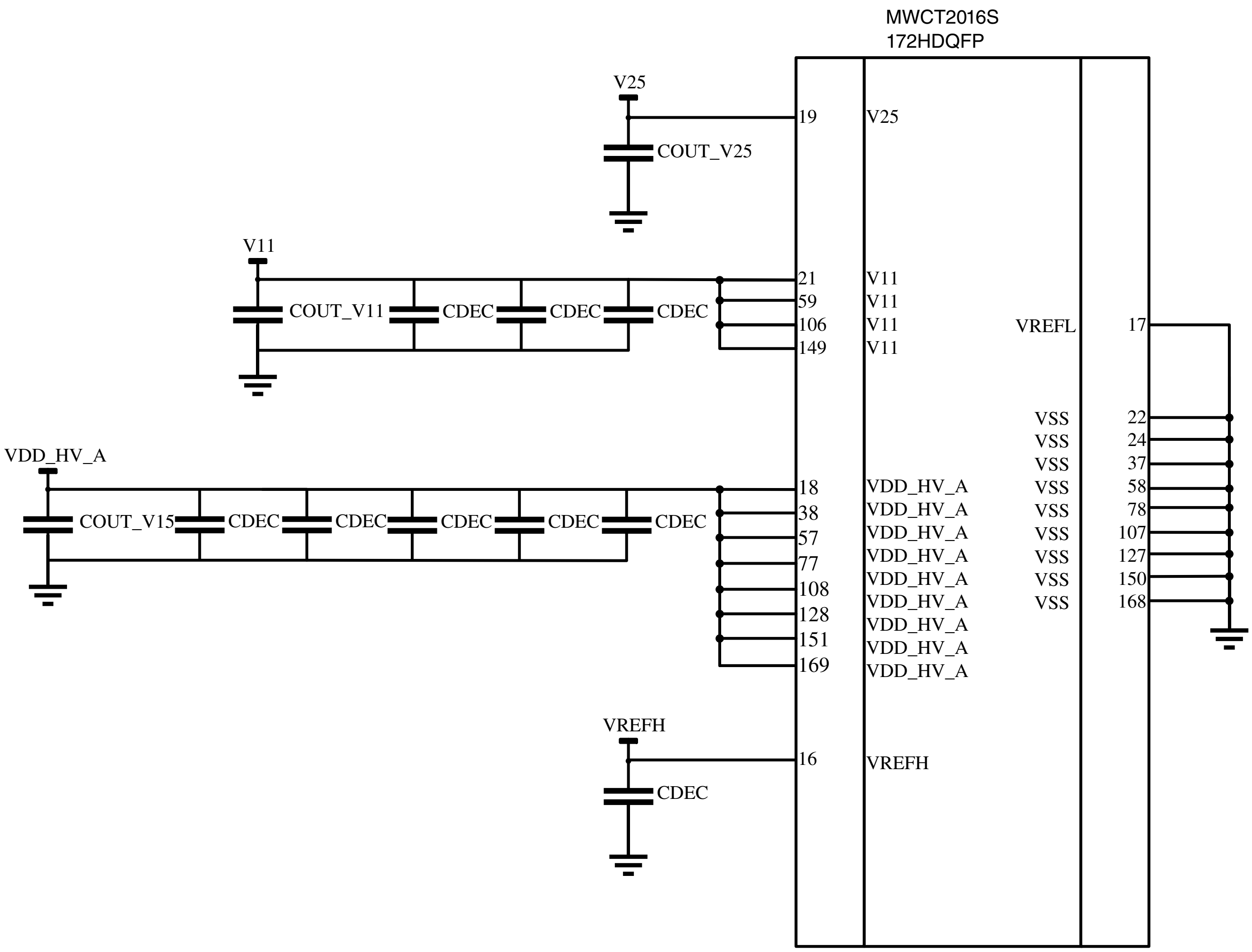


Figure 10. 172-pin HDQFP decoupling capacitor pinout diagram (MWCT2016S)

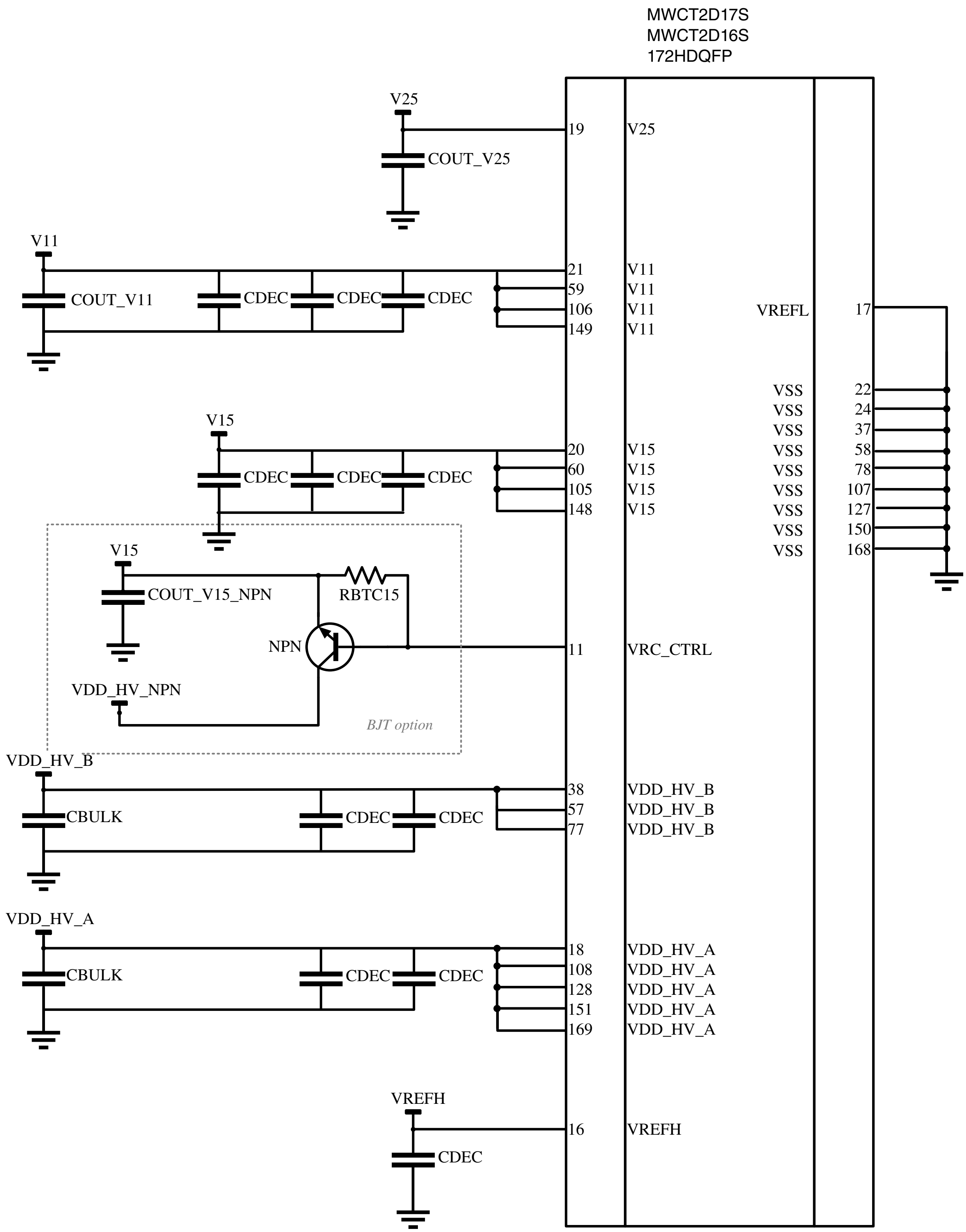


Figure 11. 172-pin HDQFP decoupling capacitor pinout diagram (MWCT2D16S and MWCT2D17S)

6.6 V15 regulator (BJT option, NPN ballast transistor control) electrical specifications

Some devices (MWCT2D17S,MWCT2D16S) support a linear regulator stage, with a dedicated pin to control an external NPN bipolar transistor. The chip hardware design guidelines document lists the recommended part numbers for the external devices.

Table 12. V15 regulator (BJT option, NPN ballast transistor control) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
V15	V15 output	—	1.51	—	V	—	—
V15	V15 input	—	1.5	—	V	—	—
IBCTL	IBCTL (V15 reg) source	10	—	—	mA	—	—
IBCTL	IBCTL (V15 reg) sink	—	—	-50	uA	—	—
tsettle_lm	Required setting time from activating last mile regulator to load change	2	—	—	us	—	—
VDD_HV_NPN	Input voltage supply for NPN external ballast transistor	2.5	3.3 or 5	—	V	—	—

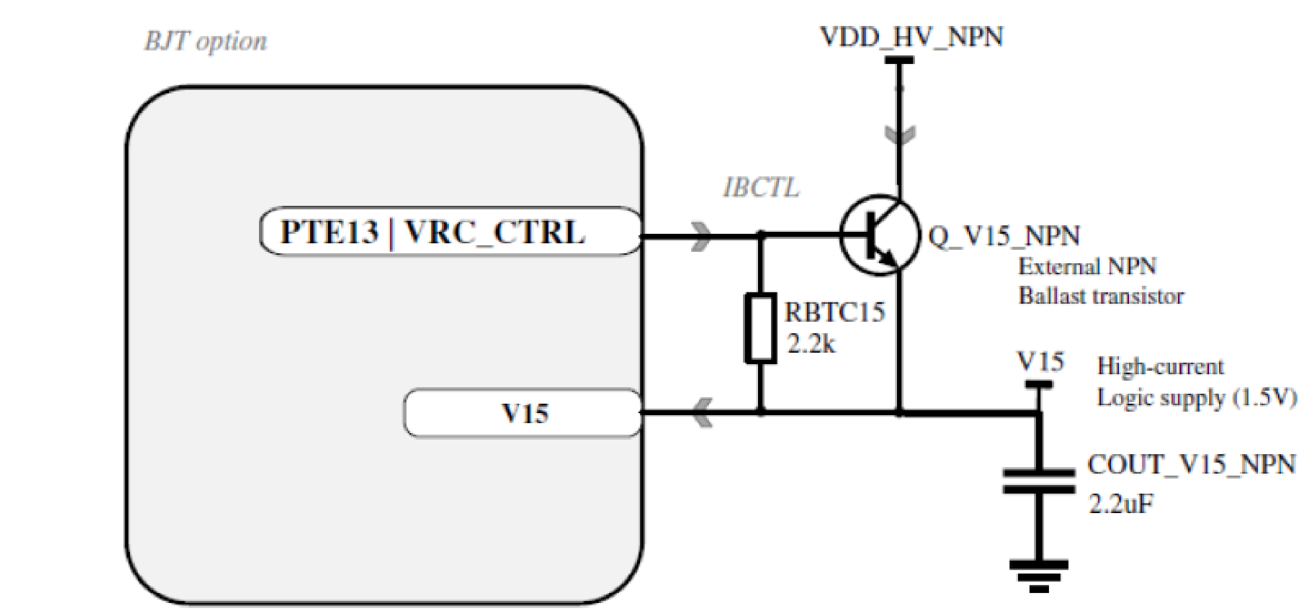


Figure 12. Ballast circuit

6.7 Supply currents

NOTE
All data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C, and typical silicon process unless otherwise stated. In STANDBY configuration, no current flows through the V15 supply.

Table 13. STANDBY mode supply currents

Chip	Ambient Temperature (°C)	STANDBY [1]			
		VDD_HV_A [2]			VDD_HV_B [2]
		All clocks & peripherals OFF (µA)	SIRC ON (µA)	FIRC ON (24 MHz) (mA)	All Config. (µA)
MWCT2D17S	25, typ [3]	50	52	0.91	1.8
	25, max [4]	153	153	1.05	3.8
	85, typ [3]	315	316	1.18	6.1
	85, max[4]	900	910	1.78	15.4
	105, typ [3]	498	530	1.40	8.5
	105, max [4]	1672	1682	2.55	26.2
	125, typ [3]	932	998	1.88	18.5
	125, max [4]	2638	2650	3.5	47.3
MWCT2D16S	25, typ [3]	46.5	49	0.900	1.8
	25, max [4]	88	94	1.040	3.5
	85, typ [3]	220.5	239.4	1.1619	5.4
	85, max [4]	627.0	642.9	1.587	13.9
	105, typ [3]	428.3	456.5	1.3638	7.3
	105, max [4]	1272.6	1301.6	2.2098	22.5
	125, typ [3]	715.2	745	1.6279	16.7

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Table 13. STANDBY mode supply currents (continued)

	125, max [4]	2113.4	2160.6	3.0016	41.6
MWCT2016S	25, typ [3]	40	41	0.887	NA
	25, max [4]	79	80	1.031	
	85, typ [3]	178	178	1.027	
	85, max [4]	496	497	1.422	
	105, typ [3]	350	346	1.197	
	105, max [4]	994	997	1.924	
	125, typ [3]	620	611	1.457	
	125, max [4]	1788	1792	2.761	
MWCT2015S, MWCT2014S	25, typ [3]	38.9	39.8	1.365	NA
	25, max [4]	77.2	79.8	1.823	
	85, typ [3]	144.3	144.9	1.490	
	85, max [4]	491.5	494.8	2.263	
	105, typ [3]	263.8	264.2	1.559	
	105, max [4]	937.4	947.1	2.597	
	125, typ [3]	508.5	510	1.811	
	125, max [4]	1740.1	1760.3	3.488	

1. See the configurations in Table 17.
2. IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
3. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, for the typical silicon process.
4. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, for the fast silicon process.

NOTE

All data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C, and typical silicon process unless otherwise stated.

Table 14. Low speed RUN mode supply currents

Chip	Ambient Temperature (°C)	Low Speed RUN Mode (mA) [1]												
		BOOT Mode [2] [Clock Option C] FIRC @ 24 MHz [Last Mile Disabled]		BOOT Mode [2] [Clock Option C] FIRC @ 24 MHz [Last Mile Enabled]		Low Speed RUN [2] [Clock Option E] FIRC @3 MHz [Last Mile Disabled]		Low Speed RUN [2] [Clock Option E] FIRC @3 MHz [Last Mile Enabled]		Low Speed RUN [2] [Clock Option D] FIRC @48 MHz [Last Mile Disabled]		Low Speed RUN [2] [Clock Option D] FIRC @48 MHz [Last Mile Enabled]		All Config[2] .
		VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_B [3]
MWCT2D17S	25, typ [6]	20.5	-	2.8	17.9	6.4	-	2.8	4.5	37.2	-	2.9	34	0.6
	25, max [7]	29.4	-	3.2	27.2	14.8	-	3.1	12.6	46.8	-	3.2	46.6	0.8
	85, typ [6]	34.2	-	2.9	31.2	19.7	-	2.9	17.5	50.4	-	2.9	47.3	0.5
	85, max [7]	71.6	-	3.5	68.7	56.2	-	3.4	54	89.1	-	3.5	86.2	0.7
	105, typ [6]	46.1	-	2.9	43.1	31.7	-	2.9	29.3	62.2	-	2.9	59.2	0.5
	105, max [7]	114	-	3.7	111	99.1	-	3.6	96.1	131	-	3.9	128	0.7
	125, typ [6]	69.9	-	3.0	66.8	55.8	-	3.0	53.1	86	-	3.1	83	0.5
	125, max [7, 8]	161	-	4.2	159	148	-	4.1	145	178	-	4.3	176	0.7
MWCT2D16S	25, typ [6]	19.6	-	2.8	17.6	6.0	-	2.8	4.0	36.2	-	2.9	33	0.5
	25, max [7]	23.5	-	3.2	22.1	7.9	-	3.1	8.2	40.7	-	3.2	38.4	0.8
	85, typ [6]	28.8	-	2.9	26.8	15.2	-	2.9	13.4	45.7	-	2.9	42.4	0.5

Table continues on the next page...

Table 14. Low speed RUN mode supply currents (continued)

	85, max [7]	41.8	-	3.5	39.6	27.7	-	3.4	25.9	58.7	-	3.5	55.3	0.8
	105, typ [6]	38.6	-	2.9	36.9	25	-	2.9	23.3	55.6	-	2.9	52.4	0.5
	105, max [7]	63.1	-	3.7	61.5	49	-	3.7	46.5	80.1	-	3.9	77.2	0.8
	125, typ [6]	50.7	-	2.9	49.6	37.2	-	2.9	35.5	67.9	-	3.0	64.7	0.5
	125, max [7, 8]	88.2	-	4.1	88.5	75.3	-	4.0	73.3	105.2	-	4.2	103.1	0.8
MWCT2016S	25, typ [6]	15	NA	NA		5	NA	NA		26	NA	NA		NA
	25, max [7]	20				10				32				
	85, typ [6]	20				10				31				
	85, max [7]	35.2				24.6				46.4				
	105, typ [6]	26.1				16.2				37				
	105, max [7]	52.9				42.6				64.2				
	125, typ [6]	35.3				25.3				46.4				
	125, max [7, 8, 9]	79.8				66.9				90.1				
MWCT2015S, MWCT2014S	25, typ [6]	12.9	NA	NA		4.4	NA	NA		22.4	NA	NA		NA
	25, max [7]	14.9				6.0				24.8				
	85, typ [6]	16.0				7.5				25.6				
	85, max [7]	31.0				22.2				41.1				
	105, typ [6]	19.1				10.5				28.7				
	105, max [7]	45.8				36.8				55.6				
	125, typ [6]	25.2				16.5				34.7				

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Table 14. Low speed RUN mode supply currents (continued)

	125, max [7], [8], [9]	73.2			64.3			82.4			

1. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
2. See the example configurations in Table 17.
3. IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
4. RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
5. RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail
6. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
7. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
8. For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.
9. If the total power dissipation would cause the junction temperature to be exceeded when VDD_HV_A is at 5V, then VDD_HV_A should be limited to operate at 3.3V.

NOTE

All data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C and typical silicon process unless otherwise stated.

Table 15. RUN mode supply currents (peripherals disabled)

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]												
		Min. Config. [2] Single Core @80 MHz [Clock Option F]		Min. Config. [2] Single Core @120 MHz [Clock Option B]		Min. Config. [2] Single Core @160 MHz [Clock Option A]		Min. Config. [2] Dual Core @80 MHz [Clock Option F]		Min. Config. [2] Dual Core @120 MHz [Clock Option B]		Min. Config. [2] Dual Core @160 MHz [Clock Option A]		All. Config. [2]
		VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_B [3]
MWCT2D17S	25, typ [6]	2.9	51.3	2.9	54.8	2.9	69.6	3.1	62.7	3.1	75.1	3.1	97.5	0.6
	25, max [7]	3.3	60.2	3.3	64.5	3.3	80.4	3.4	73.3	3.5	86.8	3.5	110	0.7
	85, typ [6]	3.0	64.5	3.0	68.1	3.0	83.1	3.1	76.2	3.2	89	3.2	111	0.4
	85, max [7]	3.6	104	3.6	108	3.7	124	3.8	117	3.9	131	3.8	155	0.6
	105, typ [6]	3.0	75.4	3.0	79	3.0	93.9	3.2	87.3	3.2	100	3.2	122.6	0.5
	105, max [7]	3.8	145	3.8	149	3.8	166	3.9	159	4.0	173	4.0	197	0.6
	125, typ [6]	3.1	97.4	3.1	101.2	3.1	116.4	3.3	110	3.3	122.9	3.3	145.7	0.5
	125, max [7, 8]	4.2	191	4.1	196	4.2	212	4.3	206	4.3	220	4.3	245	0.6
MWCT2D16S	25, typ [6]	2.8	49.5	2.8	52.2	2.9	66.3	3	58.9	2.9	72.7	3	93.7	0.5
	25, max [7]	3.3	58.5	3.3	62.4	3.3	75.9	3.3	68.1	3.4	82.9	3.5	104.6	0.7
	85, typ [6]	2.9	58.6	2.9	63.6	2.9	75.7	3	67.9	3	82.3	3	106.1	0.5
	85, max [7]	3.5	89.6	3.5	102.3	3.5	110.8	3.7	105.4	3.7	124.1	3.8	155	0.7

Table continues on the next page...

Table 15. RUN mode supply currents (peripherals disabled) (continued)

	105, typ [6]	3	68.3	3	76	3	85.6	3.1	80	3.1	92.3	3.1	119.3	0.5
	105, max [7]	3.6	124	3.7	143.4	3.7	157.5	3.9	150.5	3.9	164.5	4	191.6	0.7
	125, typ [6]	3.1	79.8	3.1	85.1	3.1	97.1	3.2	89.1	3.2	103.8	3.2	140.1	0.5
	125, max [7, 8]	3.9	146.7	4	164.7	4.1	178	4.1	171.3	4.2	188.7	4.2	235.6	0.7
MWCT2016S	25, typ [6]	37	NA	37	NA	NA		NA						NA
	25, max [7]	44		46										
	85, typ [6]	42		43										
	85, max [7]	58.5		59.7										
	105, typ [6]	48.1		48.7										
	105, max [7]	76.4		77.8										
	125, typ [6]	56.5		57										
	125, max [7, 8, 9]	98.7		99.9										
MWCT2015S, MWCT2014S	25, typ [6]	34.9	NA	36.5	NA	NA		NA						NA
	25, max [7]	39.1		41.1										
	85, typ [6]	38.1		39.8										
	85, max [7]	54.2		55.9										
	105, typ [6]	41.5		43.2										
	105, max [7]	69.1		71.1										
	125, typ [6]	47.7		49.4										
	125, max [7, 8, 9]	97		99.1										

1. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.

2. See the configurations in Table 18.
3. IO load current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.
4. RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
5. RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
6. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
7. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
8. For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, $T_J < 150°C$, to avoid self-heating.
9. If the total power dissipation would cause the junction temperature to be exceeded when VDD_HV_A is at 5V, then VDD_HV_A should be limited to operate at 3.3V.

NOTE

The data in this table is preliminary and based on first samples.

Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes VDD_HV_A = VREFH = 5 V, VDD_HV_B = 5V (if the VDD_HV_B domain present in the device), temperature = 25 °C and typical silicon process unless otherwise stated.

Table 16. Example RUN mode configuration supply currents

Chip	Ambient Temperature (°C)	RUN Mode (mA) [1]										
		Config. 1 [2] Dual Core @160 MHz		Config. 2 [2] Single Core @160 MHz		Config. 3 [2] Dual Core @120 MHz		Config. 4 [2] Single Core @120 MHz		Config. 5 [2] Single Core @80 MHz		Config. 1-6 [2]
		VDD_HV_A [3, 4]	V15 [5]/V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_A [3, 4]	V15 [5]/ V11	VDD_HV_B [3]
MWCT2D17S	25, typ [6]	2.9	119	3.0	102	3.1	106	3.0	80	2.9	68	0.6
	25, max [7]	3.3	133	3.3	115	3.5	119	3.4	92	3.4	79	0.7
	85, typ [6]	3.0	134	3.0	116	3.2	120	3.1	94	3.0	81.8	0.4
	85, max [7]	3.6	180	3.7	160	3.9	165	3.8	137	3.6	123	0.6
	105, typ [6]	3.0	145	3.1	128	3.2	132	3.1	105	3.0	93	0.5
	105, max [7]	3.8	222	3.9	203	4.0	208	3.9	179	3.6	165	0.6
	125, typ [6]	3.1	169	3.2	151	3.3	155	3.2	128	3.2	116	0.5
	125, max [7, 8]	4.3	271	4.3	250	4.5	256	4.4	226	4.2	213	0.6
MWCT2D16S	25, typ [6]	2.9	115.3	3.0	93.2	3.0	96.1	3.0	79.6	2.8	64.1	0.5
	25, max [7]	3.3	127.0	3.3	104.5	3.3	106.9	3.3	89.7	3.3	73.3	0.7
	85, typ [6]	2.9	125.0	3.0	102.7	3.0	105.8	3.0	89.2	2.9	73.6	0.5
	85, max [7]	3.6	178.8	3.6	126.5	3.6	132.0	3.6	105.0	3.5	92.5	0.7
	105, typ [6]	3.0	135.2	3.0	111.9	3.0	115.5	3.1	98.6	2.9	83.4	0.5

Table continues on the next page...

Table 16. Example RUN mode configuration supply currents (continued)

	105, max [7]	3.8	219.6	3.7	184.6	3.7	188.5	3.7	168.5	3.6	152.5	0.7
	125, typ [6]	3.1	145.8	3.1	123.8	3.1	127.3	3.1	110.2	3.0	94.7	0.5
	125, max [7, 8]	4.3	258.1	4.3	235.2	4.3	243.9	4.2	206.9	4.1	183.7	0.7
MWCT2016S	25, typ [6]	NA		NA		NA		54	NA	44	NA	NA
	25, max [7]							62		53		
	85, typ [6]							60		49		
	85, max [7]							76.4		66.3		
	105, typ [6]							65.8		55		
	105, max [7]							94.4		84.4		
	125, typ [6]							78.6		64.7		
	125, max [7, 8, 9]							120.7		110.5		
MWCT2015S, MWCT2014S	25, typ [6]	NA		NA		NA		53.4	NA	43	NA	NA
	25, max [7]							57.7		51.2		
	85, typ [6]							56.8		50.8		
	85, max [7]							73.2		66		
	105, typ [6]							60.1		54		
	105, max [7]							88.5		81.9		
	125, typ [6]							66.3		60.2		
	125, max [7, 8, 9]							115.3		109.3		

1. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
2. See the configurations in Table 18.
3. IO current is not included. The actual current requirements for IOs will depend on the I/O configuration in the application.

4. RUN IDD @ VDD_HV_A includes Flash memory read current from the V25 voltage rail.
5. RUN IDD @ V15 includes Flash memory read current from the V11 voltage rail.
6. “typ” is indicative of the average current numbers at the nominal internally regulated V11 supply voltage, VDD_HV_A = 5.0V, VDD_HV_B = 5.0V, V15 = 1.5V, for the typical silicon process.
7. “max” is indicative of the maximum current numbers at the maximum internally regulated V11 supply voltage (1.16 V), VDD_HV_A = 5.5V, VDD_HV_B = 5.5V, V15 = 1.65V, for the fast silicon process.
8. For the maximum allowable RUN current in an application, the junction temperature must be kept below the maximum specification, T_J < 150°C, to avoid self-heating.
9. If the total power dissipation would cause the junction temperature to be exceeded when VDD_HV_A is at 5V, then VDD_HV_A should be limited to operate at 3.3V.

6.8 Operating mode

Table 17. STANDBY and low speed RUN configuration options

MODULE	STANDBY All OFF	STANDBY SIRC ON	STANDBY FIRC ON	BOOT Mode (OptionC[1], FIRC @24 MHz)	Low Speed RUN (OptionE [1], FIRC @ 3MHz)	FIRC Mode (OptionD [1], FIRC @48 MHz)
Core M7_0/1	OFF	OFF	OFF	24 MHz	3 MHz	48 MHz
HSE_B	OFF	OFF	OFF	24 MHz	3 MHz	48 MHz
FIRC	OFF	OFF	24 MHz	24 MHz	3 MHz	48 MHz
FXOSC	OFF	OFF	OFF	OFF	OFF	OFF
SIRC	OFF	ON	OFF	ON	ON	ON
PLL	OFF	OFF	OFF	OFF	OFF	OFF
Flash	OFF	OFF	OFF	ON	ON	ON
eDMA	OFF	OFF	OFF	ON	ON	ON
FlexCAN	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPUART	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPSPI	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPI2C	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
EMAC/GMAC	OFF	OFF	OFF	OFF	OFF	OFF
eMIOS	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
SAR_ADC	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF
LPCMP	All OFF	All OFF	All OFF	All OFF	All OFF	All OFF

1. See clocking use case examples in the Clocking chapter of the MWCT2xxxS Reference Manual.

Table 18. RUN mode configuration options

MODULE	Min. Config. (OptionF[1]), PLL@80 MHz	Min. Config. (OptionB[1]), PLL@120 MHz	Min. Config. (OptionA[1]), PLL@160 MHz	Config. 1 Dual Core @160MHz	Config. 2 Single Core @160MHz	Config. 3 Dual Core @120MHz	Config. 4 Single Core @120MHz	Config. 5 Single Core @80MHz
Core M7_0	80 MHz	120 MHz	160 MHz	160 MHz	160 MHz	120 MHz	120 MHz	80 MHz
Core M7_1	80 MHz	120 MHz	160 MHz	160 MHz	-	120 MHz	-	-
Core M7_2	-	-	-	-	-	-	-	-

Table continues on the next page...

Table 18. RUN mode configuration options (continued)

HSE_B[2]	80 MHz	120 MHz	80 MHz	80 MHz	80 MHz	120 MHz	120 MHz	80 MHz
FIRC	ON	ON	ON	ON	ON	ON	ON	ON
FXOSC	ON	ON	ON	ON	ON	ON	ON	ON
SIRC	ON	ON	ON	ON	ON	ON	ON	ON
PLL	ON	ON	ON	ON	ON	ON	ON	ON
Flash	ON	ON	ON	ON	ON	ON	ON	ON
eDMA	ON	ON	ON	ON	ON	ON	ON	ON
FlexCAN[3]	All OFF	All OFF	All OFF	6x	2x	4x	6x	1x
LPUART[4]	All OFF	All OFF	All OFF	16x	4x	10x	8x	7x
LPSPI[5]	All OFF	All OFF	All OFF	6x	4x	4x	4x	3x
LPI2C[6]	All OFF	All OFF	All OFF	All OFF	2x	2x	2x	All OFF
EMAC/ GMAC[7]	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
SAI	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
QSPI	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
eMIOS[8]	All OFF	All OFF	All OFF	All OFF	3x	3x	2x	2x
SAR_ADC[9]	All OFF	All OFF	All OFF	All OFF	3x	3x	2x	2x
LPCMP[10]	All OFF	All OFF	All OFF	All OFF	2x	3x	All OFF	All OFF

1. See clocking use case examples in the Clocking chapter of the MWCT2xxxS Reference Manual.
2. HSE_B: After start-up, the HSE core is in WFI.
3.
    - FlexCAN0: Transmitting an 8-byte CAN-FD data frame at 5 Mbps, every 10 ms.
    - FlexCAN1: Transmitting a 64-byte CAN-FD data frame at 2 Mbps, every 20 ms.
    - FlexCAN2-5: Transmitting an 8-byte CAN data frame at 500 Kbps, every 20 ms.
4. LPUART0-15: Transmitting at 19200 bps, every 100ms.
5.
    - LPSPI0: Transmitting 32 bits at 20 Mbps (GPIO Fast pads), every 5 ms.
    - LPSPI1-5: Transmitting 32 bits at 1 Mbps, every 5 ms.
6. LPI2C0-1: Transmitting 3 bytes at 400 Kbps, every 100ms.
7. EMAC: ON for MII interface.
8.
    - eMIOS0: 6 channels in PWM mode @ 20 KHz.
    - eMIOS1-2: 8 channels in PWM mode @ 400 Hz.
9.
    - SAR_ADC0: 16 channels at 400 Hz rate, BCTU triggered.
    - SAR_ADC1-2: 4 channels at 20 KHz rate, BCTU triggered.
10. LPCMP0: 8 channels enabled; LPCMP1-2: 4 channels enabled.

6.9 Cyclic wake-up current

The cyclic wake-up current is the calculated average current consumption during the periodic switching between RUN mode and STANDBY mode. This average current can be calculated with the following formula:

ICYCL = RUN Current According to Ratio + STANDBY Current According to Ratio

Where the Current According to Ratio value is calculated as follows:

Current According to Ratio = Supply Current × Ratio of Duration

As an example, the following data was obtained with an application that periodically (every 40ms) alternates between RUN mode, for approximately 200μs to scan several GPIO inputs (51 GPIOS), and spends the rest of the time in STANDBY mode.

7 I/O parameters

7.1 GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

The leakage current on the GPIO pins is specified as a function of the pad type (Standard, Standard Plus, Medium, Fast, or GPI) and the number of Analog functions (CMP and ADC channels) multiplexed per pin.

For other devices, the "Analog Function Count" is defined from the number of CMP and ADC channels multiplexed to a given pin. This information can be obtained from the "Direct Signals" column in the IOMUX files attached to the Reference Manual. The "Analog Function Count" is shown in the Condition column of the following table.

Table 19. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.70 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 3.3V	—
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.30 x VDD_HV_A/B	V	VDD_HV_A/B = 3.3V	—
WFRST	RESET Input Filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_33_S0	3.3V input leakage current for Standard GPIO [3]	-133	—	300	nA	Pins with Analog Function Count = 0	—
ILKG_33_S1	3.3V input leakage current for Standard GPIO [3]	-545	—	445	nA	Pins with Analog Function Count = 1	—
ILKG_33_S2	3.3V input leakage current for Standard GPIO [3]	-749	—	517	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_33_S3	3.3V input leakage current for Standard GPIO [3]	-1288	—	679	nA	Pins with Analog Function Count = 3, plus PTD0	—

Table continues on the next page...

Table 19. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_33_S_PTE13	3.3V input leakage current for Standard GPIO [3]	-1935	—	483	nA	PMC VRC_CTRL pin	—
ILKG_33_SP0	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-370	—	575	nA	Pins with Analog Function Count = 0	—
ILKG_33_SP1	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-660	—	659	nA	Pins with Analog Function Count = 1	—
ILKG_33_SP2	3.3V input leakage current for Standard Plus GPIO and RESET IO [3]	-1094	—	749	nA	Pins with Analog Function Count = 2	—
ILKG_33_M0	3.3V GPIO input leakage current for Medium GPIO [3]	-792	—	750	nA	Pins with Analog Function Count = 0	—
ILKG_33_M1	3.3V GPIO input leakage current for Medium GPIO [3]	-989	—	824	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—
ILKG_33_M2	3.3V GPIO input leakage current for Medium GPIO [3]	-1233	—	1248	nA	Pins PTD6 and PTE8	—
ILKG_33_F0	3.3V GPIO input leakage current for Fast GPIO [3]	-1139	—	1178	nA	Pins with Analog Function Count = 0	—
ILKG_33_F1	3.3V GPIO input leakage current for Fast GPIO [3]	-1464	—	1239	nA	Pins with Analog Function Count = 1	—
ILKG_33_I	3.3V input leakage current for GPI [3]	-120	—	120	nA	—	—
VHYS_33	Input hysteresis voltage	0.06 x VDD_HV_A/B	—	—	mV	Always enabled.	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_33	3.3V GPIO pull up/ down resistance	20	—	60	kΩ	pull up @ 0.3 x VDD_HV_A/B, pull down @ 0.7 x VDD_HV_A/B	—

Table continues on the next page...

Table 19. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_33_S	3.3V output high current for Standard GPIO [4, 5]	1.0	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [4, 5]	1.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [4, 5]	3	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_F	3.3V output high current for Fast GPIO [4, 5]	4.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_SP	3.3V output high current for Standard Plus GPIO and RESET IO [4, 5]	3	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_M	3.3V output high current for Medium GPIO [4, 5]	6	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_33_F	3.3V output high current for Fast GPIO [4, 5]	9	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_33_S	3.3V output low current for Standard GPIO [4, 5]	1.0	—	—	mA	VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [4, 5]	1.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_M	3.3V output low current for Medium GPIO [4, 5]	3.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_F	3.3V output low current for Fast GPIO [4, 5]	4.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_33_SP	3.3V output low current for Standard Plus GPIO and RESET IO [4, 5]	3	—	—	mA	DSE =1, VOL <= 0.7V	—

Table continues on the next page...

Table 19. GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOL_33_M	3.3V output low current for Medium GPIO [4, 5]	6	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_33_F	3.3V output low current for Fast GPIO [4, 5]	9	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_33_S	3.3V maximum frequency for Standard GPIO [4, 6]	—	—	10	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF and external 10pF, total 25pF load	—
FMAX_33_SP	3.3V maximum frequency for Standard Plus GPIO [4, 6]	—	—	25	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF and external 10pF, total 25pF load	—
FMAX_33_M	3.3V maximum frequency for Medium GPIO [4, 6]	—	—	50	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF and external 10pF, total 25pF load	—
FMAX_33_F	3.3V maximum frequency for Fast GPIO [4, 6]	—	—	120	MHz	2.9V - 3.6V, internal 5pF, PCB trace ~10pF and external 10pF, total 25pF load	—
IOHT	Output high current total for all ports [7]	—	—	100	mA	—	—

1. Maximum length of RESET pulse will be filtered by an internal filter on this pin.
2. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
3. A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
4. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
5. I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
6. I/O timing specifications are valid for the un-terminated transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 1.5pF/inch (25pF total with margin). For signals with frequency greater than 63MHz, a maximum 2 inch PCB trace is assumed.
7. To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

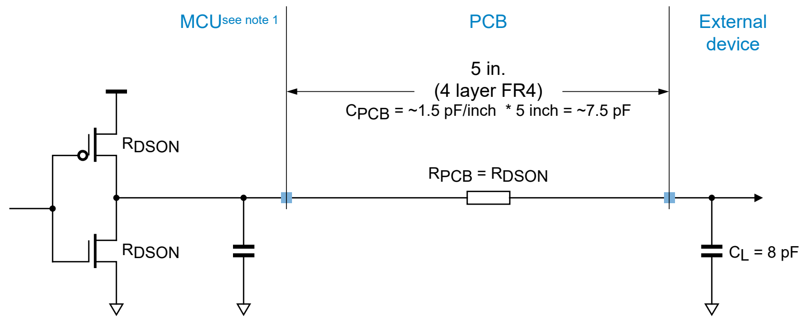

Figure 13. Reference Load Diagram

7.2 GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

The leakage current on the GPIO pins is specified as a function of the pad type (Standard, Standard Plus, Medium, Fast, or GPI) and the number of Analog functions (CMP and ADC channels) multiplexed per pin.

For other devices, the "Analog Function Count" is defined from the number of CMP and ADC channels multiplexed to a given pin. This information can be obtained from the "Direct Signals" column in the IOMUX files attached to the Reference Manual. The "Analog Function Count" is shown in the Condition column of the following table.

Table 20. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VIH	Input high level DC voltage threshold	0.65 x VDD_HV_A/B	—	VDD_HV_A/B + 0.3	V	VDD_HV_A/B = 5.0V	—
VIL	Input low level DC voltage threshold	VSS - 0.3	—	0.35 x VDD_HV_A/B	V	VDD_HV_A/B = 5.0V	—
WFRST	RESET Input filtered pulse width [1]	—	—	33	ns	—	—
WNFRST	RESET Input not filtered pulse width [2]	100	—	—	ns	—	—
ILKG_50_S0	5.0V input leakage current for Standard GPIO [3]	-193	—	389	nA	Pins with Analog Function Count = 0	—
ILKG_50_S1	5.0V input leakage current for Standard GPIO [3]	-691	—	580	nA	Pins with Analog Function Count = 1	—
ILKG_50_S2	5.0V input leakage current for Standard GPIO [3]	-947	—	673	nA	Pins with Analog Function Count = 2, plus PTA12, PTD1	—
ILKG_50_S3	5.0V input leakage current for Standard GPIO [3]	-1614	—	879	nA	Pins with Analog Function Count = 3, plus PTD0	—

Table continues on the next page...

Table 20. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
ILKG_50_S_PTE13	5.0V input leakage current for Standard GPIO [3]	-2335	—	619	nA	PMC VRC_CTRL pin	—
ILKG_50_SP0	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-553	—	736	nA	Pins with Analog Function Count = 0	—
ILKG_50_SP1	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-855	—	846	nA	Pins with Analog Function Count = 1	—
ILKG_50_SP2	5.0V input leakage current for Standard Plus GPIO and RESET IO [3]	-1389	—	1017	nA	Pins with Analog Function Count = 2	—
ILKG_50_M0	5.0V input leakage current for Medium GPIO [3]	-1036	—	951	nA	Pins with Analog Function Count = 0	—
ILKG_50_M1	5.0V input leakage current for Medium GPIO [3]	-1284	—	1057	nA	Pins with Analog Function Count = 1, plus PTC16, PTD5	—
ILKG_50_M2	5.0V input leakage current for Medium GPIO [3]	-1518	—	1289	nA	Pins PTD6 and PTE8	—
ILKG_50_F0	5.0V input leakage current for Fast GPIO [3]	-1675	—	1497	nA	Pins with Analog Function Count = 0	—
ILKG_50_F1	5.0V input leakage current for Fast GPIO [3]	-1805	—	1573	nA	Pins with Analog Function Count = 1	—
ILKG_50_I	5.0V input leakage current for GPI [3]	-150	—	150	nA	—	—
VHYS_50	input hysteresis voltage	0.06 x VDD_HV _A/B	—	—	mV	Always enabled.	—
CIN	GPIO Input capacitance	2	4	6	pF	add 2pF for package/ parasitic	—
IPU_50	5.0V GPIO pull up/ down resistance	20	—	55	kΩ	pull up @ 0.3 * VDD_ HV_*, pull down @ 0.7 * VDD_HV_*	—

Table continues on the next page...

Table 20. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOH_50_S	5.0V output high current Standard GPIO [4, 5]	1.6	—	—	mA	VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current Standard Plus GPIO and RESET IO [4, 5]	2.5	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [4, 5]	4.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_F	5.0V output high current for Fast GPIO [4, 5]	6.0	—	—	mA	DSE = 0, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_SP	5.0V output high current for Standard Plus GPIO and RESET IO [4, 5]	5.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_M	5.0V output high current for Medium GPIO [4, 5]	8.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOH_50_F	5.0V GPIO output high current for Fast GPIO [4, 5]	12.0	—	—	mA	DSE = 1, VOH >= VDD_HV_A/B - 0.7V	—
IOL_50_S	5.0V output low current for Standard GPIO [4, 5]	1.6	—	—	mA	VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [4, 5]	2.5	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_M	5.0V output low current for Medium GPIO [4, 5]	4.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_F	5.0V output low current for Fast GPIO [4, 5]	6.0	—	—	mA	DSE =0, VOL <= 0.7V	—
IOL_50_SP	5.0V output low current for Standard Plus GPIO and RESET IO [4, 5]	5.0	—	—	mA	DSE =1, VOL <= 0.7V	—

Table continues on the next page...

Table 20. GPIO DC electrical specifications, 5.0V (4.5V - 5.5V) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
IOL_50_M	5.0V output low current for medium GPIO [4, 5]	8.0	—	—	mA	DSE =1, VOL <= 0.7V	—
IOL_50_F	5.0V output low current for Fast GPIO [4, 5]	12.0	—	—	mA	DSE =1, VOL <= 0.7V	—
FMAX_50_S	5.0V maximum frequency for Standard GPIO [4, 6]	—	—	10	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_SP	5.0V maximum frequency for Standard Plus GPIO [4, 6]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_M	5.0V maximum frequency for Medium GPIO [4, 6]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
FMAX_50_F	5.0V maximum frequency for Fast GPIO [4, 6]	—	—	25	MHz	3.6V - 5.5V CL (max) = 25pF	—
IOHT	Output high current total for all ports [7]	—	—	100	mA	—	—

1. Maximum length of RESET pulse will be filtered by an internal filter on this pin.
2. Minimum length of RESET pulse, guaranteed not to be filtered by the internal filter.
3. A positive value is leakage flowing into pin with pin at VDD_HV_A/B (the GPIO supply level); a negative value is leakage flowing out the pin with the pin at ground.
4. GPIO output transition time information can be obtained from the device IBIS model. IBIS models are recommended for system level simulations, as discrete values for I/O transition times are not representative of the I/O pad behavior when connected to an actual transmission line load.
5. I/O output current specifications are valid for the given reference load figure, and the constraints given in the Operating Conditions of this document.
6. I/O timing specifications are valid for the un-terminated transmission line reference load given in the figure below. A lumped 8pF load is assumed at the end of a 5 inch microstrip trace on standard FR4 with approximately 1.5pF/inch (25pF total with margin).
7. To determine total switching current on any I/O supply, current values per output pin should not be incrementally summed. I/O interfaces on the device are asynchronous to each other, so not all switching occurs at the same instant. Actual use case must be considered.

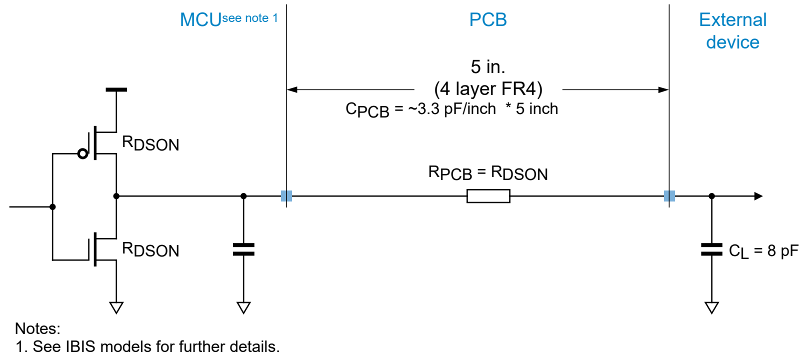

Figure 14. Reference Load Diagram

7.3 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Table 21. 5.0V (4.5V - 5.5V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_S	5.0V Standard GPIO rise/fall time	5	—	21	ns	CL (max) = 25pF	—
TR_TF_50_S	5.0V Standard GPIO rise/fall time	8.5	—	31	ns	CL (max) = 50pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	3	—	13.2	ns	DSE=0, CL (max) = 25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	1	—	7.1	ns	DSE=1, CL (max) = 25pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	6.4	—	18.8	ns	DSE=0, CL (max) = 50pF	—
TR_TF_50_SP	5.0V Standard Plus GPIO rise/fall time	3.4	—	11	ns	DSE=1, CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	1.8	—	8.2	ns	DSE=0, SRE=0, CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	2.5	—	9.8	ns	DSE=0, SRE=1, CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	0.7	—	4.5	ns	DSE=1, SRE=0, CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	1.8	—	7.2	ns	DSE=1, SRE=1, CL (max) = 25pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	3.95	—	13.2	ns	DSE=0, SRE=0, CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	4.3	—	13.8	ns	DSE=0, SRE=1, CL (max) = 50pF	—

Table continues on the next page...

Table 21. 5.0V (4.5V - 5.5V) GPIO Output AC Specification (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_50_M	5.0V Medium GPIO rise/fall time	1.6	—	7.1	ns	DSE=1, SRE=0, CL (max) = 50pF	—
TR_TF_50_M	5.0V Medium GPIO rise/fall time	2.7	—	9.6	ns	DSE=1, SRE=1, CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	0.4	—	3.15	ns	DSE=0, SRE=0, CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	1.5	—	6.7	ns	DSE=0, SRE=1, CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	0.3	—	2.02	ns	DSE=1, SRE=0, CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	0.9	—	4.85	ns	DSE=1, SRE=1, CL (max) = 25pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	1.0	—	5.8	ns	DSE=0, SRE=0, CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	1.9	—	8.5	ns	DSE=0, SRE=1, CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	0.9	—	3.0	ns	DSE=1, SRE=0, CL (max) = 50pF	—
TR_TF_50_F	5.0V Fast GPIO rise/ fall time	1.3	—	6.1	ns	DSE=1, SRE=1, CL (max) = 50pF	—

7.4 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Table 22. 3.3V (2.97V - 3.63V) GPIO Output AC Specification

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_S	3.3V Standard GPIO rise/fall time	5	—	28	ns	CL (max) = 25pF	—
TR_TF_33_S	3.3V Standard GPIO rise/fall time	9.5	—	43	ns	CL (max) = 50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	4	—	17.5	ns	DSE=0, CL (max) = 25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	1.9	—	10	ns	DSE=1, CL (max) = 25pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	7.5	—	27	ns	DSE=0, CL (max) = 50pF	—
TR_TF_33_SP	3.3V Standard Plus GPIO rise/fall time	3.5	—	15	ns	DSE=1, CL (max) = 50pF	—

Table continues on the next page...

Table 22. 3.3V (2.97V - 3.63V) GPIO Output AC Specification (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TR_TF_33_M	3.3V Medium GPIO rise/fall time	2.2	—	12.3	ns	DSE=0, SRE=0, CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	3.0	—	14	ns	DSE=0, SRE=1, CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	0.8	—	6.6	ns	DSE=1, SRE=0, CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	2.4	—	10.5	ns	DSE=1, SRE=1, CL (max) = 25pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	4.5	—	17.3	ns	DSE=0, SRE=0, CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	5	—	19.8	ns	DSE=0, SRE=1, CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	2.2	—	10	ns	DSE=1, SRE=0, CL (max) = 50pF	—
TR_TF_33_M	3.3V Medium GPIO rise/fall time	3.6	—	13.9	ns	DSE=1, SRE=1, CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	0.5	—	4.9	ns	DSE=0, SRE=0, CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	2.1	—	10	ns	DSE=0, SRE=1, CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	0.4	—	2.2	ns	DSE=1, SRE=0, CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	1.2	—	7.1	ns	DSE=1, SRE=1, CL (max) = 25pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	1.1	—	8	ns	DSE=0, SRE=0, CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	2.6	—	12.1	ns	DSE=0, SRE=1, CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	0.8	—	4.2	ns	DSE=1, SRE=0, CL (max) = 50pF	—
TR_TF_33_F	3.3V Fast GPIO rise/ fall time	1.5	—	8.6	ns	DSE=1, SRE=1, CL (max) = 50pF	—

8 Glitch Filter

The glitch filter parameters in the following table apply to the filters of WKPU pins and TRGMUX inputs 60-63.

Table 23. Glitch Filter

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TFILT	Glitch filter max filtered pulse width [1, 2, 3]	—	—	20	ns	—	—
TUNFILT	Glitch filter min unfiltered pulse width [1, 3, 4]	400	—	—	ns	—	—

1. An input signal pulse is defined by the duration between the input signal's crossing of a Vil/Vih threshold voltage level, and the next crossing of the opposite level.
2. Pulses shorter than defined by the maximum value are guaranteed to be filtered (not passed).
3. Pulses in between the max filtered and min unfiltered may or may not be passed through.
4. Pulses larger than defined by the minimum value are guaranteed to not be filtered (passed).

9 Flash memory specification

9.1 Flash memory program and erase specifications

Table 24. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3,4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 100,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	102	122	129	111	150		μs
t_{ppgm}	Page (256 bits) program time	142	171	180	157	200		μs
t_{qppgm}	Quad-page (1024 bits) program time	314	377	396	341	450		μs
t_{8kpgm}	8 KB Sector program time	20	24	26	22	30		ms
t_{8kers}	8 KB Sector erase time	4.8	8.5	10.6	6.5	30		ms
$t_{256kbers}$	256KB Block erase time	22.8	27.4	28.8	24.4	40	—	ms
$t_{512kbers}$	512KB Block erase time	25.4	30.5	32.1	27.9	45	—	ms
t_{1mbers}	1MB Block erase time	30.6	36.8	38.7	33.6	50	—	ms
t_{2mbers}	2MB Block erase time	41.1	49.3	51.8	45.2	60	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Sector program times assume quad-page programming.

2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 25 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤T_J ≤150°C, full spec voltage.

9.2 Flash memory Array Integrity and Margin Read specifications

Table 25. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1] [2]	Units[3]
$t_{ai256kseq}$	Array Integrity time and Margin Read time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai512kseq}$	Array Integrity time and Margin Read time for sequential sequence on 512KB block.	—	—	16384 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai1mseq}$	Array Integrity time and Margin Read time for sequential sequence on 1MB block.	—	—	32768 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai2mseq}$	Array Integrity time and Margin Read time for sequential sequence on 2MB block.	—	—	65536 x Tperiod x Nread (plus 40uS adder required if User Margin Read)	—
$t_{ai256kprop}$	Array Integrity time for proprietary sequence on 256KB block.	—	—	106496 x Tperiod x Nread	—
$t_{ai512kprop}$	Array Integrity time for proprietary sequence on 512KB block.	—	—	229376 x Tperiod x Nread	—
$t_{ai1mprop}$	Array Integrity time for proprietary sequence on 1MB block.	—	—	491520 x Tperiod x Nread	—
$t_{ai2mprop}$	Array Integrity time for proprietary sequence on 2MB block.	—	—	1048576 x Tperiod x Nread	—

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including single read, dual read, quad read contribution. Thus for a read setup that requires 6 clocks to read Nread would equal 6.
2. Array Integrity times are actual hardware execution times and do not include software overhead or system code execution overhead.
3. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

9.3 Flash memory module life specifications

Table 26. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 256 KB and 512 KB blocks using Sector Erase.	—	100,000	—	P/E cycles
	Number of program/erase cycles per block for 1 MB and 2 MB blocks using Sector Erase.	—	1,000	—	P/E cycles
	Number of program/erase cycles per block using Block Erase[1]	—	25	—	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	20	—	Years
		Blocks with 100,000 P/E cycles.	10	—	Years

1. Program and erase supported for factory conditions. Nominal supply values and operation at 25°C.

9.3.1 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure.

The spec window represents qualified limits.

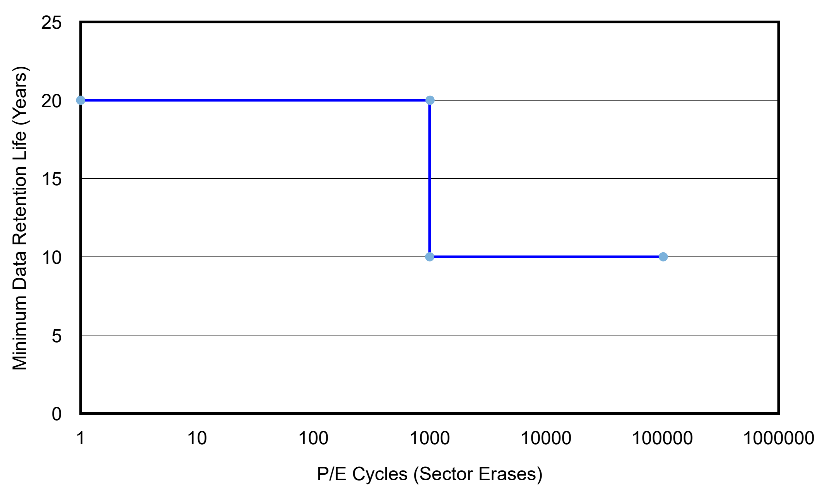

Figure 15. Data retention vs program/erase cycles

9.4 Flash memory AC timing specifications

Table 27. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{done}	Time from 0 to 1 transition on the MCR[EHV] bit initiating a program/erase until the MCR[DONE] bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR[EHV] bit aborting a program/erase until the MCR[DONE] bit is set to a 1.	5 plus four system clock periods	—	22 plus four system clock periods[1]	μs
t_{drcv}	Time to recover once exiting low power mode.	14 plus seven system clock periods[2]	17.5 plus seven system clock periods	21 plus seven system clock periods	μs
$t_{aistart}$	Time from 0 to 1 transition of UT0[AIE] initiating a Margin Read or Array Integrity until the UT0[AID] bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing UT0[AISUS] or clearing UT0[NAIBP]	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0[AIE] initiating an Array Integrity abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Array Integrity suspend request.	—	—	50 system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0[AIE] initiating a Margin Read abort until the UT0[AID] bit is set. This time also applies to the UT0[AISUS] to UT0[AID] setting in the event of a Margin Read suspend request.	—	—	26 plus fifteen system clock periods	μs

1. For Block Erase, Tdones times may be 3x max spec.
2. In extreme cases (1 block configurations) Tdrcv min may be faster (12uS plus seven system clocks)

9.5 Flash memory read timing parameters

Table 28. Flash Read Wait State Settings (MWCT2014S, MWCT2015S, MWCT2016S, MWCT2D16S, and MWCT2D17S)

Flash Frequency	RWSC setting
250 KHz < Freq ≤ 66 MHz	1
66 MHz < Freq ≤ 100 MHz	2
100 MHz < Freq ≤ 133 MHz	3
133 MHz < Freq ≤ 167 MHz	4
167 MHz < Freq ≤ 200 MHz	5

Table continues on the next page...

Table 28. Flash Read Wait State Settings (MWCT2014S, MWCT2015S, MWCT2016S, MWCT2D16S, and MWCT2D17S) (continued)

Flash Frequency	RWSC setting
200 MHz < Freq ≤ 233 MHz	6
233 MHz < Freq ≤ 250 MHz	7

10 Analog modules

10.1 SAR ADC

All below specs are applicable only when one ADC instance is in operation and averaging is used or multiple ADC instances are operational at the same time but sampling different channels. Best performance can be achieved if only one ADC is operational at a time sampling one channel.

Table 29. SAR ADC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VDD_HV_A	ADC Supply Voltage [1]	2.97	—	5.5	V	—	—
DVREFL	VSS / VREFL Voltage Difference [2]	-100	—	100	mV	—	—
VAD_INPUT	ADC Input Voltage [3]	VREFL	—	VREFH	V	—	—
fAD_CK	ADC Clock Frequency (MWCT2D16S, MWCT2D17S)	10	—	80	MHz	—	—
fAD_CK	ADC Clock Frequency (MWCT2016S, MWCT2015S, MWCT2014S)	10	—	120	MHz	—	—
tSAMPLE	ADC Input Sampling Time	275	—	—	ns	—	—
tCONV	ADC Total Conversion Time	1	—	—	us	12-bit result	—
tCONV	ADC Total Conversion Time	0.9	—	—	us	10-bit result	—
CAD_INPUT	ADC Input Capacitance	—	—	13.8	pF	ADC component plus pad capacitance (~2pF)	—
RAD_INPUT	ADC Input Resistance	—	—	4.6	KΩ	ADC + mux+SOC routing	—

Table continues on the next page...

Table 29. SAR ADC (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RS	Source Impedance, precision channels	—	20	—	Ω	—	—
RS	Source Impedance, standard channels	—	20	—	Ω	—	—
TUE	ADC Total Unadjusted Error [4] [5]	—	+/-4	+/-6	LSB	without adjacent pin current injection	—
TUE	ADC Total Unadjusted Error [4]	—	+/-4	+/-8	LSB	with up to +/-3mA of current injection on adjacent pins	—
IAD_REF	Current Consumption on ADC Reference pin, VREFH.	—	—	200	uA	Per ADC for dedicated or shared reference pins	—
IDDA	Current Consumption on ADC Supply, VDD_HV_A	—	2.1	—	mA	Current consumption per ADC module, ADC enabled and converting	—
CS	Sampling Capacitance	6.4 (gain=0) 9.72 pF(gain=max)	7.36 (gain=0) 11.12 pF(gain=max)	8.32 (gain=0) 12.52 (gain=max)	pF	all channels	—
RAD	Sampling Switch Impedance	80	170	520	Ohm	all channels	—
CP1	Pin capacitance	1.42	—	5.30	pF	all channels	—
CP1	Pin capacitance	1.42	—	4.38	pF	Precision channels	—
CP1	Pin capacitance	1.61	—	5.30	pF	Standard channels	—
CP2	Analog Bus Capacitance	0.32	—	4.18	pF	all channels	—
CP2	Analog Bus Capacitance	0.32	—	1.42	pF	Precision channels	—
CP2	Analog Bus Capacitance	0.497	—	4.18	pF	Standard channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	all channels	—
RSW1	Channel selection Switch impedance	65.9	—	712	Ohm	Precision channels	—
RSW1	Channel selection Switch impedance	65.9	—	1410	Ohm	Standard channels	—

1. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC.

2. VSS and VREFL should be shorted on PCB. 100mV difference between VSS and VREFL is for transient only (not for DC).
3. This is ADC Input range for ADC accuracy guaranteed in this input range only. For SoC Pin capability, see Operation Condition Section.
4. TUE spec for precision and standard channels is based on 12-bit level resolution.
5. Spec valid if potential difference between VDD_HV_A and VREFH should follow VDD_HV_A +0.1V >=VREFH >= VDD_HV_A -1.5V.

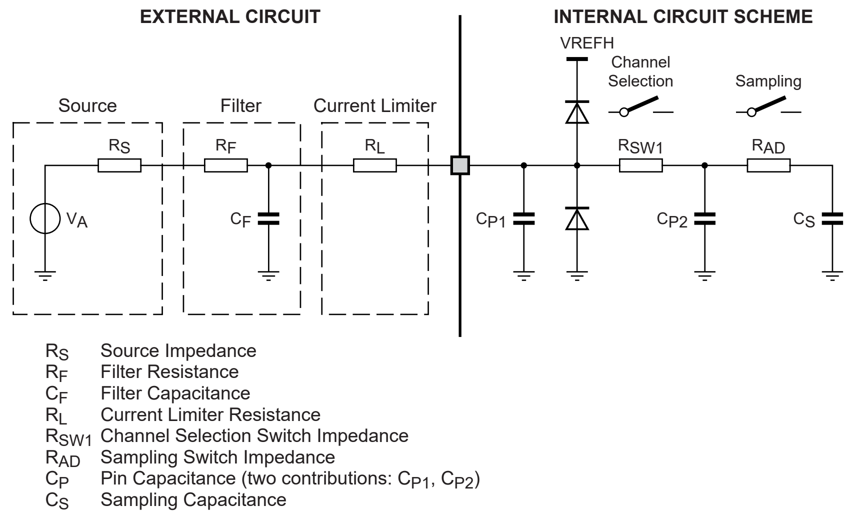

Figure 16. SAR ADC Input Circuit

10.2 Supply Diagnosis

The table below gives the specification for the on die supply diagnosis.

Table 30. Supply Diagnosis

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
AN_ACC	Offset to internally monitored supply at ADC input [1, 2, 3]	-5	0	5	%	—	—
AN_T_on	Switching time from closed (OFF) to conducting (ON) [3]	—	2.5	12	ns	—	—
AN_TADCSA	Required ADC sampling time [1]	1.2	—	—	μs	—	—

1. Required ADC sampling time specified by parameter AN_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
2. If V15 > VDD_HV_A +100mV then the V15 measurement via anamux may be imprecise.
3. These specs will have degraded performance when used in extended supply voltage operation range, i.e. normal supply voltage range specification is exceeded.

10.3 Low Power Comparator (LPCMP)

Table 31. Low Power Comparator (LPCMP)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
idda(IDHSS)	vdda Supply Current, High Speed Mode [1, 2]	—	240	—	uA	—	—
idda(IDLSS)	vdda Supply Current, Low Speed Mode [1, 2]	—	17	—	uA	—	—
idda(IDHSS)	vdda Supply Current, high speed mode, DAC only [1]	—	10	—	uA	—	—
idda_lkg	vdda Supply Current, module disabled [1]	—	2	—	nA	vdda=5.5V, T=25C	—
TDHSB	Propagation Delay, High Speed Mode [3]	—	—	200	ns	—	—
TDLSB	Propagation Delay, Low Speed mode [3]	—	—	2	us	—	—
TDHSS	Propagation Delay, High Speed Mode [4]	—	—	400	ns	—	—
TDLSS	Propagation Delay, Low Speed mode [4]	—	—	5	us	—	—
TIDHS	Initialization Delay, High Speed Mode [5]	—	—	3	us	—	—
TIDLS	Initialization Delay, Low Speed mode [5]	—	—	30	us	—	—
VAIO	Analog Input Offset Voltage, High Speed Mode	-25	+/-1	25	mV	—	—
VAIO	Analog Input Offset Voltage, Low Speed mode	-40	+ /- 5	40	mV	—	—
VAHYST0	Analog Comparator Hysteresis, High Speed Mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, High Speed Mode	—	14	41	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, High Speed Mode	—	27	76	mV	HYSTCTR[1:0]= 2'b10	—

Table continues on the next page...

Table 31. Low Power Comparator (LPCMP) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
VAHYST3	Analog Comparator Hysteresis, High Speed Mode	—	40	111	mV	HYSTCTR[1:0]= 2'b11	—
VAHYST0	Analog Comparator Hysteresis, Low Speed mode	—	0	—	mV	HYSTCTR[1:0]= 2'b00	—
VAHYST1	Analog Comparator Hysteresis, Low Speed mode	—	8	60	mV	HYSTCTR[1:0]= 2'b01	—
VAHYST2	Analog Comparator Hysteresis, Low Speed mode	—	15	113	mV	HYSTCTR[1:0]= 2'b10	—
VAHYST3	Analog Comparator Hysteresis, Low Speed mode	—	23	165	mV	HYSTCTR[1:0]= 2'b11	—
INL	DAC integral linearity [1, 6, 7]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
INL	DAC integral linearity [1, 6, 7]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
DNL	DAC differential linearity [1, 6]	-1	—	1	LSB	vrefh_cmp = vdda, vrefl_cmp = vss	—
DNL	DAC differential linearity [1, 6]	-1.5	—	1.5	LSB	vrefh_cmp < vdda	—
tDDAC	DAC Initialization and switching settling time	—	—	30	us	—	—
VAIN	Analog input voltage	0	—	VDDA	V	—	—

1. vdda is comparator HV supply and internally shorted to VDD_HV_A pin. vss is comparator ground
2. Difference at input > 200mV
3. Applied +/- (100 mV + VAHYST0/1/2/3 + max. of VAIO) around switch point
4. Applied +/- (30 mV + 2 x VAHYST0/1/2/3 + max. of VAIO) around switch point
5. Applied ± (100 mV + VAHYST0/1/2/3).
6. 1 LSB = (vrefh_cmp - vrefl_cmp) /256. vrefh_cmp and vrefl_cmp are comparator reference high and low
7. Calculation method used: Linear Regression Least Square Method

For Comparator IN signals adjacent to VDD_HV_A/VDD_HV_B/VSS or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired Comparator performance. Additionally an external capacitor to ground (1nF) should be used to filter noise on input signal. Also source drive should not be weak (Signal with <50K pull up/down is recommended).

For devices where the VDD_HV_B domain is present, ACMP0 channels must only be selected/enabled when VDD_HV_A >= VDD_HV_B. These channels must be disabled when VDD_HV_A goes below VDD_HV_B.

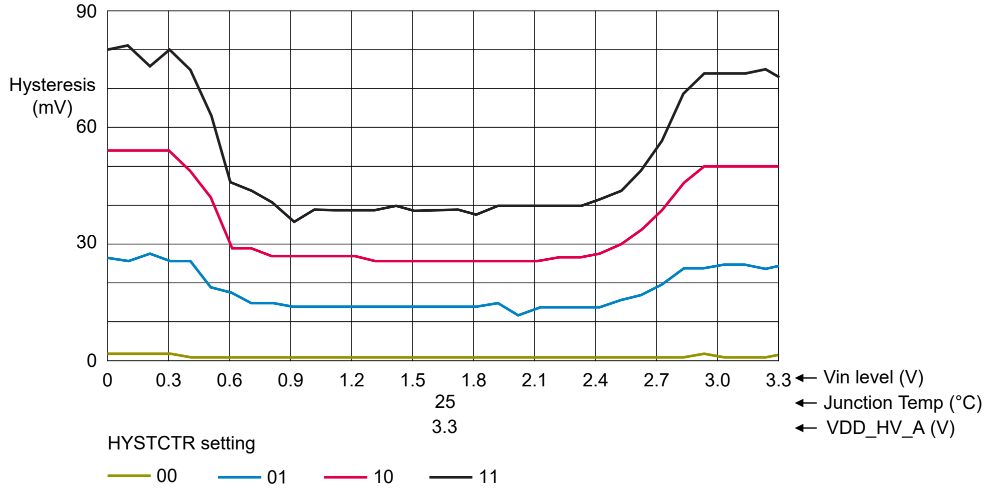

Figure 17. Typical Hysteresis vs Vin level (VDD_HV_A = 3.3 V, High Speed Mode)

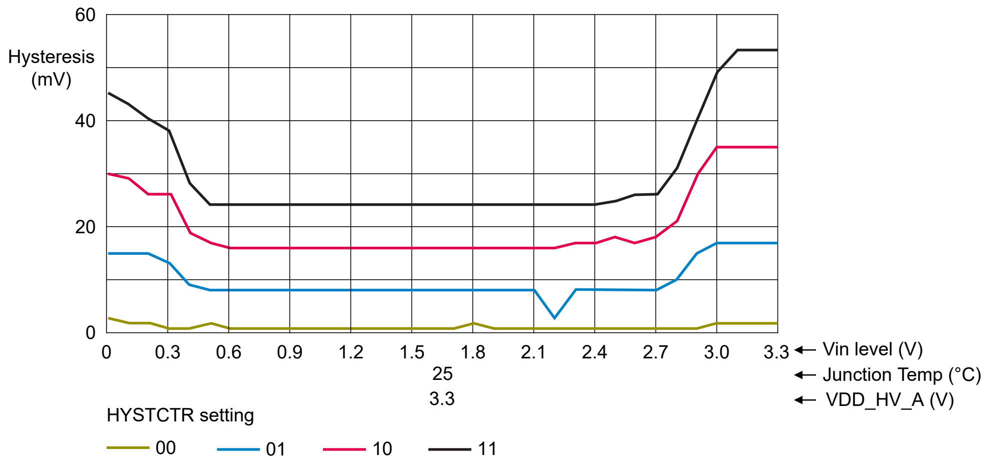

Figure 18. Typical Hysteresis vs Vin level (VDD_HV_A = 3.3 V, Low Speed Mode)

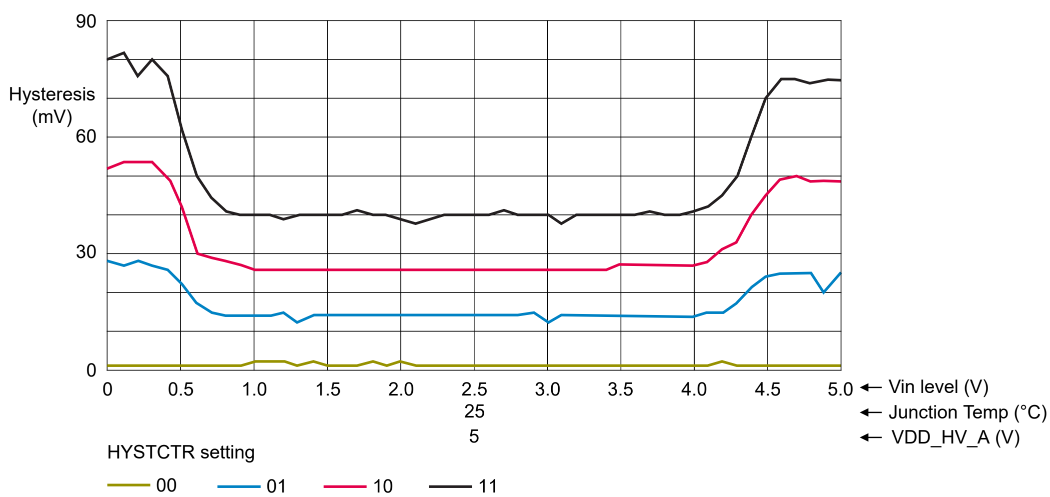

Figure 19. Typical Hysteresis vs Vin level (VDD_HV_A = 5 V, High Speed Mode).png

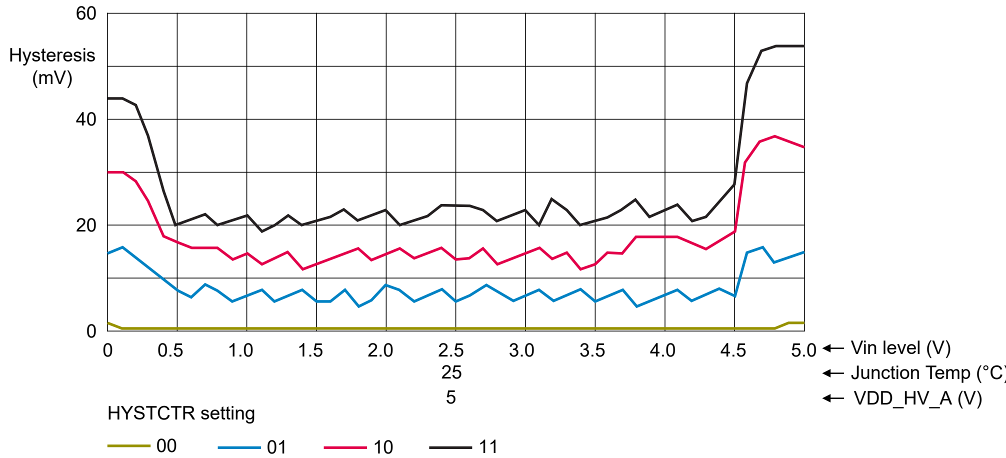

Figure 20. Typical Hysteresis vs Vin level (VDD_HV_A = 5 V, Low Speed Mode).png

10.4 Temperature Sensor

The table below gives the specification for the on die temperature sensor.

Table 32. Temperature Sensor

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
TS_TJ	Junction temperature monitoring range	-40	—	150	°C	—	—
TS_IV25	ON state current consumption on V25	—	400	—	µA	ETS_EN=1	—
TS_ACC1	Temperature output error at circuit output (Voltage) [1, 2, 3]	-5	0	+5	°C	100 °C < Tj <= 150 °C	—
TS_ACC2	Temperature output error at circuit output (Voltage) [1, 2, 3]	-10	0	+10	°C	-40 °C <= Tj <=100 °C	—
TS_TSTART	Circuit start up time	—	4	30	µs	—	—
TS_TADCSA	Required ADC sampling time [1]	1.2	—	—	µs	—	—

1. Required ADC sampling time specified by parameter TS_TADCSA needs to be used at the ADC conversion to guarantee the specified accuracy. A smaller sampling time leads to a less accurate result.
2. Note: The temperature sensor measures the junction temperature Tj at the location where it is placed on die. The local Tj is modulated by current and previous active state of the circuit elements on die.
3. The error caused by ADC conversion and provided temperature calculation formula is not included.

11 Clocking modules

11.1 FIRC

Table 33. FIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fFIRC	FIRC nominal Frequency	—	48	—	MHz	—	—
FACC	FIRC Frequency deviation across process, voltage, and temperature after trimming	-5	—	5	%	—	—
TSTART	Startup Time [1]	—	10	25	us	—	—

1. Startup time is for reference only.

11.2 SIRC

Table 34. SIRC

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSIRC	SIRC nominal Frequency	—	32	—	KHz	—	—
fSIRC_ACC	SIRC Frequency deviation across process, voltage, and temperature after trimming	-10	—	10	%	—	—
TSIRC_start	SIRC Startup Time [1]	—	—	3	ms	—	—
TSIRC_DC	SIRC duty cycle	30	—	70	%	—	—

1. Startup time is for information only.

11.3 PLL

Table 35. PLL

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FPLL_in	PLL input frequency	8	—	40	MHz	This is the frequency after the Reference Divider within the PLL	—
FPLL_out	PLL output frequency (PLL_PHIn_CLK)	25	—	320	MHz	—	—

Table continues on the next page...

Table 35. PLL (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FPLL_vcoRange	VCO Frequency range	640	—	1280	MHz	—	—
FPLL_DS	Modulation Depth (down spread)	-0.5	—	-3	%	—	—
FPLL_FM	Modulation frequency	—	—	32	KHz	—	—
TPLL_start	PLL lock time	—	—	1	ms	—	—
JPLL_cyc	PLL period jitter (pk-pk) [1, 2, 3]	—	—	237	ps	FPLL_out = 240MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1, 2, 3]	—	—	487	ps	FPLL_out = 240MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1, 2, 3]	—	—	840	ps	FPLL_out = 240MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1, 2, 3]	—	—	1680	ps	FPLL_out = 240MHz, Fractional Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1, 2, 3]	—	—	295	ps	FPLL_out = 160MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1, 2, 3]	—	—	670	ps	FPLL_out = 160MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1, 2, 3]	—	—	840	ps	FPLL_out = 160MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1, 2, 3]	—	—	1680	ps	FPLL_out = 160MHz, Fractional Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1, 2, 3]	—	—	353	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_cyc	PLL period jitter (pk-pk) [1, 2, 3]	—	—	853	ps	FPLL_out = 120MHz, Fractional Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1, 2, 3]	—	—	840	ps	FPLL_out = 120MHz, Integer Mode	—
JPLL_acc	PLL accumulated jitter (pk-pk) [1, 2, 3]	—	—	1680	ps	FPLL_out = 120MHz, Fractional Mode	—

1. For SSCG, jitter due to systematic modulation needs to be added as per applied modulation.
2. Jitter numbers are valid only at IP boundary and does not include any degradation due to IO pad for clock measurement.
3. Jitter numbers calculated by extrapolating RMS jitter numbers to +/- 7 sigma .

11.4 Fast External Oscillator (FXOSC)

Table 36. Fast External Oscillator (FXOSC)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
FREQ_BYPASS	Input clock frequency in bypass mode [1]	—	—	50	MHz	—	—
TRF_BYPASS	Input clock rise/fall time in bypass mode [1]	—	—	5	ns	—	—
CLKIN_DUTY_BYPASS	Input clock duty cycle in bypass mode [1]	47.5	—	52.5	%	—	—
FXOSC_CLK	output clock frequency in crystal mode	8	—	40	MHz	—	—
TFXOSC	Fxosc start up time (ALC enabled) [2]	—	—	2	ms	—	—
IFXOSC	Oscillator Analog circuit supply current, V25 supply (ALC disabled)	—	—	2.7	mA	using 8, 16 or 40 MHz crystal	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC enabled)	0.3	—	1.4	V	—	—
EXTAL_SWING_PP	Peak-to-peak voltage swing on EXTAL pin in crystal oscillator mode (ALC disabled) [3]	1.2	—	2.75	V	—	—
CLKIN_VIL_EXTAL_BYPASS	Input clock low level in Bypass mode	0	—	vref-0.5	V	vref=0.5*VDD_HV_A	—
CLKIN_VIH_EXTAL_BYPASS	Input clock high level in Bypass mode	vref+0.5	—	VDD_HV_A	V	vref=0.5*VDD_HV_A	—
VSB	Self Bias Voltage	350	—	850	mV	—	—
GM	Amplifier Transconductance	9.7	—	18.5	mA/V	GM_SEL[3:0] = 4`b1111	—

1. For bypass mode applications, the EXTAL pin should be driven low when FXOSC is in off/disabled state.
2. The startup time specification is valid only when the recommended crystal and load capacitors are used. For higher load capacitances, the actual startup time might be higher.
3. The recommended gm setting to ensure extal swing < 2.75V at 8MHz in ALC-disabled mode is gm=4'b0010. Recommended gm settings in ALC-disabled mode for all other supported frequencies and crystals remain the same.

To ensure stable oscillations, FXOSC incorporates the feedback resistance internally.

Drive level is a crystal specification and if crystal load capacitance is increased beyond the recommended value, it may violate the crystal drive level rating. In such cases, contact NXP sales representative for selecting the correct crystal.

Crystal oscillator circuit provides stable oscillations when gmXOSC > 5 * gm_crit. The gm_crit is defined as:

$$gm\_crit = 4 * (ESR + RS) * (2\pi F)^2 * (C0 + CL)^2$$

where:

- gmXOSC is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- RS is the series resistance connected between XTAL pin and external crystal for current limitation
- F is the external crystal oscillation frequency
- C0 is the shunt capacitance of the external crystal
- CL is the external crystal total load capacitance. CL = Cs+ [C1*C2/(C1+C2)]
- Cs is stray or parasitic capacitance on the pin due to any PCB traces
- C1, C2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

Figure 21. Oscillation build-up equation

NOTE

To improve the FXOSC jitter & duty cycle performance, the functionality of the pin next to the Oscillator (namely, PTE14 in HDQFP172 and PTE3 in HDQFP100 package) must be limited to static GPIO operation.

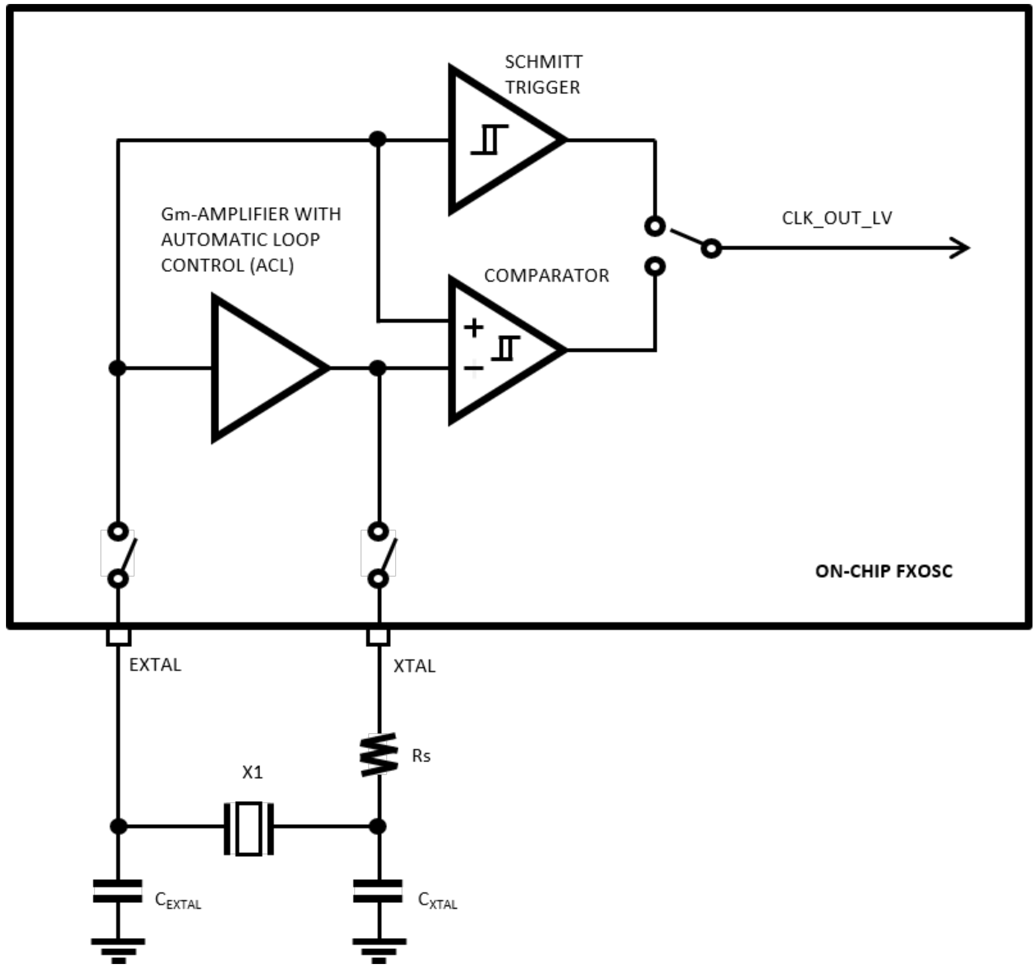

Figure 22. Block diagram

11.5 Slow Crystal Oscillator (SXOSC)

Table 37. Slow Crystal Oscillator (SXOSC)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Fsxosc	Oscillator Crystal Frequency [1]	—	32.768	—	KHz	IP in crystal mode	—
Tstart	SXOSC startup time	—	—	2	s	start up time is dependent upon board and crystal model.	—
ISXOSC	Oscillator Analog circuit supply current	—	2.1	10	uA	—	—
gm_sxocs	NMOS Amplifier Transconductance	3	—	40	u A/V	—	—

1. Supports single frequency

12 Communication interfaces

12.1 LPSPI

12.1.1 LPSPI

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following table provides timing characteristics for classic LPSPI timing modes.

1. All timing is shown with respect to 50% VDD_HV_A/B thresholds.

2. All measurements are with maximum output load of 30pF (except 50pF support on K3x8 with Fast/Medium/Standard-Plus IOs), input transition of 1 ns and pad configured DSE = 1, SRC = 0.

Table 38. LPSPI

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fperiph	Peripheral Frequency [1, 2, 3]	—	—	40	MHz	Master	—
fperiph	Peripheral Frequency [1, 2, 3]	—	—	40	MHz	Slave	—
fperiph	Peripheral Frequency [1, 3, 4]	—	—	80	MHz	Master Loopback	—
fop	Operating frequency	—	—	15	MHz	Slave	1
fop	Operating frequency	—	—	15	MHz	Master	1
fop	Operating frequency [5]	—	—	10	MHz	Slave_10Mbps	1
fop	Operating frequency [5]	—	—	10	MHz	Master_10Mbps	1
fop	Operating frequency [4, 6]	—	—	20	MHz	Master Loopback	1
tSPSCK	SPSCK period	66	—	—	ns	Slave	2
tSPSCK	SPSCK period	66	—	—	ns	Master	2
tSPSCK	SPSCK period [4]	50	—	—	ns	Master Loopback	2
tSPSCK	SPSCK period	100	—	—	ns	Master_10Mbps	—
tSPSCK	SPSCK period	100	—	—	ns	Slave_10Mbps	—
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	tSPCK/2	—	—	ns	Slave	3
tLEAD	Enable lead time (PCS to SPSCK delay) [7]	30	—	—	ns	Master	3
tLEAD	Enable lead time (PCS to SPSCK delay) [4, 7]	30	—	—	ns	Master Loopback	3

Table continues on the next page...

Table 38. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tLAG	Enable lag time (After SPSCK delay) [8]	tSPCK/2	—	—	ns	Slave	4
tLAG	Enable lag time (After SPSCK delay) [8]	30	—	—	ns	Master	4
tLAG	Enable lag time (After SPSCK delay) [4, 8]	30	—	—	ns	Master Loopback	4
tWSPCK	Clock (SPSCK) high or low time (SPSCK duty cycle) [9]	tSPSCK/ 2 - 3	—	tSPSCK/ 2 + 3	ns	Slave	5
tWSPCK	Clock (SPSCK) high or low time (SPSCK duty cycle) [9]	tSPSCK/ 2 - 3	—	tSPSCK/ 2 + 3	ns	Master	5
tWSPCK	Clock (SPSCK) high or low time (SPSCK duty cycle) [4, 9]	tSPSCK/ 2 - 3	—	tSPSCK/ 2 + 3	ns	Master Loopback	5
tSU	Data setup time(inputs)	6	—	—	ns	Slave	6
tSU	Data setup time(inputs)	25	—	—	ns	Master	6
tSU	Data setup time(inputs)	5	—	—	ns	Slave_10Mbps	6
tSU	Data setup time(inputs)	36	—	—	ns	Master_10Mbps	6
tSU	Data setup time(inputs) [4]	6	—	—	ns	Master_Loopback	6
tHO	Data hold time(inputs)	3	—	—	ns	Slave	7
tHO	Data hold time(inputs)	0	—	—	ns	Master	7
tHO	Data hold time(inputs)	4	—	—	ns	Slave_10Mbps	7
tHO	Data hold time(inputs)	0	—	—	ns	Master_10Mbps	7
tHO	Data hold time(inputs) [4]	3	—	—	ns	Master Loopback	7
tA	Slave access time	—	—	50	ns	Slave	8

Table continues on the next page...

Table 38. LPSPI (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tDIS	Slave MISO (SOUT) disable time	—	—	50	ns	Slave	9
tV	Data valid (after SPSCK edge)	—	—	26	ns	Slave	10
tV	Data valid (after SPSCK edge)	—	—	14	ns	Master	10
tV	Data valid (after SPSCK edge)	—	—	36	ns	Slave_10Mbps	10
tV	Data valid (after SPSCK edge)	—	—	21	ns	Master_10Mbps	10
tV	Data valid (after SPSCK edge) [4]	—	—	17.5	ns	Master Loopback	10
tHO	Data hold time (outputs)	3	—	—	ns	Slave	11
tHO	Data hold time (outputs)	-8	—	—	ns	Master	11
tHO	Data hold time (outputs)	3	—	—	ns	Slave_10Mbps	11
tHO	Data hold time (outputs)	-15	—	—	ns	Master_10Mbps	11
tHO	Data hold time (outputs) [4]	-2	—	—	ns	Master Loopback	11
tRI/FI	Rise/Fall time input	—	—	1	ns	Slave	12
tFI/RI	Rise/Fall time input	—	—	1	ns	Master	12
tFI/RI	Rise/Fall time input [4]	—	—	1	ns	Master Loopback	12

1. tperiph = 1/fperiph
2. For LPSPI0 instance, max. peripheral frequency is equal to AIPS_PLAT_CLK.
3. fperiph = LPSPI peripheral clock
4. Master Loopback mode: In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1.
5. These specifications apply to the SPI operation, as master or slave, at up to 10 Mbps for the combinations not indicated in the table below. Unless otherwise noted, all other 'master' and 'slave' specifications are also applicable in the 10Mbps configurations. See table "LPSPI 20 MHz and 15 MHz Combinations.
6. LPSPI0 support up to 20MHz on fast pin.
7. Minimum configuration value for CR[PCSSCK] field is 3(0x00000011).
8. Minimum configuration value for CCR[SCKPCS] field is 3(0x00000011).
9. While selecting odd dividers, ensure Duty Cycle is meeting this parameter.

fperiph = LPSPI peripheral clock

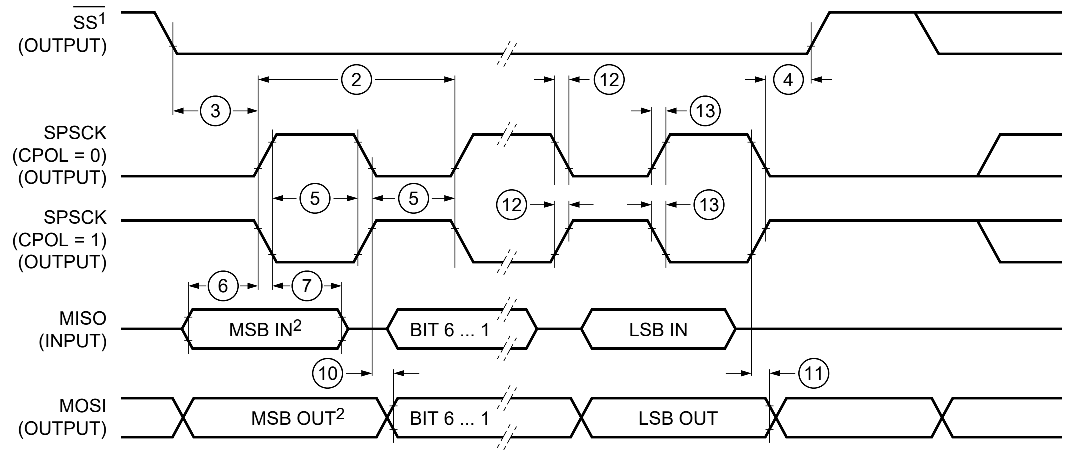

Figure 23. LPSPI Master Mode Timing (CPHA=0)

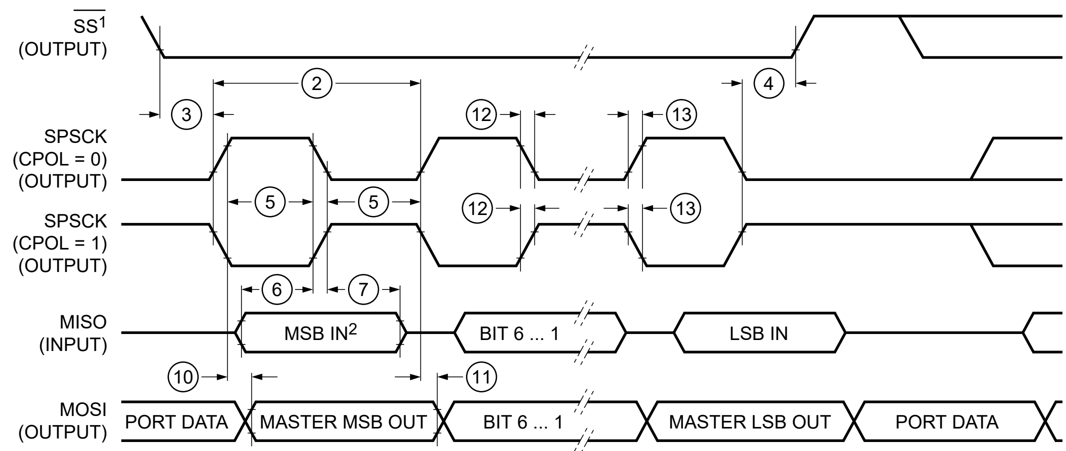

Figure 24. LPSPI Master Mode Timing (CPHA=1)

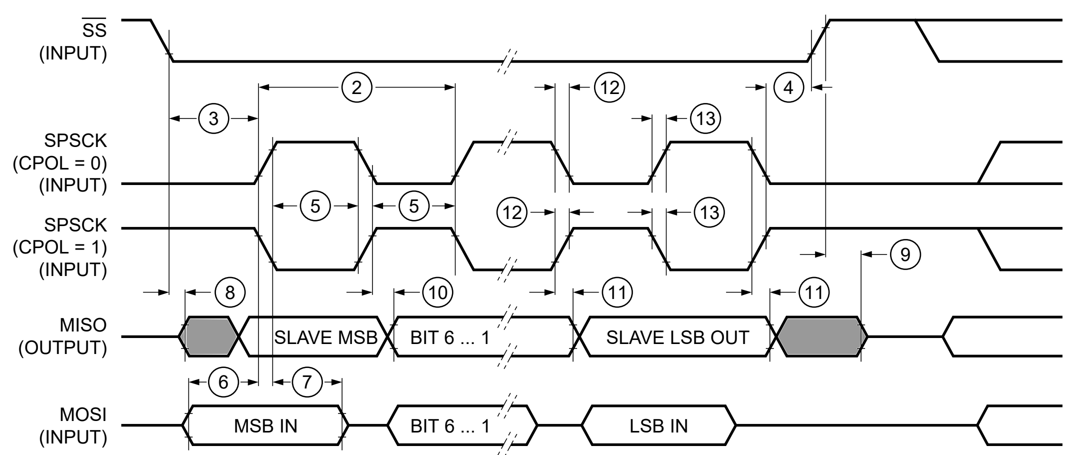

Figure 25. LPSPI Slave Mode Timing (CPHA=0)

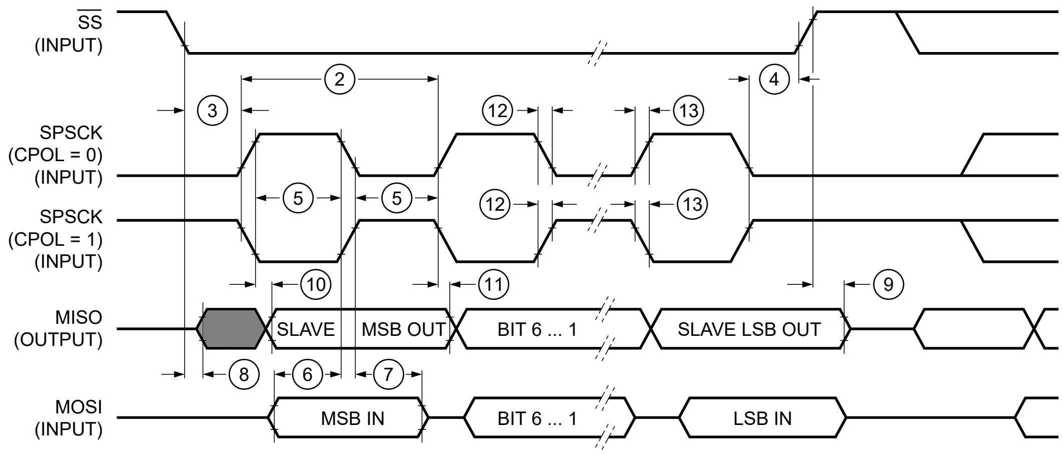

Figure 26. LPSPI Slave Mode Timing (CPHA=1)

12.1.2 LPSPI0 20 MHz and 15 MHz Combinations

NOTE

15 and 20 Mbps is supported on LPSPI0 only.

Table 39. LPSPI0 20 MHz and 15 MHz Combinations

PORT	PAD TYPE	SPI Signal	20Mbps (In loopback mode only)	15 Mbps
PTB1		LPSPI0_SOUT		LPSPI0_SOUT
PTB0		LPSPI0_PCS0		LPSPI0_PCS0
PTC9		LPSPI0_SIN		LPSPI0_SIN
PTC8		LPSPI0_SCK		LPSPI0_SCK
PTD6	GPIO-Medium	LPSPI0_PCS0	LPSPI0_PCS0	
PTD5	GPIO-Medium	LPSPI0_PCS1	LPSPI0_PCS1	
PTD12	GPIO-FAST	LPSPI0_SOUT	LPSPI0_SOUT	
PTD11	GPIO-FAST	LPSPI0_SCK	LPSPI0_SCK	
PTD10	GPIO-FAST	LPSPI0_SIN	LPSPI0_SIN	

NOTE

Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.

12.2 I^{2}C

See I/O parameters for I^{2}C specification.

"For supported baud rate see section 'Chip-specific LPI2C information' of the Reference Manual."

12.3 FlexCAN characteristics

See I/O parameters for FlexCAN specification.

"For supported baud rate, see section 'Protocol timing' of the Reference Manual."

12.4 SAI electrical specifications

12.4.1 SAI Electrical Characteristics, Slave Mode

The following table describes the SAI electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Table 40. SAI Electrical Characteristics, Slave Mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S13	SAI_BCLK cycle time (input)	80	—	—	ns	—	—
S14	SAI_BCLK pulse width high/low (input) [1]	45	—	55	%	—	—
S15	SAI_RXD input setup before SAI_BCLK	8	—	—	ns	—	—
S16	SAI_RXD input hold after SAI_BCLK	2	—	—	ns	—	—
S17	SAI_BCLK to SAI_TXD output valid	—	—	28	ns	—	—
S18	SAI_BCLK to SAI_TXD output invalid	0	—	—	ns	—	—
S19	SAI_FS input setup before SAI_BCLK	8	—	—	ns	—	—
S20	SAI_FS input hold after SAI_BCLK	2	—	—	ns	—	—
S21	SAI_BCLK to SAI_FS output valid	—	—	28	ns	—	—
S22	SAI_BCLK to SAI_FS output invalid	0	—	—	ns	—	—

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

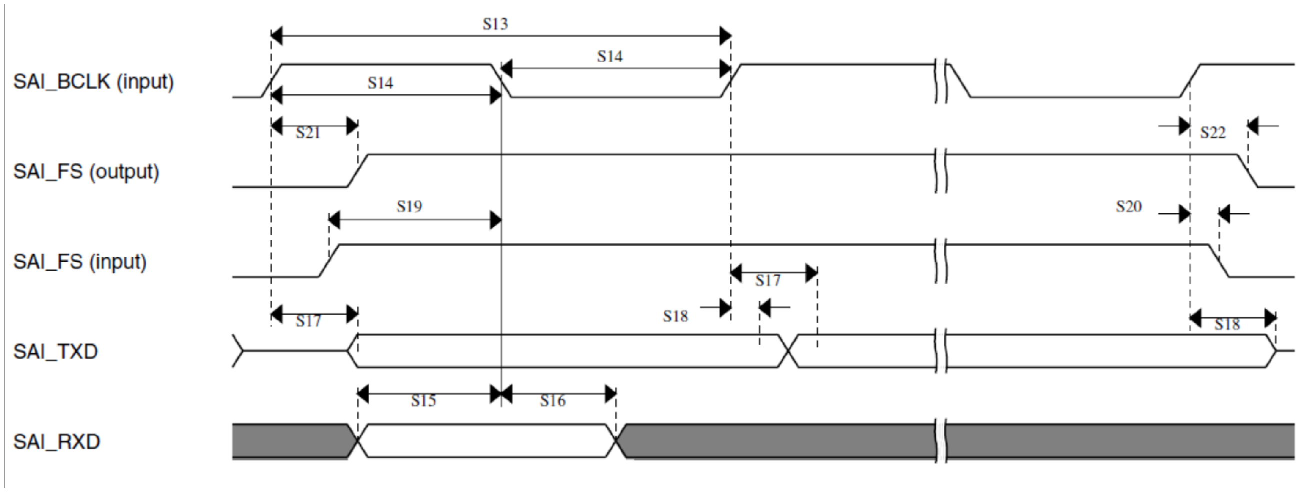

Figure 27. SAI slave mode

12.4.2 SAI Electrical Characteristics, Master Mode

The following table describes the SAI electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b 0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Table 41. SAI Electrical Characteristics, Master Mode

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SAI_MCLK cycle time	40	—	—	ns	—	—
S2	SAI_MCLK pulse width high/low	45	—	55	%	—	—
S3	SAI_BCLK cycle time	80	—	—	ns	—	—
S4	SAI_BCLK pulse width high/low	45	—	55	%	—	—
S5	SAI_RXD input setup before SAI_BCLK	28	—	—	ns	—	—
S6	SAI_RXD input hold after SAI_BCLK	0	—	—	ns	—	—
S7	SAI_BCLK to SAI_TXD output valid	—	—	8	ns	—	—
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	—	ns	—	—
S9	SAI_FS input setup before SAI_BCLK	28	—	—	ns	—	—

Table continues on the next page...

Table 41. SAI Electrical Characteristics, Master Mode (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S10	SAI_FS input hold after SAI_BCLK	0	—	—	ns	—	—
S11	SAI_BCLK to SAI_FS output valid	—	—	8	ns	—	—
S12	SAI_BCLK to SAI_FS output invalid	-2	—	—	ns	—	—

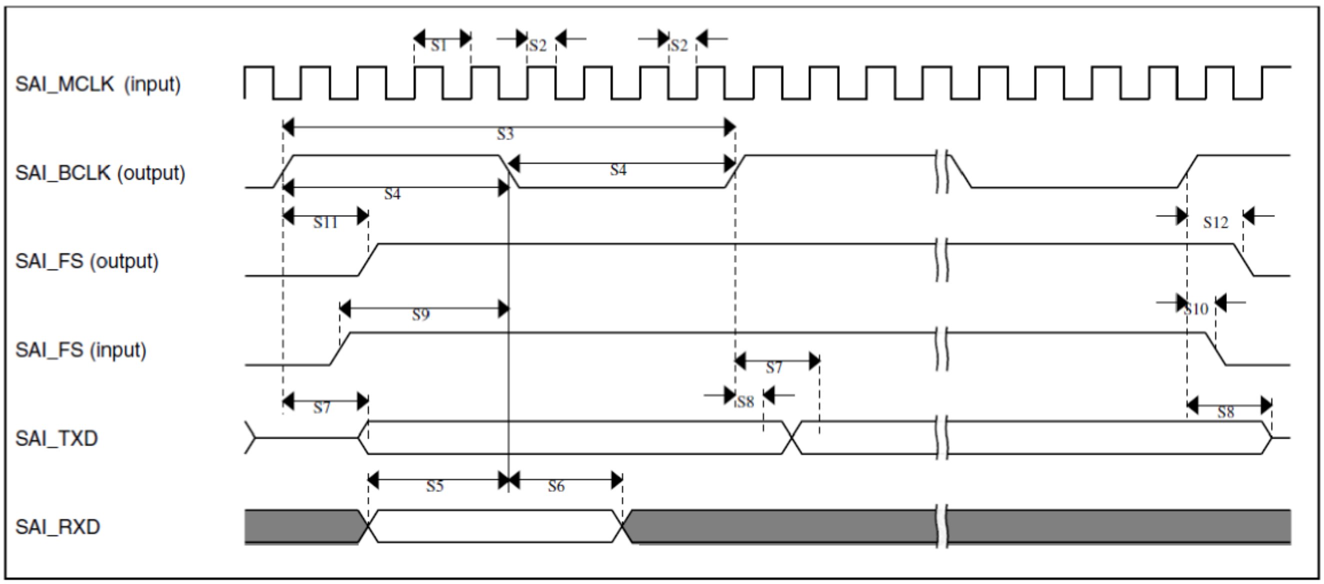

Figure 28. SAI master mode

12.5 Ethernet characteristics

12.5.1 Ethernet MII (10/100 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Table 42. Ethernet MII (100 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RXCLK frequency	—	2.5/25	—	MHz	10/100 Mbps	—
MII1	RXCLK pulse width high	35	—	65	%RXCLK period	—	—

Table continues on the next page...

Table 42. Ethernet MII (100 Mbps) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
MII2	RXCLK pulse width low	35	—	65	%RXCLK period	—	—
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	—	ns	10/100 Mbps	—
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	—	ns	10/100 Mbps	—
tCYC_TX	TXCLK frequency	—	2.5/25	—	MHz	10/100 Mbps	—
MII5	TXCLK pulse width high	35	—	65	%TXCLK period	—	—
MII6	TXCLK pulse width low	35	—	65	%TXCLK period	—	—
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	—	ns	—	—
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	—	25	ns	—	—

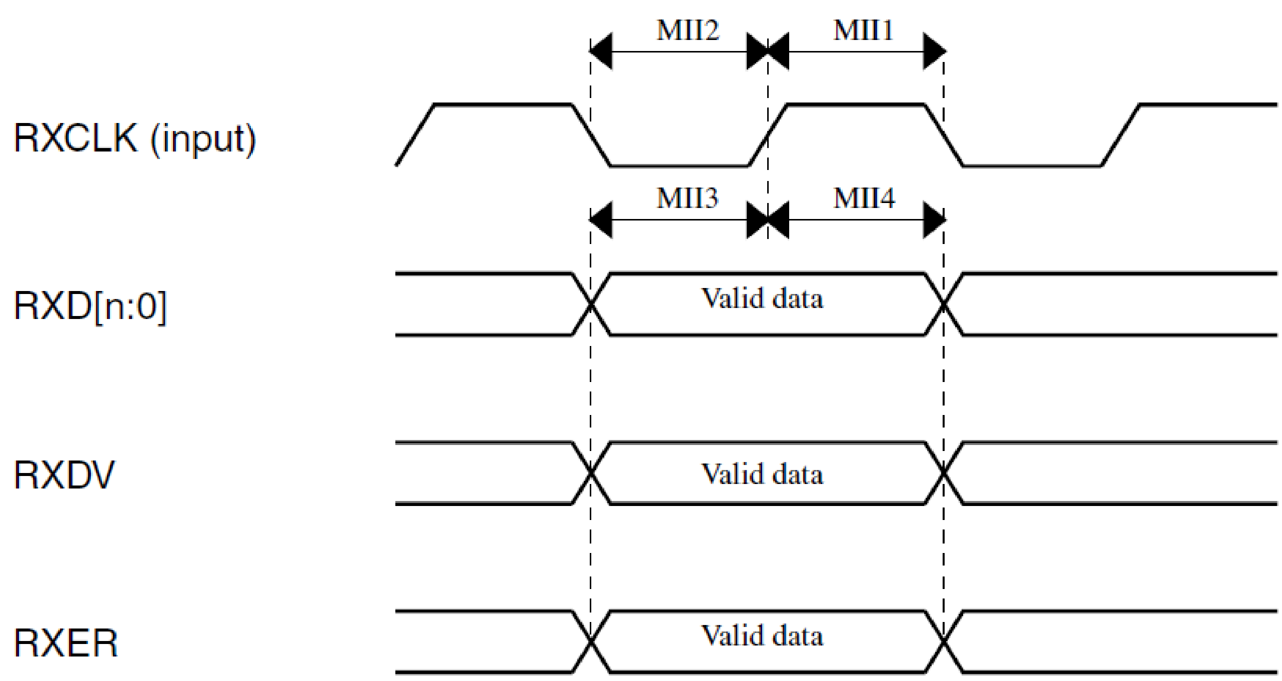

Figure 29. MII receive diagram

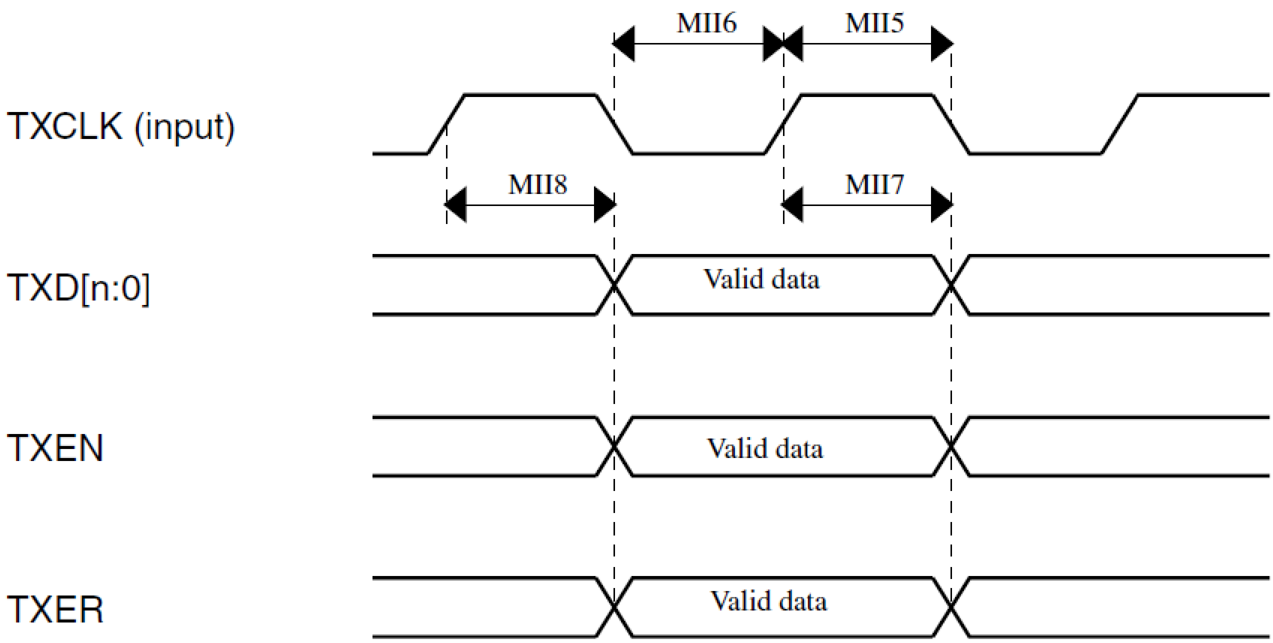

Figure 30. MII transmit diagram

12.5.2 Ethernet MII (200 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Table 43. Ethernet MII (200 Mbps)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RXCLK frequency	—	—	50	MHz	—	—
MII1	RXCLK pulse width high	35	—	65	% RXCLK period	—	—
MII2	RXCLK pulse width low	35	—	65	% RXCLK period	—	—
MII3	RXD[3:0], RXDV, RXER to RXCLK setup time	4	—	—	ns	—	—
MII4	RXCLK to RXD[3:0], RXDV, RXER hold time	2	—	—	ns	—	—
—	TXCLK frequency	—	—	50	MHz	—	—

Table continues on the next page...

Table 43. Ethernet MII (200 Mbps) (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
MII5	TXCLK pulse width high	35	—	65	% TXCLK period	—	—
MII6	TXCLK pulse width low	35	—	65	% TXCLK period	—	—
MII7	TXCLK to TXD[3:0], TXDV, TXER invalid	2	—	—	ns	—	—
MII8	TXCLK to TXD[3:0], TXDV, TXER valid	—	—	15	ns	—	—

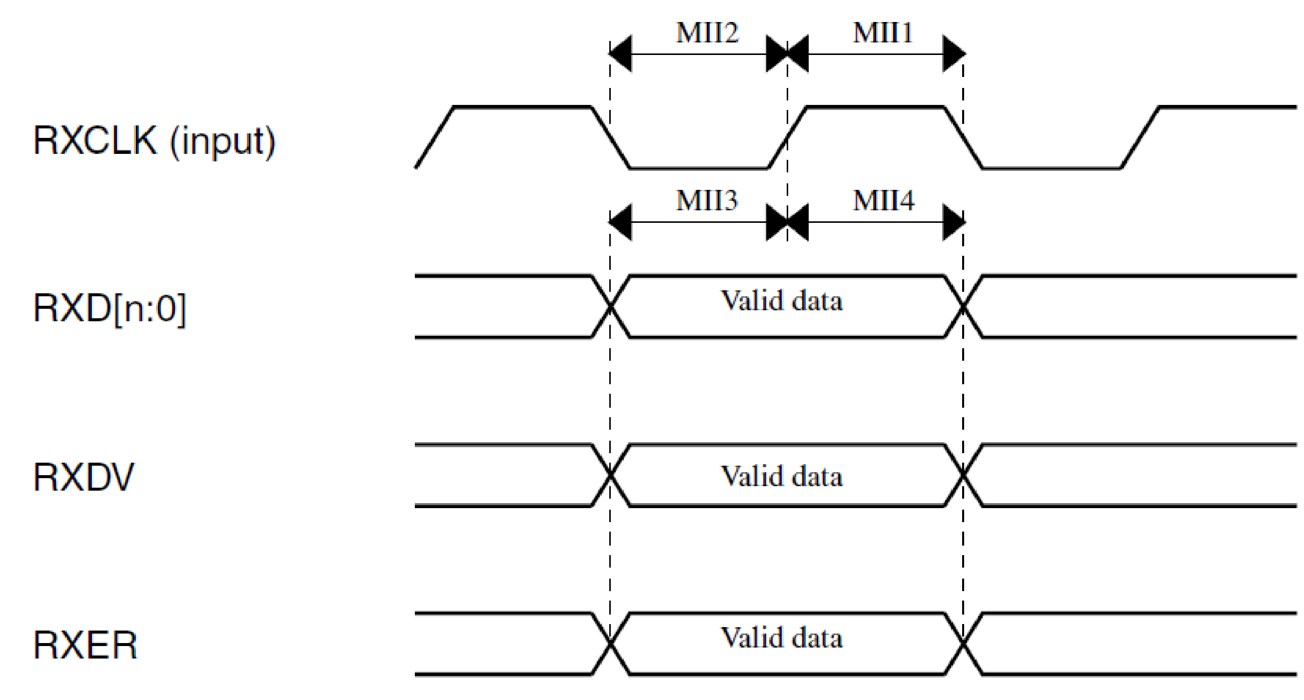

Figure 31. MII receive diagram

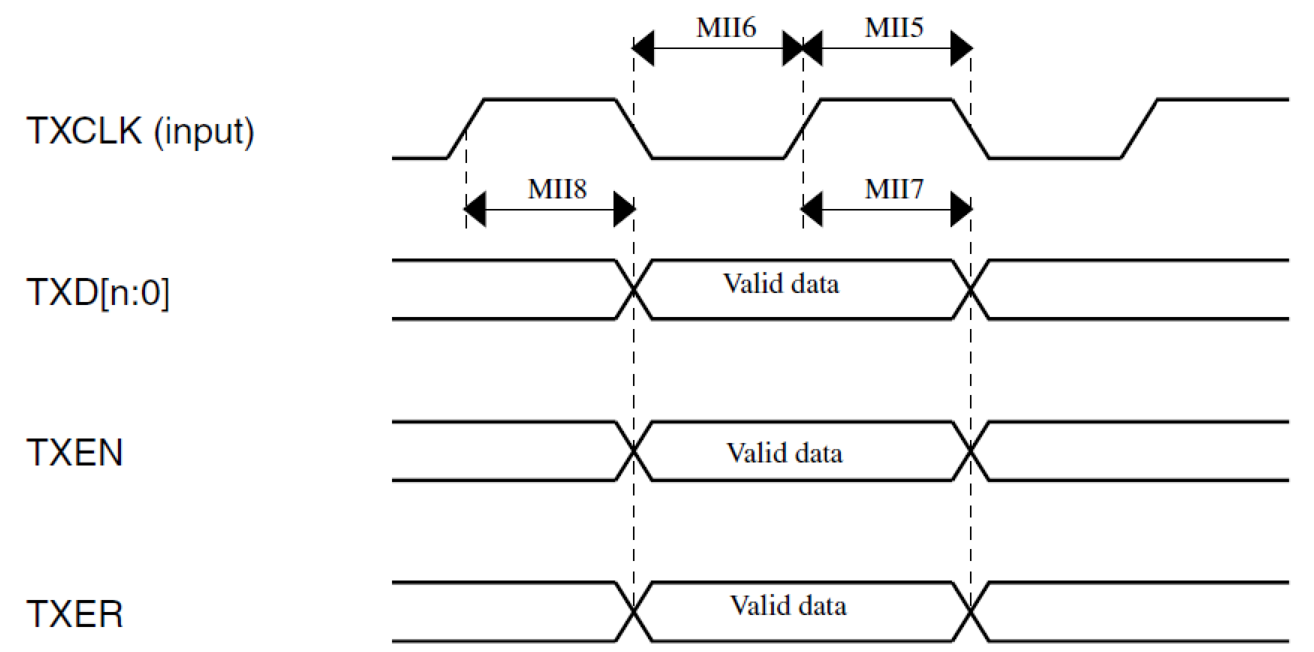

Figure 32. MII transmit diagram

12.5.3 Ethernet RMII (10/100 Mbps)

The following timing specs are defined at the device I/O pin and must be translated appropriately to arrive at timing specs/ constraints for the physical interface. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97 V to 3.63 V.

Table 44. Ethernet RMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	RMII input clock frequency (RMII_CLK)	—	—	50	MHz	10/100 Mbps	—
RMII1,RMII5	RMII_CLK pulse width high	35	—	65	%RMII_CLK period	—	—
RMII2,RMII6	RMII_CLK pulse width low	35	—	65	%RMII_CLK period	—	—
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	—	ns	—	—
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	—	ns	—	—
RMII8	RMII_CLK to TXD[1:0], TXEN data valid	—	—	15	ns	—	—

Table continues on the next page...

Table 44. Ethernet RMII (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
RMII7	RMII_CLK to TXD[1:0], TXEN data invalid	2	—	—	ns	—	—

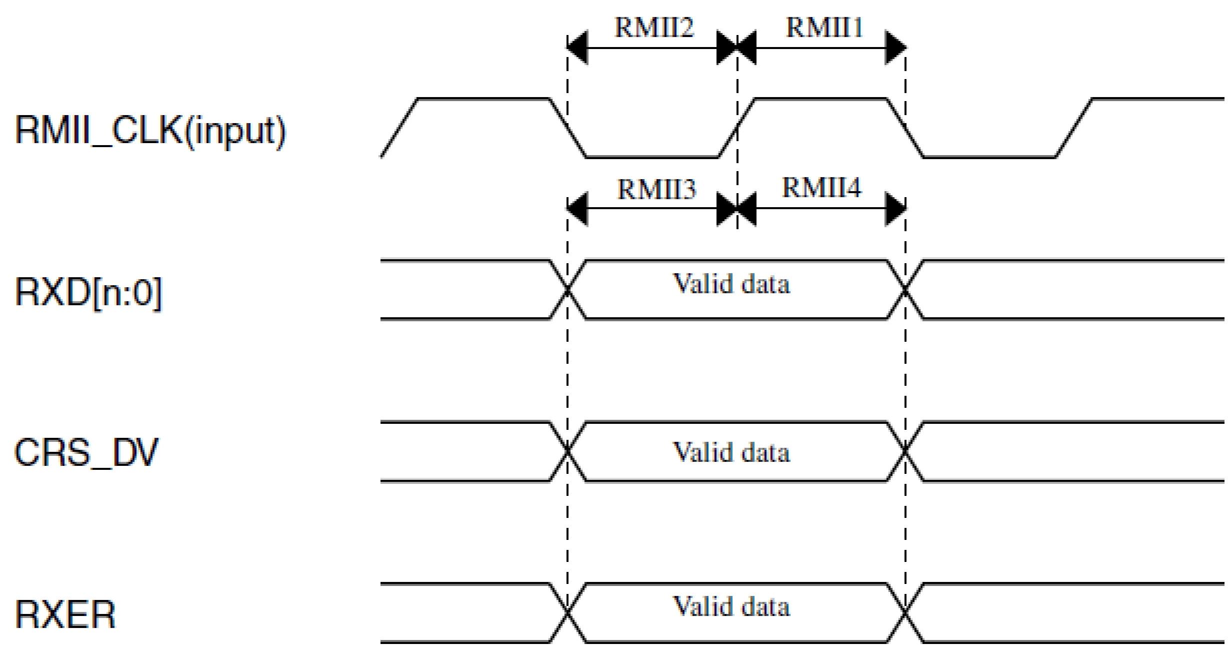

Figure 33. RMII receive diagram

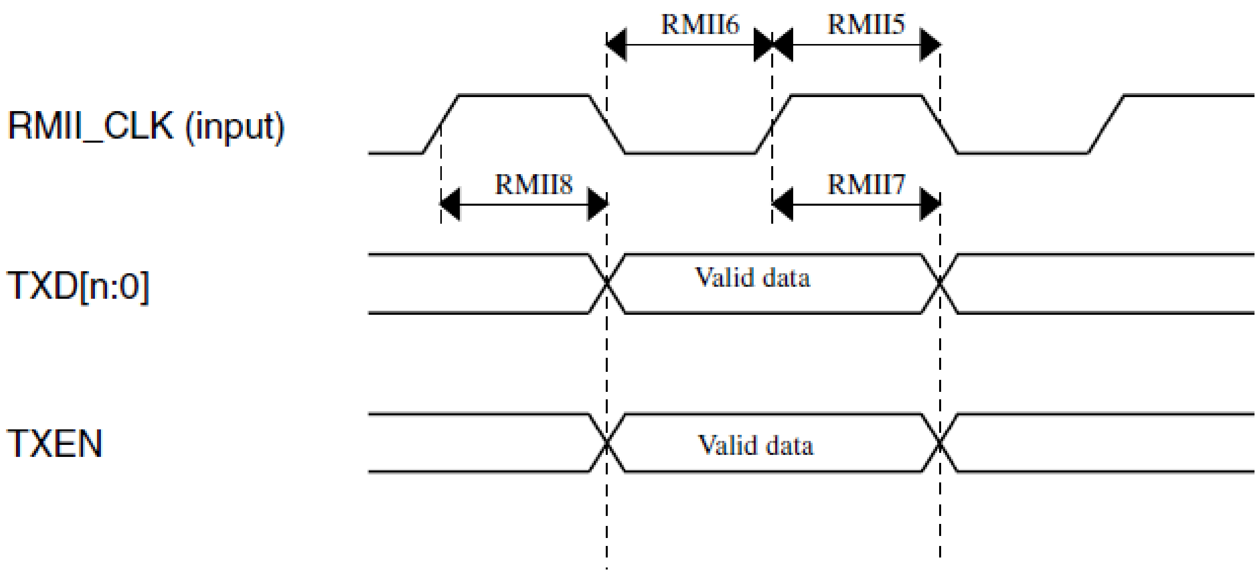

Figure 34. RMII transmit diagram

12.5.4 Ethernet RGMII

Table 45. Ethernet RGMII

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
Tcyc	Clock cycle duration [1, 2]	7.2	—	8.8	ns	SRC = 0	—
TskewT	Data to clock output skew (at transmitter) [2]	-500	—	500	ps	SRC=0	—
TskewRi	Data to clock input skew (at receiver) [2]	1	—	2.6	ns	SRC=0	—
TskewRo	Data to clock output skew (at receiver) [2]	-650	—	650	ps	SRC=0	—
Duty_G	Clock duty cycle for Gigabit [2]	45	—	55	%	SRC=0	—
Duty_T	Clock duty cycle for 10/100T [2]	40	—	60	%	SRC=0	—
Tr	Output rise time [3]	—	—	1	ns	SRC=0	—
Tf	Output fall time [3]	—	—	1	ns	SRC=0	—

1. For 10 Mbps and 100 Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.
2. RGMII timing specifications is valid for 3.3V nominal I/O pad supply voltage.
3. Output timing valid for maximum external load CL = 13.5pF, which is assumed to be a 5pF load at the end of a 50ohm, un-terminated, 2.5 inch microstrip trace on standard FR4 (1.5pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.”

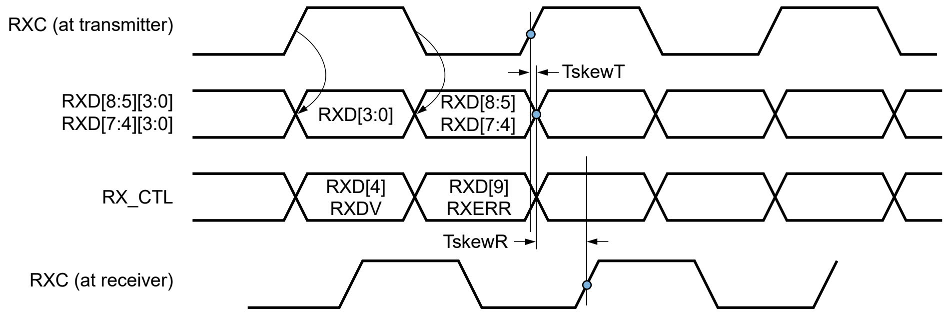

Figure 35. RGMII Receive Timing

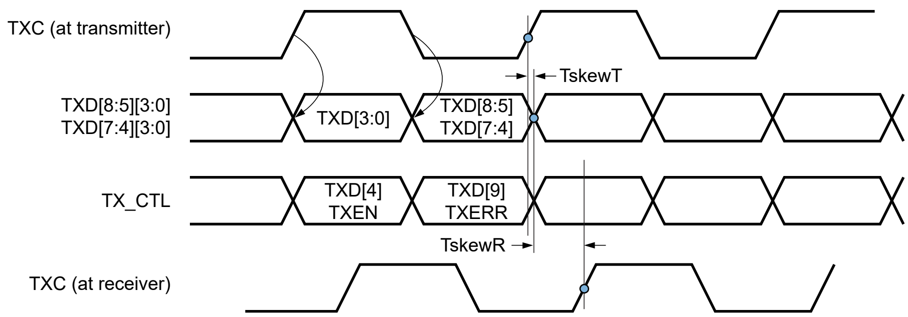

Figure 36. RGMII Transmit Timing

12.5.5 MDIO timing specifications

The following table describes the MDIO electrical characteristics. Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1 and SRE = 1’b0). I/O operating voltage ranges from 2.97 V to 3.63 V. MDIO pin must have external Pull-up.

Table 46. MDIO timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
—	MDC clock frequency	—	—	2.5	MHz	—	—
MDC1	MDC pulse width high	40	—	60	%MDC period	—	MDC1
MDC2	MDC pulse width low	40	—	60	%MDC period	—	MDC2
MDC5	MDC falling edge to MDIO output valid(maximum propagation delay)	—	—	25	ns	—	MDC5
MDC6	MDC falling edge to MDIO output invalid(minimum propagation delay)	-10	—	—	ns	—	MDC6

Table continues on the next page...

Table 46. MDIO timing specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
MDC3	MDIO (input) to MDC rising edge setup time	25	—	—	ns	—	MDC3
MDC4	MDIO (input) to MDC rising edge hold time	0	—	—	ns	—	MDC4

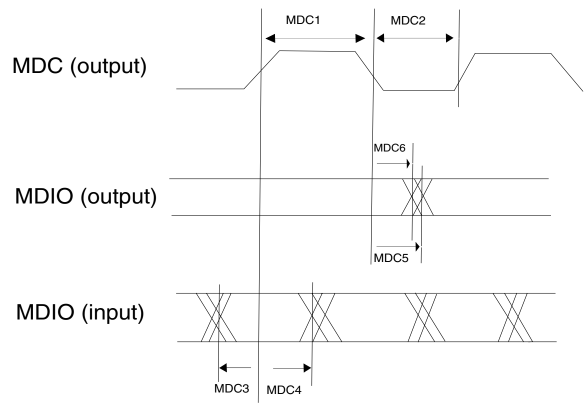

Figure 37. MII/RMII serial management channel timing

12.6 QuadSPI

12.6.1 QuadSPI Quad 3.3V SDR 120MHz

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Program register value QuadSPI_FLSHCR[TCSS] = 4`h3.

Program register value QuadSPI_FLSHCR[TCSH] = 4`h3.

Program register value QuadSPI_DLLCRA[SLV_FINE_OFFSET] to 4'b0001.

Table 47. QuadSPI Quad 3.3V SDR 120MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK	SCK clock frequency [1]	—	—	120	MHz	Pad Loopback	—
fSCK	SCK clock frequency [1]	—	—	60	MHz	Internal Loopback	—

Table continues on the next page...

Table 47. QuadSPI Quad 3.3V SDR 120MHz (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tSCK	SCK clock period	1/fSCK	—	—	ns	Pad Loopback	—
tSCK	SCK clock period	1/fSCK	—	—	ns	Internal Loopback	—
tSDC	SCK duty cycle	45	—	55	%	Internal Loopback	—
tSDC	SCK duty cycle	45	—	55	%	Pad Loopback	—
tIS	Data input setup time	1.75	—	—	ns	Pad Loopback	—
tIS	Data input setup time	9	—	—	ns	Internal Loopback	—
tIH	Data input hold time	1	—	—	ns	Pad Loopback	—
tIH	Data input hold time	1	—	—	ns	Internal Loopback	—
tOV	Data output valid time	—	—	1.75	ns	Pad Loopback	—
tOV	Data output valid time	—	—	1.75	ns	Internal Loopback	—
tIV	Data output invalid time	-1.5	—	—	ns	Pad Loopback	—
tIV	Data output invalid time	-1.5	—	—	ns	Internal Loopback	—
tCSSCK	CS to SCK time	5	—	—	ns	Pad Loopback	—
tCSSCK	CS to SCK time	5	—	—	ns	Internal Loopback	—
tSCKCS	SCK to CS time	3	—	—	ns	Pad Loopback	—
tSCKCS	SCK to CS time	3	—	—	ns	Internal Loopback	—

1. This frequency specification is valid only if output valid time of external flash is ≤ 5.5ns, and if output valid time of external flash is more than 5.5ns but ≤ 6.5ns, then maximum fSCK is 104MHz.

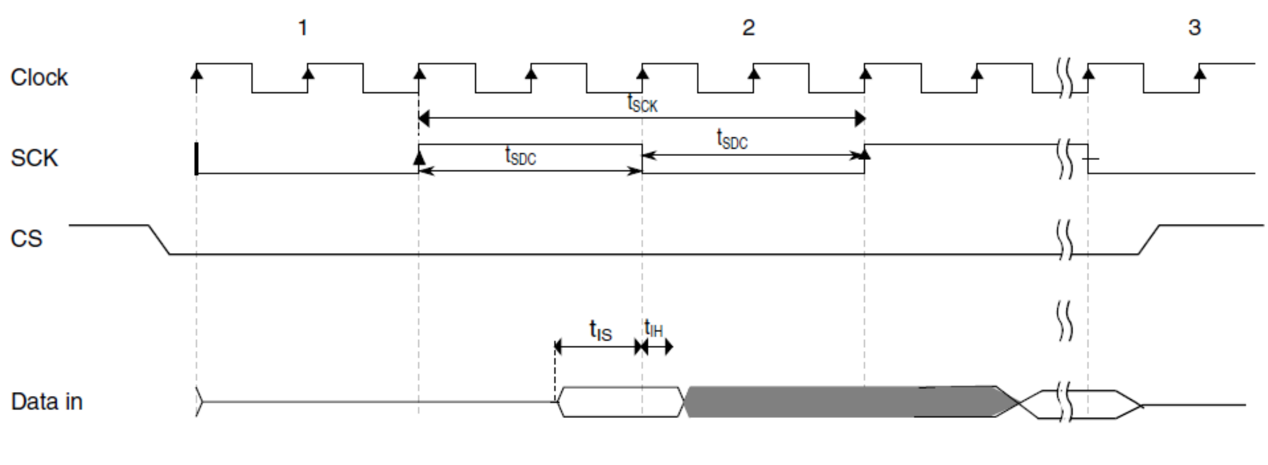

Figure 38. QuadSPI input timing (SDR mode)

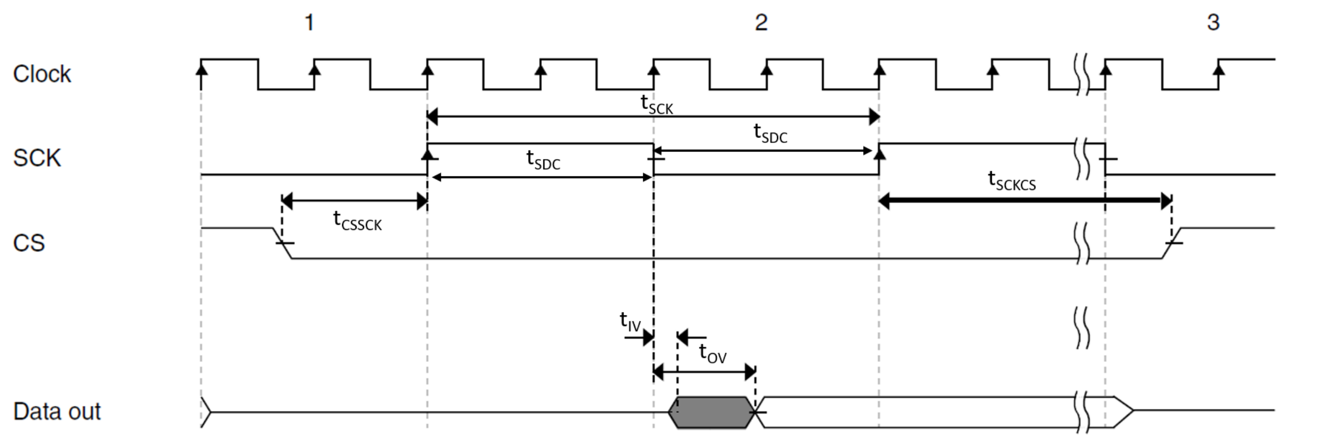

Figure 39. QuadSPI output timing (SDR mode)

12.6.2 QuadSPI Octal 3.3V DDR 100MHz

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn't have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Set FLSHCR[TCSS]=2 and FLSHCR[TCSH]=5.

Table 48. QuadSPI Octal 3.3V DDR 100MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1]	—	—	100	MHz	—	—
tSDC	SCK duty cycle	45	—	55	%	—	—
tCL_SCK_DQS	SCK / DQS low time [1]	4.500	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1]	4.500	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	1.016	—	3.484	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK) [2]	3.016 - n/ fSCK	—	-0.016 + m/fSCK	ns	—	—
tDVW	Input data valid window [1]	3.284	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.816	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.684	—	—	ns	—	—

1. Input timing assumes maximum input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.
2. Where m=TCSS and n=TCSH-1.

12.6.3 QuadSPI Octal 3.3V DDR 120MHz

The following table describes the QuadSPI electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pads configured with DSE = 1'b1 and SRE = 1'b0. I/O operating voltage ranges from 2.97V to 3.63V. QuadSPI trace length should be less than or equal to 2 inches. For Single and Dual IO modes of operation if external device doesn’t have pull-up feature, then external pull-up must be added at board level for unused device pins. With external pull-up, performance of the interface may degrade in Quad IO mode based on load associated with external pull-up. QuadSPI support delay chain upto length 16, wherein delay length of low-frequency segment is 16 and length of high-frequency segment is 0. See the device Reference Manual for register and bit descriptions.

Set FLSHCR[TCSS]=2 and FLSHCR[TCSH]=5.

Table 49. QuadSPI Octal 3.3V DDR 120MHz

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fSCK_DQS	SCK / DQS frequency [1]	—	—	120	MHz	DLL and Auto-Learning mode enabled	—
fSCK_DQS	SCK / DQS frequency [1]	—	—	120	MHz	DLL mode enabled	—
tSCK	SCK clock period	1/ fSCK_DQS	—	—	ns	External DQS	—
tSDC	SCK / DQS duty cycle	45	—	55	%	External DQS	—
tCL_SCK_DQS	SCK / DQS low time [1]	3.75	—	—	ns	—	—
tCH_SCK_DQS	SCK / DQS high time [1]	3.75	—	—	ns	—	—
tOD_DATA	Data output delay (w.r.t. SCK)	0.816	—	2.934	ns	—	—
tOD_CS	CS output delay (w.r.t. SCK)	3.016	—	-0.766	ns	—	—
tDVW	Input data valid window [1]	2.518	—	—	ns	—	—
tISU_DQS	Input setup time (w.r.t. DQS) [1]	-0.616	—	—	ns	—	—
tIH_DQS	Input hold time (w.r.t. DQS) [1]	3.134	—	—	ns	—	—

1. Input timing assumes an input signal transition of 1 ns (20%/80%). DQS denotes external strobe provided by the Flash.

12.7 LPUART specifications

See I/O parameters for LPUART specifications.

13 Debug modules

13.1 Debug trace timing specifications

The following table describes the Debug trace electrical characteristics. Measurements are with maximum output load of 25pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 50. Debug trace timing specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
fTRACE	Trace clock frequency (trace on Fast pads)	—	—	120	MHz	—	—
fTRACE	Trace clock frequency (trace on StandardPlus pads)	—	—	25	MHz	—	—
tDVW	Data output valid window	1.2	—	—	ns	—	—
tDIV	Data output invalid	0.3	—	—	ns	—	—

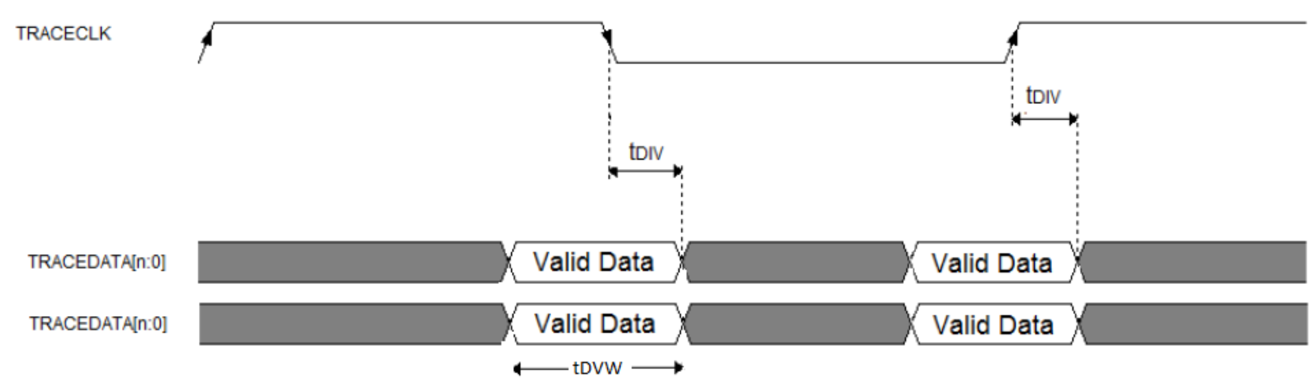

Figure 40. Trace CLKOUT specifications

13.2 SWD electrical specifications

The following table describes the SWD electrical characteristics. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 51. SWD electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S1	SWD_CLK frequency	—	—	33	MHz	—	S1
S2	SWD_CLK cycle period	1 / S1	—	—	ns	—	S2

Table continues on the next page...

Table 51. SWD electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
S3	SWD_CLK pulse width	40	—	60	%	—	S3
S4	SWD_CLK rise and fall times	—	—	1	ns	—	S4
S9	SWD_DIO input data setup time to SWD_CLK rise	5	—	—	ns	—	S9
S10	SWD_DIO input data hold time after SWD_CLK rising edge	5	—	—	ns	—	S10
S11	SWD_CLK high to SWD_DIO output data valid	—	—	22	ns	—	S11
S12	SWD_CLK high to SWD_DIO output data hi-Z	—	—	22	ns	—	S12
S13	SWD_CLK high to SWD_DIO output data invalid	0	—	—	ns	—	S13

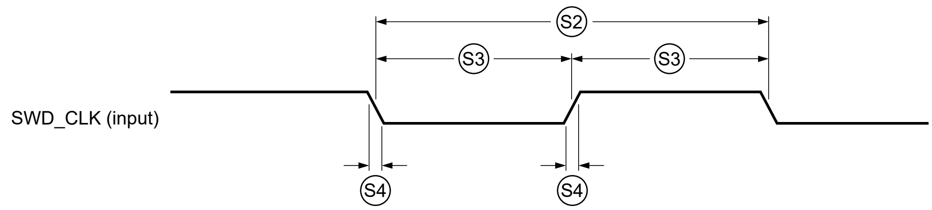

Figure 41. SWD Input Clock Timing

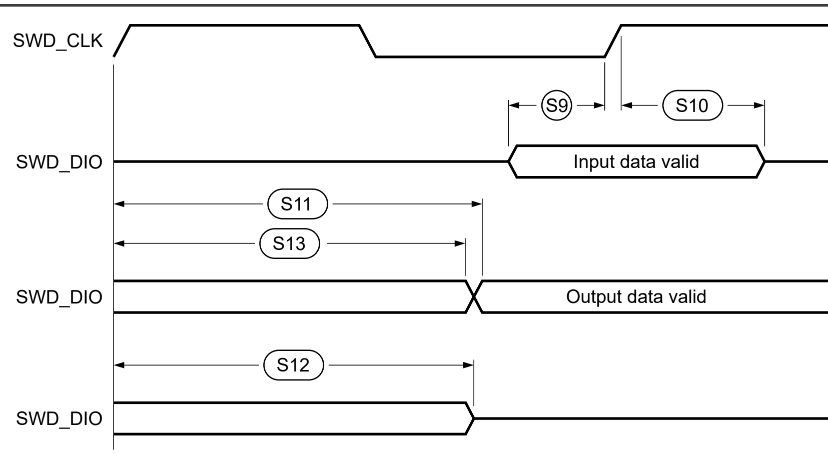

Figure 42. SWD Output Data Timing

13.3 JTAG electrical specifications

The following table describes the JTAG electrical characteristics. These specifications apply to JTAG and boundary scan. Measurements are with maximum output load of 30pF, input transition of 1ns and pad configured with DSE = 1'b1 and SRE = 1'b0.

Table 52. JTAG electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition	Spec Number
tJCYC	TCK cycle time [1, 2]	30	—	—	ns	—	1
tJDC	TCK clock pulse width	40	—	60	%	—	2
tTCKRISE	TCK rise/fall times (40%-70%)	—	—	1	ns	—	3
tTMSS, tTDIS	TMS, TDI data setup time	5	—	—	ns	—	4
tTMSH, tTDIH	TMS, TDI data hold time	5	—	—	ns	—	5
tTDOV	TCK low to TDO data valid [3]	—	—	22	ns	—	6
tTDOI	TCK low to TDO data invalid	0	—	—	ns	—	7
tTDOHZ	TCK low to TDO high impedance	—	—	22	ns	—	8
tBSDV	TCK falling edge to output valid [4]	—	—	600	ns	—	11
tBSDVZ	TCK falling edge to output valid out of high impedance	—	—	600	ns	—	12
tBSDHZ	TCK falling edge to output high impedance	—	—	600	ns	—	13
tBSDST	Boundary scan input valid to TCK rising edge	15	—	—	ns	—	14
tBSDHT	TCK rising edge to boundary scan input invalid	15	—	—	ns	—	15

1. Cycle time is 30ns assuming full cycle timing. Cycle time is 60ns assuming half cycle timing.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

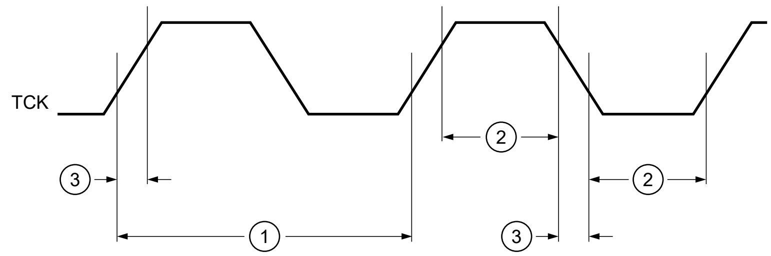

Figure 43. JTAG TCK Input Timing

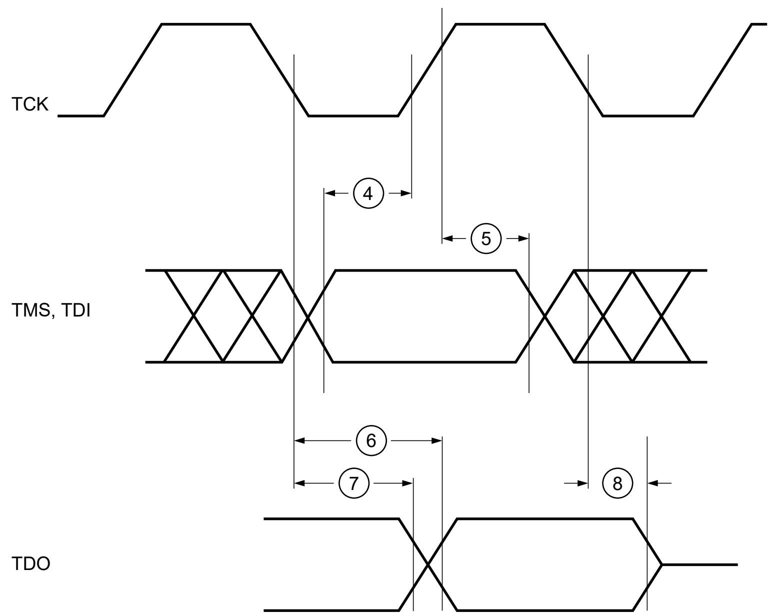

Figure 44. JTAG Test Access Port Timing

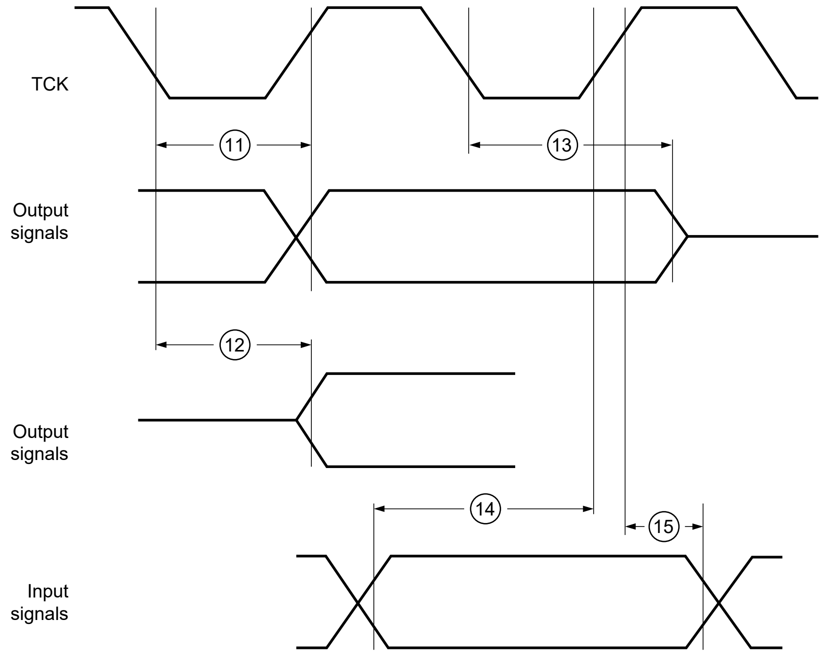

Figure 45. Boundary Scan Timing

14 Thermal Attributes

14.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

14.2 Thermal characteristics

Junction temperature of the device does not solely depend on package thermal resistance but is also a function of chip power dissipation, PCB attributes, environmental conditions (ambient temperature and air flow) and cumulative effects of other heat generating ICs on the PCB.

The appropriate thermal design must be carried out on package so that it can safely dissipate the necessary amount of power needed for it to function properly without exceeding the maximum junction temperature. This may involve adding a cooling solution on the package, creating thermal enhancements on the PCB and improving environmental conditions. The customer is encouraged to use the package model to perform design and risk assessment through simulations. Package models in FloTHERM or Icepak formats can be obtained under NDA from the sales team.

Thermal Ratings

The table below is the package thermal ratings for LQFP, HDQFP package variants. These numbers are derived through simulations based on standardized tests as described in the footnotes.

Table 53. Thermal characteristics

Rating	Conditions	Symbol	Package	Device				Unit
				MWCT2015S MWCT2014S	MWCT2016S	MWCT2D16S	MWCT2D17S	
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Four-layer board (2s2p)[2]	$R_{\Theta JA}$	48-LQFP	45	NA	NA	NA	°C/W
			100-HDQFP	35.3	38	33.8	NA	°C/W
			172-HDQFP	NA	30.5	29.6	28.9	°C/W
Thermal characterization parameter, Junction-to-Top of package[1]	Natural Convection	Ψ_{JT}	48-LQFP	2	NA	NA	NA	°C/W
			100-HDQFP	0.66	0.8	0.5	NA	°C/W
			172-HDQFP	NA	0.5	0.5	0.4	°C/W

1. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
2. Thermal test board meets JEDEC specification for this package (JESD51-9).

15 Dimensions

15.1 Obtaining package dimensions

Package dimensions are provided in the package drawings. To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
48-pin LQFP	98ASH00962A
172-pin HDQFP	98ASA01107D
100-pin HDQFP	98ASA01570D

16 Revision history

The following table lists the changes in this document.

Table 54. Revision history

Document ID	Release date	Description
MWCT2xxxS v.4.0	12 September 2024	• Deleted bullet "Up to two Synchronous Audio Interface (SAI) modules" from Communications interfaces. • Updated first bullet of Reliability, safety and security. • In Overview section changed ASIL-B and D to ASIL-B. • In Overview section deleted the Caution. • In Block diagram section updated Figure 1, Figure 2, Figure 3, Figure 4, and Figure 5. • In section Thermal operating characteristics- Updated Table Thermal operating characteristics. • In section Boot time, HSE firmware not installed- Updated Condition in Table Boot time, HSE firmware not installed. • In section Boot time, HSE firmware installed- Updated Condition in Table Boot time, HSE firmware installed. • In section HSE firmware memory verification time examples- UpdatedI Table HSE firmware memory verification time examples. • In section Supply Monitoring- In table Supply Monitoring- Updated description of HVD_V15 Symbol. • In section V15 regulator (BJT option, NPN ballast transistor control) electrical specifications- Updated Table V15 regulator (BJT option, NPN ballast transistor control) electrical specifications. Updated Figure Ballast circuit. • In section Supply currents- Updated Table STANDBY mode supply currents, Table- Low speed RUN mode supply currents, Table- RUN mode supply currents, and Table- Example RUN mode configuration supply currents.

Table continues on the next page...

Table 54. Revision history

Document ID	Release date	Description
		• In section Operating mode- Updated Table- RUN mode configuration options. • In section GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V)- Updated Table- GPIO DC electrical specifications, 3.3V Range (2.97V - 3.63V). • In section GPIO DC electrical specifications, 5.0V (4.5V - 5.5V)- Updated Table GPIO DC electrical specifications, 5.0V (4.5V - 5.5V), Updated Figure 14. Reference Load Diagram. • In section 5.0V (4.5V - 5.5V) GPIO Output AC Specification- Updated Table- 5.0V (4.5V - 5.5V) GPIO Output AC Specification. • In section 3.3V (2.97V - 3.63V) GPIO Output AC Specification- Updated Table- 3.3V (2.97V - 3.63V) GPIO Output AC Specification. • In section Flash memory read timing parameters- Updated the title of Table from "Flash Read Wait State Settings (MWCT2015S, MWCT2016S, MWCT2D16S, and MWCT2D17S)" to "Flash Read Wait State Settings (MWCT2014S, MWCT2015S, MWCT2016S, MWCT2D16S, and MWCT2D17S)". • Updated section SAR ADC. Added a footnote in Table- SAR ADC • In section PLL- In Table- PLL- Updated the Min. value of FPLL_out. • In section Fast External Oscillator (FXOSC)- Updated Table- Fast External Oscillator (FXOSC). • In section Slow Crystal Oscillator (SXOSC)- Updated Max value of ISXOSC in Table- Slow Crystal Oscillator (SXOSC). • Updated section LPSPI. • Updated the title of section from "Ethernet MII (100 Mbps)" to "Ethernet MII (10/100 Mbps)". Also, updated the Table- Ethernet MII (100 Mbps). • Updated the title of section from "Ethernet RMII" to "Ethernet RMII (10/100 Mbps)". Also, updated the Table- Ethernet RMII. • Updated the section Thermal characteristics. • In section Obtaining package dimensions- Updated the Document number of 172-pin HDQFP and 100-pin HDQFP.

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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