MCXA156, A155, A154, A146, A145, A144 Data Sheet

Arm® Cortex®-M33 48MHz or 96MHz 32-bit MCU, up to 1MB Flash

Rev. 5 — July 2024

Data Sheet: Technical Data

MCXA14x
MCXA15x

LQFP100	LFBGA64	VFBGA112
14 x 14 x 1.4 mm, 0.5mm	5 x 5 x 1.2 mm,0.5mm	7 x 7x 0.86mm, 0.5mm

Features

- Arm Cortex-M33 48MHz(A14x) or 96MHz(A15x) with 396 CoreMark (4.12 CoreMark/MHz)
- Up to 1MB Flash, 128KB SRAM, up to 8 KB SRAM with ECC
- All RAM can be retained down to Deep Power Down mode
- -40 °C to 125 °C temperature range
- Down to 64 µA/MHz Active current, 32.26 µA Deep Sleep current, 8.2 µA Power Down current, 412 nA Deep Power Down current

Core

- Arm 32-bit Cortex-M33 CPU, with FPU and DSP extension instruction set, no TrustZone, no MPU

Memories

- Single-bank Flash: Up to 1024 KB Flash with ECC (support one bit correction and two bits detection)
- Cache Engine with 4 KB RAM
- Up to 128 KB RAM, configurable as up to 8KB RAM with ECC (support one bit correction and two bits detection)
- All RAM can be retained down to Deep Power Down mode
- 16 KB ROM

Security

- 128-bit Universal Unique Identifier (UUID) per device in accordance with IETF's RFC4122 version5 specification
- Device lifecycle management
- Flash read/write/execute permission protect by MBC and lockable
- Implicit-protected Flash Region (IFR)
- Security Monitoring:
  - Code Watchdog for code flow integrity checking
  - GLIKEY enhances protection against attacks to gain unauthorized access to sensitive registers

Low-Power Performance

- **Active**
  - 64 µA/MHz in Active Mode (executing while(1) from flash, 3.3 V@25 °C)
- **Deep Sleep**
  - 32.26 µA, 7.1 µs wake-up (3.3 V@25 °C)
- **Power Down**
  - 8.2 µA, 16.6 µs wake-up (RAM X0/X1 and RAM A0 retained, 3.3 V@25 °C)

Deep Power Down

- 412 nA, 1.44 ms wake-up (wake timer disabled, reset pin enabled, all SRAM off, 3.3 V@25 °C)

System and Clocks

- 192 MHz free-running oscillator (FRO192M)
- 12 MHz free-running oscillator (FRO12M)
- 16 KHz free-running oscillator (FRO16K)
- Up to 50 MHz crystal oscillator
- Hardware and Software Watchdogs
- Asynchronous DMA modules (8-channels)

Communication Interfaces for Connectivity

- 4x LPI2C, 2x LPSPI, 5x LPUART
- 1x I3C
- USB Full-speed (Device) with on-chip FS PHY
- 1x FlexCAN with FD
- FlexIO

Advanced Motor Control

- Up to 2x FlexPWM each with 3 sub-modules, providing 12 complementary outputs of PWM (no Nanoedge module)
- Up to 2x Quadrature Decoder (eQDC)
- 2x AOI (AND/OR/Invert) module support up to 4 output trigger

Analog

- 2x 16-bit ADC
  - Up to 3.2 Msps in 16-bit mode, and 4 Msps in 12-bit
  - Up to 32 ADC Input channels (depending on the package)
  - One integrated temperature sensor per ADC
- 1x 12-bit DAC
- Two Low power Comparators (LPCMP) with 8 input pins and 8-bit DAC as internal reference
  - 1x LPCMP is functional down to Deep Power Down mode
- 1x OpAmp with PGA

Timers

- Five 32-bit standard general-purpose asynchronous timers/counters, which support up to four capture inputs and four compare outputs, PWM mode, and external count input. Specific timer events can be selected to generate DMA requests.
- Low power timer
- Frequency measurement timer
- Windowed watchdog timer
- Wake timer
- Micro-tick timer (UTICK)
- OS event timer

General-purpose input/output

- Up to 82 GPIOs
- Up to eight 20 mA IO
- 50 MHz IO on P1, P3 and P4
- Up to 19-pin wake-up sources function down to Deep Power Down mode
- Support 1.71 V~3.6 V IO supply range
- Support 1.2V independent IO supply on P3 port

Power Management

- Integrated voltage regulator
  - Core LDO, other LDOs
- Operating range: 1.71 V to 3.6 V
- IOs: 1.71 V-3.6 V full-performance

Target Applications

Industrial

- Energy Storage and Management System
- Smart Metering
- Factory Automation
- Industrial HMI
- Mobile Robotics Ecosystem
- Motion Control and Robotics
- Motor Drives
- Brushless DC Motor (BLDC) Control
- Permanent Magnet Synchronous Motor (PMSM)

Smart Home

- Home Control Panel
- Major Home Appliances
- Robotic Appliance
- Smart Speaker
- Soundbar
- Gaming Accessories
- Smart Lighting
- Smart Power Socket and Light Switch

Table 1. Ordering Information

Part Number	Marking	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIOs	Pin Count	Package	Packing
MCXA144VLL	MCXA144VLL	48	256	64	81	100	LQFP	Tray
MCXA144VMP	MCXA144VMP	48	256	64	50	64	LFBGA	Tray

Table continues on the next page...

Table 1. Ordering Information (continued)

Part Number	Marking	Core Speed (MHz)	Flash (KB)	SRAM (KB)	GPIOs	Pin Count	Package	Packing
MCXA144VPJ	MCXA144VPJ	48	256	64	82	112	VFBGA	Tray
MCXA145VLL	MCXA145VLL	48	512	96	81	100	LQFP	Tray
MCXA145VMP	MCXA145VMP	48	512	96	50	64	LFBGA	Tray
MCXA145VPJ	MCXA145VPJ	48	512	96	82	112	VFBGA	Tray
MCXA146VLL	MCXA146VLL	48	1024	128	81	100	LQFP	Tray
MCXA146VMP	MCXA146VMP	48	1024	128	50	64	LFBGA	Tray
MCXA146VPJ	MCXA146VPJ	48	1024	128	82	112	VFBGA	Tray
MCXA154VLL	MCXA154VLL	96	256	64	81	100	LQFP	Tray
MCXA154VMP	MCXA154VMP	96	256	64	50	64	LFBGA	Tray
MCXA154VPJ	MCXA154VPJ	96	256	64	82	112	VFBGA	Tray
MCXA155VLL	MCXA155VLL	96	512	96	81	100	LQFP	Tray
MCXA155VMP	MCXA155VMP	96	512	96	50	64	LFBGA	Tray
MCXA155VPJ	MCXA155VPJ	96	512	96	82	112	VFBGA	Tray
MCXA156VLL	MCXA156VLL	96	1024	128	81	100	LQFP	Tray
MCXA156VMP	MCXA156VMP	96	1024	128	50	64	LFBGA	Tray
MCXA156VPJ	MCXA156VPJ	96	1024	128	82	112	VFBGA	Tray

Table 2. Device Revision Number

Device Mask Set Number	DIE_ID	JTAG ID Register[PRN]
0P29K	0x0059DAA0	0x0726702B

Table 3. Related Resources

Type	Description	Resource
Fact Sheet	The Fact Sheet gives overview of the product key features and its uses.	MCXA1xxFS
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	MCXAP100M96FS6RM
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	MCXA156_P29K
Package drawing	Package dimensions are provided in package drawings.	• LQFP100: 98ASS23308W • LFBGA64: 98ASA02085D

Table continues on the next page...

Table 3. Related Resources (continued)

Type	Description	Resource
		• VFBGA112: 98ASA02081D
Software development kit	MCUXpresso SDK. An open source software development kit (SDK) built specifically for your processor and evaluation board selections.	http://www.nxp.com/mcuxpresso

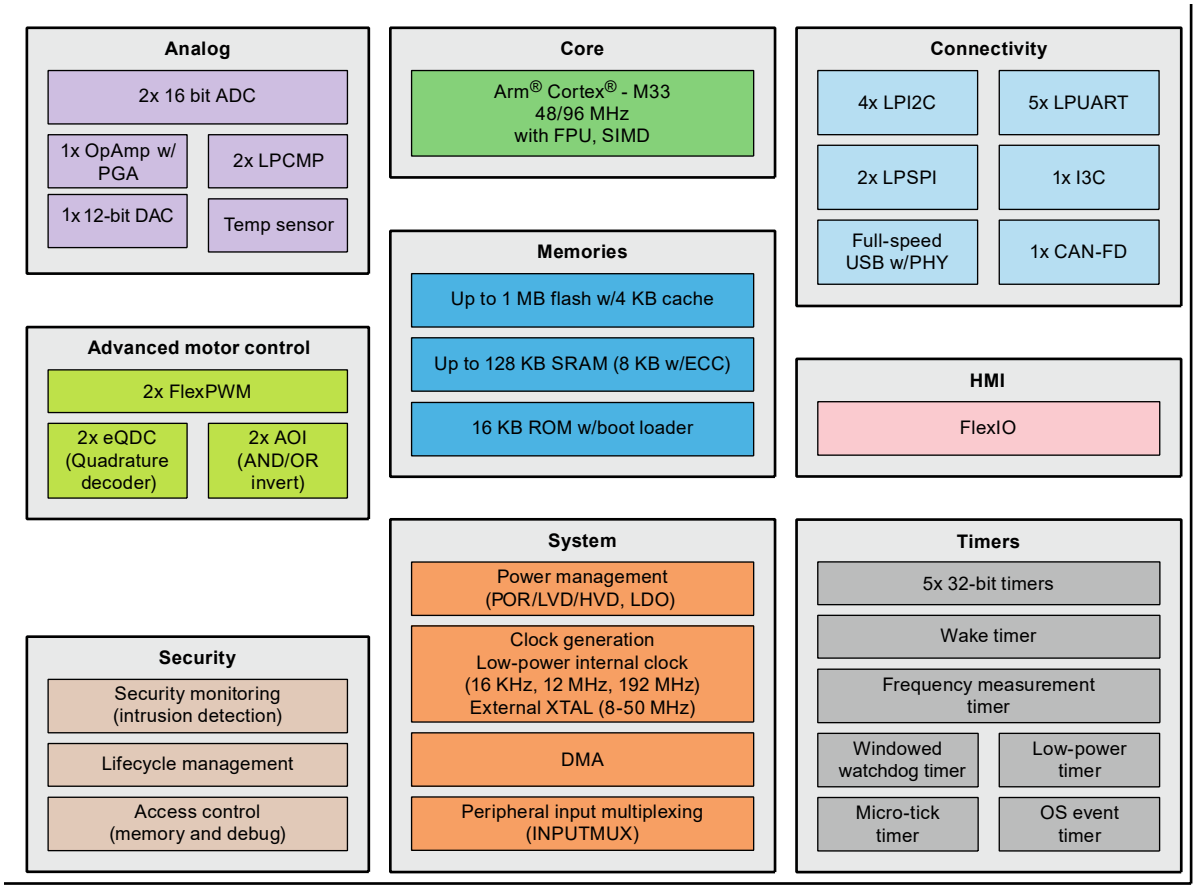

Figure 1. Block Diagram

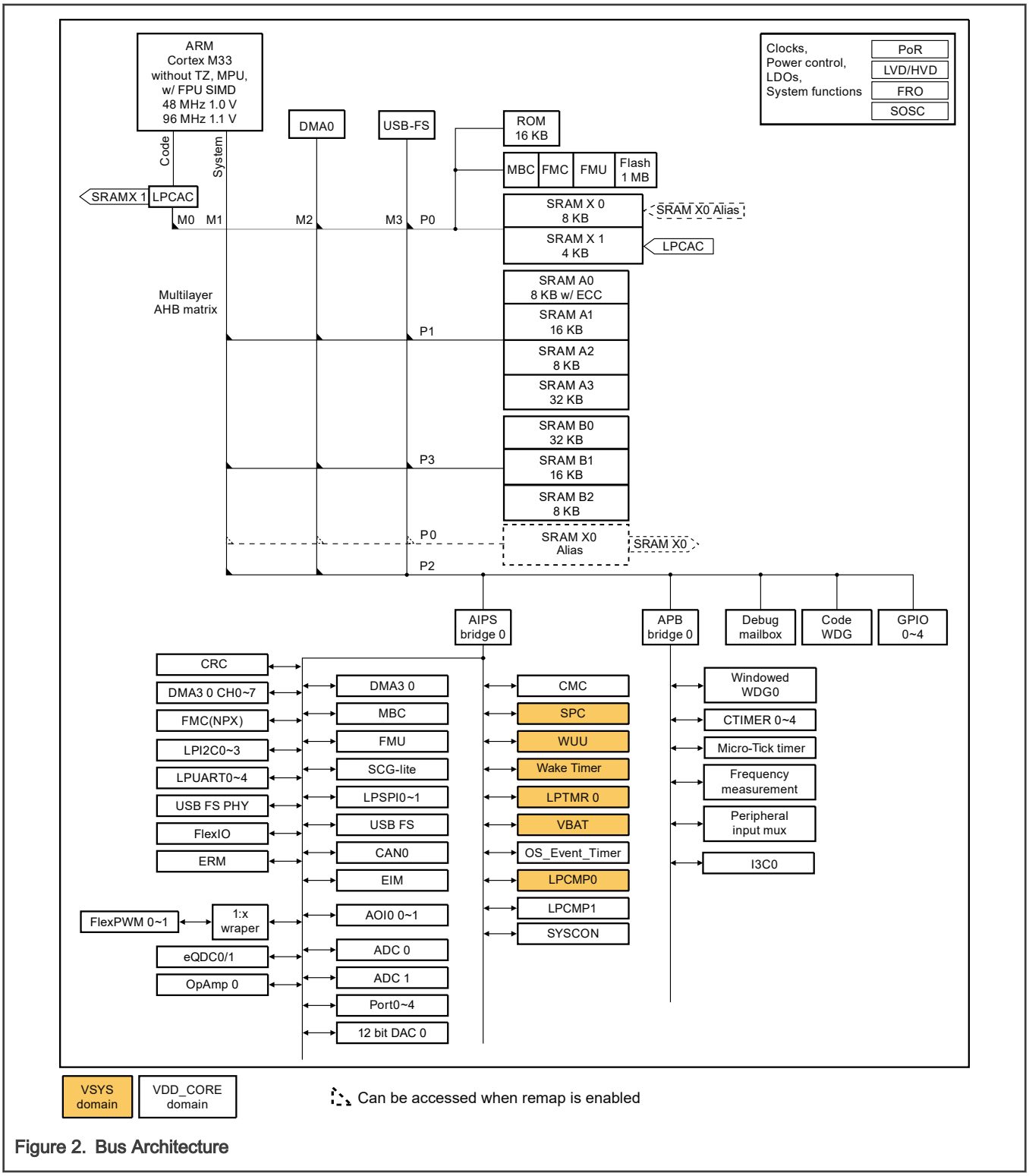

Figure 2. Bus Architecture

Contents

1 Feature Comparison

Table 4. Feature Comparison

		MCXA146	MCXA145	MCXA144	MCXA156	MCXA155	MCXA154
Core Platform	Core Cortex-M33	48 MHz	48 MHz	48 MHz	96 MHz	96 MHz	96 MHz
	Cache	4 kB					
	DMA	8 Channels					
	Wakeup unit (WUU)	Yes					
	Peripheral input multiplexing (INPUTMUX)	Yes					
Clock	Fast internal reference clock FRO192M	48 MHz	48 MHz	48 MHz	192 MHz	192 MHz	192 MHz
	Slow internal reference clock FRO12M	12 MHz					
	Low power internal reference clock FRO16K	16.384 KHz					
	System oscillator with external crystal (SOSC)	8-50 MHz					
Memory	Flash	1024 kB	512 kB	256 kB	1024 kB	512 kB	256 kB
	SRAM	128 kB including 8 kB with ECC	96 kB including 8 kB with ECC	64 kB including 8 kB with ECC	128 kB including 8 kB with ECC	96 kB including 8 kB with ECC	64 kB including 8 kB with ECC
	Error injection module (EIM)	Yes					
	Error recording module (ERM)	Yes					
Security	Lifecycle management (LC)	Yes					
	Read out protection (ROP)	Yes					
	Memory block checker (MBC)	Yes					
	GLIKEY	Yes					
	UUID	128-bit					
	Code watchdog (CDOG)	1					
	Cyclic redundancy check (CRC)	1					

Table continues on the next page...

Table 4. Feature Comparison (continued)

		MCXA146	MCXA145	MCXA144	MCXA156	MCXA155	MCXA154
Communication Interfaces	LPUART	5					
	LPSPI	2					
	LPI2C	4					
	I3C	1					
	USB FS Device	1					
	FlexCAN[1]	1	1	1	1x CAN FD	1x CAN FD	1x CAN FD
	Flexible I/O (FlexIO)	1					
Analog	Low power comparator (LPCMP)	2					
	ADC	2					
	DAC	0	0	0	1	1	1
	OPAMP	0	0	0	1	1	1
Motor Control	FlexPWM [2]	1	1	1	2	2	2
	AND/OR INVERT (AOI)	2					
	Quadrature decoder (eQDC)[3]	1	1	1	2	2	2
Timer	32-bit timer (CTimer)	5					
	Low power timer (LPTMR)	1					
	Micro-tick timer (UTICK)	1					
	OS event timer	1					
	Windowed watchdog timer (WWDT)	1					
	Frequency measurement (FREQME)	1					
	Wake timer	1					
IO	Independent IO supply [4]	VDD_P3					
	5V tolerant IO [5]	2					
	High drive IO (20 mA) [6]	Up to 8					
	50 MHz IO [7]	Up to 21					
Packages [8]	VFBGA112 (PJ)	82					
	LQFP100 (LL)	81					
	LFBGA64 (MP)	50					
	Temperature Range	-40 °C to 125 °C					

1. Flexible data rate (CAN FD) is available on MCXA156/A155/A154
2. FlexPWM0 is available on MCXA146/A145/A144. There're 3 sub-modules for each FlexPWM module.
3. eQDC0 is available on MCXA146/A145/A144.

4. Support 1.2V IO power supply.
5. P3_27, P3_28 are 5V tolerant IOs.
6. P1_8,P1_9,P1_30,P1_31,P3_1,P3_0,P0_16,P0_17 are High Drive IOs.
7. 50 MHz IOs are located on P1, P3, P4 ports.
8. Show the package types and GPIO numbers

2 Ratings

2.1 Thermal handling ratings

Table 5. Thermal handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
TSTG	Storage temperature [1]	–55	—	150	°C	—
TSDR	Solder temperature, lead-free [2]	—	—	260	°C	—

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.
2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

2.2 Moisture handling ratings

Table 6. Moisture handling ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
MSL	Moisture sensitivity level [1]	—	—	3	—	—

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

2.3 ESD handling ratings

Table 7. ESD handling ratings

Description	Rating	Unit	Notes
Electrostatic discharge voltage, human body model	+/-2000	V	[1]
Electrostatic discharge voltage, charged-device model	+/-500	V	[2]
Electrostatic discharge voltage, charged device model (corner pins)	+/-750	V	[2]
Latch-up immunity level (Class II at 125 °C junction temperature)	Immunity Level A	—	[3]

1. Determined according to ANSI/ESDA/JEDEC Standard JS-001-2023, For Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM) - Device Level.
2. Determined according to ANSI/ESDA/JEDEC Standard JS-002-2022, For Electrostatic Discharge Sensitivity Testing, Charged Device Model (CDM) - Device Level.
3. Determined according JEDEC Standard JESD78F, IC Latch-Up Test.

2.4 Voltage and current maximum ratings

Table 8. Voltage and current maximum ratings

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage for Port 0, Port 1, Port 2	-0.3	—	3.63	V	—
VDD_P3	Supply Voltage for Port 3	-0.3	—	3.63	V	—
VDD_ANA	Supply voltage for ADC	-0.3	—	3.63	V	—
VDD_USB	Supply voltage for USB analog	-0.3	—	3.63	V	—
VUSB0_Dx	USB0_DP and USB0_DM input voltage	-0.3	—	3.63	V	—
VDIO	Digital input voltage	-0.3	—	VDD + 0.3	V	—
VDIO_5VTOL	Digital input voltage for 5V tolerant I/O pins	-0.3	—	min(VDD + 3.6V, 5.5V)	V	—
VAIO	Analog input voltageAnalog pins are defined as pins that do not have an associated general-purpose I/O port function. [1]	-0.3	—	VDD_ANA + 0.3	V	—
IDD	Digital supply current [2]	—	—	100	mA	—
ID	Maximum current single pin limit (digital output pins)	-25	—	25	mA	—

1. Analog pins are defined as pins that do not have an associated general-purpose I/O port function.
2. This limit is per supply pin. It includes all power pins, including VDD, VDD_P3, VDD_ANA, VDD_USB.

2.5 Required Power-On-Reset (POR) Sequencing

- VDD and VDD_ANA must be same voltage

3 General

3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

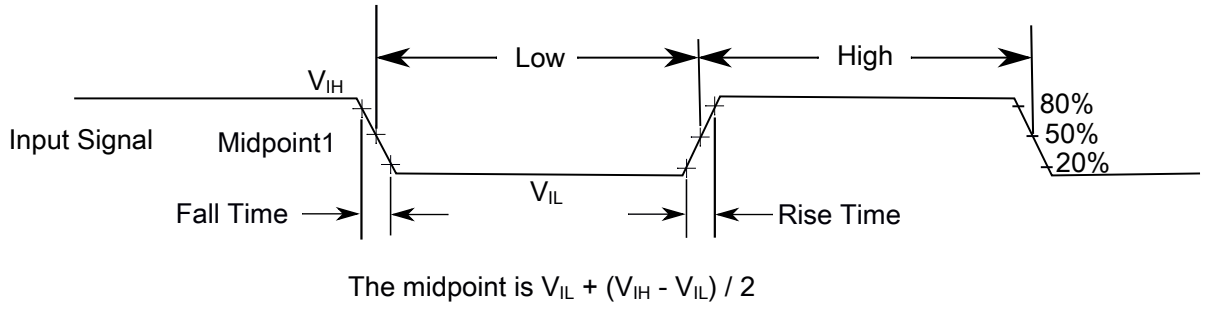

Figure 3. Input signal measurement reference

3.2 Nonswitching electrical specifications

3.2.1 Voltage and current operating requirement

Table 9. Voltage and current operating requirement

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply Voltage for IO, LDO, Flash, and LPCMP	1.71	—	3.6	V	—
VDD_P3	Supply voltage for Port 3	1.14	—	1.32	V	1.2V
VDD_P3	Supply Voltage for Port 3	1.71	—	3.6	V	Normal condition
VDD_ANA	Supply voltage for ADC	VDD - 0.1	—	VDD + 0.1	V	—
VSS - VSS_ANA	VSS-to-VSS_ANA differential voltage	-0.1	—	0.1	V	—
VDD_USB	Supply voltage for USB analog	3.0	—	3.6	V	—
VIH	Input high voltage	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIH_5VTOL	Input high voltage of 5V tolerant IO	0.7 × VDD	—	—	V	1.71 V ≤ VDD ≤ 3.6 V
VIL	Input low voltage	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VIL_5VTOL	Input low voltage of 5 V tolerant IO	—	—	0.3 × VDD	V	1.71 V ≤ VDD ≤ 3.6 V
VHYS	Input hysteresis	0.1 × VDD	—	—	V	—
VHYS_5VTOL	Input hysteresis of 5 V tolerant IO	0.1 × VDD	—	—	V	—
IICIO	IO pin DC injection current — per pin [1]	-3	—	—	mA	VIN < VSS-0.3 V (negative current injection)

Table continues on the next page...

Table 9. Voltage and current operating requirement (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
IICIO	IO pin DC injection current — per pin [1]	—	—	3	mA	VIN > VDD+0.3 V (positive current injection)
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	-25	—	—	mA	Negative current injection
IICcont	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins	—	—	25	mA	Positive current injection
VODPU	Open drain pullup voltage level [2]	VDD	—	VDD	V	—

1. All I/O pins are internally clamped to VSS and VDD through an ESD protection diode. If VIN is greater than VDD_MIN(=VSS-0.3 V) or is less than VDD_MAX(=VDD+ 0.3 V), then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed, then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (-0.3 - VIN)/(-IICIOmin). The positive injection current limiting resistor is calculated as R=(VIN-VDD_MAX)/IICIOmax. The actual resistor should be an order of magnitude higher to tolerate transient voltages
2. Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, VDD as appropriate.

3.2.2 HVD, LVD, and POR operating requirements

The device includes low-voltage detection (LVD) and high-voltage detection (HVD) power supervisor circuits for following power supplies:

- VDD

3.2.2.1 VDD supply HVD, LVD, and POR Operating Requirements

Table 10. VDD supply HVD, LVD, and POR Operating Requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VHVDH_VDD	VDD Rising high-voltage detect threshold (HVD assertion)	3.730	3.810	3.890	V	—
VHVDH_HYS_VDD	VDD High-voltage inhibit reset/ recover hysteresis	—	38	—	mV	—
VLVDH_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - high range	2.567	2.619	2.673	V	—
VLVDH_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - high range	—	27	—	mV	—
VLVDL_VDD	VDD Falling low-voltage detect threshold (LVD assertion) - low range	1.618	1.651	1.684	V	—
VLVDL_HYS_VDD	VDD Low-voltage inhibit reset/ recover hysteresis - low range	—	16	—	mV	—

3.2.3 Voltage and current operating behaviors

Table 11. Voltage and current operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 4 mA
VOH	Output high voltage — Normal drive strength [1]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 2.5 mA
VOH	Output high voltage — Normal drive strength [1]	VDD - 0.5	—	—	V	1.14 V ≤ VDD < 1.32 V, IOH = 0.5 mA
VOH	Output high voltage — High drive strength [1,2]	VDD – 0.5	—	—	V	2.7 V ≤ VDD ≤ 3.6 V, IOH = 6 mA
VOH	Output high voltage — High drive strength [1,2]	VDD – 0.5	—	—	V	1.71 V ≤ VDD < 2.7 V, IOH = 3.75 mA
VOH	Output high voltage — High drive strength [1,2]	VDD - 0.5	—	—	V	1.14 V ≤ VDD < 1.32 V, IOH = 0.75 mA
IOHT	Output high current total for all ports	—	—	100	mA	—
VOL	Output low voltage — Normal drive strength [1,3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 4 mA
VOL	Output low voltage — Normal drive strength [1,3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 2.5 mA
VOL	Output low voltage — Normal drive strength [1,3]	—	—	0.5	V	1.14 V ≤ VDD < 1.32 V, IOL = 0.5 mA
VOL	Output low voltage — High drive strength [1,2,3]	—	—	0.5	V	2.7 V ≤ VDD ≤ 3.6 V, IOL = 6 mA
VOL	Output low voltage — High drive strength [1,2,3]	—	—	0.5	V	1.71 V ≤ VDD < 2.7 V, IOL = 3.75 mA
VOL	Output low voltage — High drive strength [1,2,3]	—	—	0.5	V	1.14 V ≤ VDD < 1.32 V, IOL = 0.75 mA
IOLT	Output low current total for all ports	—	—	100	mA	—
IIN	Input leakage current (per pin) for full temperature range [4]	—	0.02	1	µA	—
IIN	Input leakage current (per pin) at 25 °C [4]	—	0.001	0.025	µA	—
IIN	Input leakage current (total all pins) for full temperature range [4]	—	0.025	41	µA	—
IOZ	Hi-Z (off-state) leakage current (per pin)	—	0.02	1	µA	—
RPU	Internal pullup resistors	33	50	75	kΩ	—

Table continues on the next page...

Table 11. Voltage and current operating behaviors (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
RPU (I3C)	Internal pullup resistors [5]	(VDD - 0.27 V)/3 mA	1.75	—	kΩ	—
RPD	Internal pulldown resistors	33	50	75	kΩ	—
RHPU	High-resistance pullup option (PCRx[PV] = 1) [6]	0.67	—	1.5	MΩ	—
RHPD	High-resistance pulldown option (PCRx[PV] = 1) [6]	0.67	—	1.5	MΩ	—
VBG	Bandgap voltage reference voltage	0.98	1.0	1.02	V	—

1. For the HD pads, when setting DSE1=1, the IOH/IOL are four times higher at the same VOH/VOL.
2. RESET_B pins are always configured in high drive mode
3. Open drain outputs must be pulled to VDD
4. Measured at VDD = 3.6 V.
5. Only I3C pins support this option
6. Only RST pins support this option.

3.2.4 On-chip regulator electrical specifications

3.2.4.1 LDO_CORE electrical specifications

Table 12. LDO_CORE electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	LDO_CORE input supply voltage	1.71	—	3.6	V	—
ILOAD	LDO_CORE max load current	—	—	16	mA	Normal drive strength
ILOAD	LDO_CORE max load current	—	—	2	mA	Low drive strength
IDD	LDO_CORE current consumption	—	—	250	µA	Normal drive strength
IDD	LDO_CORE current consumption	—	—	500	nA	Low drive strength
IINRUSH	LDO_CORE inrush current	—	—	10	mA	—

3.2.5 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- CPU clock = 48 MHz
- AHB clock = 48 MHz
- Clock source = FIRC

Table 13. Power mode transition operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
tPOR	After a POR event, amount of time to execution of the first instruction (measured from the point where VDD reach 1.8V) across the operating temperature range of the chip. [1,2]	—	2.34	2.43	ms	—
tSLEEP	Sleep → Active [1,2,3,4]	—	0.23	0.27	µs	—
tDSLEEP	Deep Sleep → Active [1,2,3,4]	—	7.1	8.4	µs	—
tPWDN	Power Down → Active [1,2,3,5]	—	16.6	19.9	µs	—
tDPWDN	Deep Power Down → Active [1,2,3,4]	—	1.44	1.52	ms	—

1. Max value is mean+3 × sigma of tested values at the worst case of ambient temperature range and VDD 1.71 V to 3.6 V. Max values are based on characterization but not covered by test limits in production.
2. Typical value is the average of values tested at Temperature=25 ℃ and VDD=3.3 V
3. WFE used for Low Power mode entry
4. SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x00 and the Core voltage level is configured for the same level in Active and Low Power mode (SPC->ACTIVE_CFG[CORELDO_VDD_LVL]=SPC->LP_CFG[CORELDO_VDD_LVL]= 01b).
5. SPC->LPWKUP_DELAY[LPWKUP_DELAY] = 0x5B and the Core voltage level is configured as different level for Active mode, (SPC->ACTIVE_CFG[CORELDO_VDD_LVL] = 01b for Active mode, SPC->LP_CFG[CORELDO_VDD_LVL] = 00b for Low Power mode)

3.2.6 Power consumption operating behaviors

When calculating the total MCU current consumption the following considerations should be made:

- Specifications below only include power for the MCU itself including VDD, VDD_ANA, VDD_P3.
- VDD_USB current draw are not included
- On top of the device's IDD current consumption, external loads applied to pins of the device need to be considered

Symbol	Description	Condition [1]	Typ	Unit
IDD_ACT_MD_1 [2]	1. CPU_CLK = 48 MHz from FRO192M; VDD_CORE = 1.0 V from LDO_CORE normal drive. 2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	3.06	mA
		105 °C	3.62	mA
		125 °C	4.17	mA
IDD_ACT_MD_2	1. CPU_CLK = 48 MHz from FRO192M; VDD_CORE = 1.0 V from LDO_CORE normal drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	3.31	mA
		105 °C	3.90	mA
		125 °C	4.47	mA
IDD_ACT_MD_CM_1	1. CPU_CLK = 48 MHz from FRO192M; VDD_CORE = 1.0 V from LDO_CORE normal drive.	25 °C	3.40	mA

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	2. All peripheral clocks disabled; Flash is configured to LP mode; Cache enabled. 3. CoreMark executing from internal flash.	105 °C	3.95	mA
		125 °C	4.48	mA
IDD_ACT_MD_CM_2	1. CPU_CLK = 48 MHz from FRO192M; VDD_CORE = 1.0 V from LDO_CORE normal drive. 2. All peripheral clocks enabled; Cache enabled. 3. CoreMark executing from internal flash.	25 °C	3.66	mA
		105 °C	4.23	mA
		125 °C	4.79	mA
IDD_ACT_SD_1	1. CPU_CLK = 96 MHz from FRO192M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	6.40	mA
		105 °C	7.11	mA
		125 °C	7.76	mA
IDD_ACT_SD_2	1. CPU_CLK = 96 MHz from FRO192M, FRO192M output is 192MHz; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks enabled; Cache enabled. 3. While(1) loop executing from internal flash.	25 °C	7.45	mA
		105 °C	8.16	mA
		125 °C	8.82	mA
IDD_ACT_SD_CM_1	1. CPU_CLK = 96 MHz from FRO192M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled; Cache enabled. 3. CoreMark executing from internal flash.	25 °C	7.09	mA
		105 °C	7.72	mA
		125 °C	8.40	mA
IDD_ACT_SD_CM_2	1. CPU_CLK = 96 MHz from FRO192M, FRO192M output is 192MHz; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks enabled; Cache enabled. 3. CoreMark executing from internal flash.	25 °C	8.13	mA
		105 °C	8.79	mA
		125 °C	9.42	mA
IDD_SLEEP_SD	1. CPU_CLK = OFF, SYSTEM_CLK = 96 MHz from FRO192M; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. All peripheral clocks disabled.	25 °C	3.34	mA
		105 °C	4.05	mA
		125 °C	4.70	mA
IDD_SLEEP_MD_1	1. CPU_CLK = OFF, SYSTEM_CLK = 48 MHz from FRO192M; VDD_CORE = 1.0 V from LDO_CORE normal drive. 2. All peripheral clocks disabled.	25 °C	1.81	mA
		105 °C	2.39	mA
		125 °C	2.93	mA

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IDD_SLEEP_MD_2	1. CPU_CLK = OFF, SYSTEM_CLK = 12 MHz from FRO12M; VDD_CORE = 1.0 V from LDO_CORE low drive. 2. All peripheral clocks disabled.	25 °C	0.43	mA
		105 °C	0.99	mA
		125 °C	1.55	mA
IDD_DEEP_SLEEP_SD	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 1.1 V from LDO_CORE normal drive. 2. Core domain in Deep Sleep; FRO12M disabled.	25 °C	257.98	µA
		105 °C	781.14	µA
		125 °C	1286.88	µA
IDD_DEEP_SLEEP_MD_1	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE low drive. 2. Core domain in Deep Sleep; FRO12M disabled.	25 °C	32.26	µA
		105 °C	470.82	µA
		125 °C	916.19	µA
IDD_DEEP_SLEEP_MD_2	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = 1.0 V from LDO_CORE low drive. 2. Core domain in Deep Sleep; FRO12M enabled.	25 °C	104.53	µA
		105 °C	542.00	µA
		125 °C	988.01	µA
IDD_POWER_DOWN_1	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = retention voltage from LDO_CORE low drive. 2. Core domain in Power Down(Lowest power mode can retain all registers); All RAM retained; FRO16K disabled.	25 °C	9.47	µA
		105 °C	257.00	µA
		125 °C	520.08	µA
IDD_POWER_DOWN_2	1. CPU_CLK = SYSTEM_CLK = OFF; VDD_CORE = retention voltage from LDO_CORE low drive. 2. Core domain in Power Down(Lowest power mode can retain all registers); RAM X0/X1 and RAM A0 retained; FRO16K disabled.	25 °C	8.20	µA
		105 °C	222.28	µA
		125 °C	443.17	µA
IDD_DEEP_POWER_DOWN_1	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in Deep Power Down; All RAM OFF; FRO16K disabled; Wakeup timer disabled.	25 °C	0.41	µA
		105 °C	5.62	µA
		125 °C	12.88	µA
IDD_DEEP_POWER_DOWN_2	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in Deep Power Down; All RAM OFF; FRO16K enabled; Wakeup timer enabled.	25 °C	0.60	µA
		105 °C	5.83	µA
		125 °C	13.08	µA
IDD_DEEP_POWER_DOWN_3	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in Deep Power Down; All RAM retained; FRO16K enabled; Wakeup timer enabled.	25 °C	2.19	µA
		105 °C	47.39	µA
		125 °C	105.34	µA
IDD_DEEP_POWER_DOWN_4	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off.	25 °C	1.57	µA

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	2. Core domain in Deep Power Down; RAM X0/X1 and RAM A0~A3 retained; FRO16K enabled; Wakeup timer enabled.	105 °C	29.84	µA
		125 °C	66.33	µA
IDD_DEEP_POWER_DOWN_5	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in Deep Power Down; RAM X0/X1 and RAM A0 retained; FRO16K enabled; Wakeup timer enabled.	25 °C	0.93	µA
		105 °C	12.71	µA
		125 °C	28.28	µA
IDD_DEEP_POWER_DOWN_6	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in Deep Power Down; RAM A0 retained; FRO16K enabled; Wakeup timer enabled.	25 °C	0.79	µA
		105 °C	8.86	µA
		125 °C	19.80	µA
IDD_DEEP_POWER_DOWN_7	1. CPU_CLK = SYSTEM_CLK = OFF; LDO_CORE is powered off. 2. Core domain in Deep Power Down; RAM X0/X1 retained; FRO16K enabled; Wakeup timer enabled.	25 °C	0.82	µA
		105 °C	9.88	µA
		125 °C	22.00	µA

1. **Ambient temperature**
2. SD standard drive, core voltage is 1.1V. MD middle drive, core voltage is 1.0V

3.2.7 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

3.2.8 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

3.2.9 Capacitance attributes

Table 14. Capacitance attributes

Symbol	Description	Min	Typ	Max	Unit	Condition
CIN_A	Input capacitance: analog pins	—	—	7	pF	—
CIN_D	Input capacitance: digital pins	—	—	7	pF	—

3.3 Switching specifications

3.3.1 Device clock specs

Table 15. Device clock specs

Symbol	Description	Min	Typ	Max	Unit	Condition
fCPU	CPU clock (CPU_CLK)	—	—	96	MHz	Standard drive (SD) mode VDD_CORE = 1.1 V
fSYSTEM	SYSTEM clock (SYSTEM_CLK)	—	—	96	MHz	Standard drive (SD) mode VDD_CORE = 1.1 V
fSLOW	Slow clock (SLOW_CLK)	—	—	24	MHz	Standard drive (SD) mode VDD_CORE = 1.1 V
fCPU	CPU clock (CPU_CLK)	—	—	48	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSYSTEM	SYSTEM clock (SYSTEM_CLK)	—	—	48	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V
fSLOW	Slow clock (SLOW_CLK)	—	—	12	MHz	Middle drive (MD) mode VDD_CORE = 1.0 V

3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPUART, LPI2C, LPI3C, LPSPI functions.

3.3.2.1 General switching specifications

NOTE

Refer to attached pinout spreadsheet.

Table 16. General switching specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
—	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path [1]	1.5	—	—	SYSTEM clock cycles	The synchronous and asynchronous timing must be met.
—	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	150	—	—	ns	—
—	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	—	ns	—

Table continues on the next page...

Table 16. General switching specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	External RST pin interrupt pulse width — Asynchronous path [2]	330	—	—	ns	This is the shortest pulse that is guaranteed to be recognized.
—	GPIO pin interrupt pulse width — Asynchronous path [2]	16	—	—	ns	—
—	Port rise/fall time for slow I/O pins [3,4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins [3,4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins [3,4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins [3,4]	9	—	45	ns	1.14 ≤ VDD < 1.32 V, Slow slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for slow I/O pins [3,4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	3.5	—	15	ns	2.7 ≤ VDD≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for slow I/O pins, 5V Tolerant [3,4]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 1; DSE = 1)
—	Port rise/fall time for slow I/O pins [3,4]	3.5	—	14	ns	1.14 ≤ VDD < 1.32 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for medium I/O pins [5,6]	0.8	—	4	ns	2.7 ≤ VDD ≤ 3.6 V, Fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for medium I/O pins [5,6]	1	—	7	ns	2.7 ≤ VDD ≤ 3.6 V, Slow slew rate (SRE = 1; DSE = 0)

Table continues on the next page...

Table 16. General switching specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Port rise/fall time for medium I/O pins [5,6]	0.8	—	4	ns	1.71 ≤ VDD < 2.7 V, Fast slew rate (SRE = 0; DSE = 1)
—	Port rise/fall time for medium I/O pins [5,6]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, Slow slew rate (SRE = 1; DSE = 1)
—	HD pins [7]	2.2	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive, fast slew rate (SRE = 0; DSE = 0)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	2.7 ≤ VDD≤ 3.6 V, Normal drive (DSE = 0), fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	15	ns	2.7 ≤ VDD ≤ 3.6 V, Normal drive (DSE =0), slow slew rate (SRE = 1)
—	Port rise/fall time for HD pins [7]	3.5	—	14	ns	1.14 ≤ VDD < 1.32 V, Fast slew rate (SRE = 0; DSE = 1 or 3)
—	Port rise/fall time for HD pins [7]	9	—	45	ns	1.14 ≤ VDD < 1.32 V, Slow slew rate (SRE = 1; DSE = 1 or 3)
—	Port rise/fall time for HD pins [7]	1	—	7	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE=1), Fast slew rate (SRE = 0)
—	Port rise/fall time for HD pins [7]	3.5	—	25	ns	1.71 ≤ VDD < 2.7 V, High drive (DSE =1), Slow slew rate (SRE=1)
—	RST pins [4]	3	—	8	ns	2.7 ≤ VDD ≤ 3.6 V
—	RST pins [4]	3.6	—	20	ns	1.71 ≤ VDD < 2.7 V

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized
3. For the HD I/O pins, setting DSE1 = 1 will support the same rise/fall time at 4x the load capacitance. For the 5VTOL I/O pins, setting DSE1=1 will support the same fall time at 2x the load capacitance, but the rise time will increase due to the increased loading
4. Load is 25 pF.
5. Assumes default values in CALIB1 and CALIB0 in PORTS
6. 25 pF lumped load
7. Load is 25 pF for DSE=0. Load is 100 pF for DSE=2 or DSE=3. Drive strength and slew rate are configured using PORTx_PCRn[DSE1], PORTx_PCRn[DSE], and PORTx_PCRn[SRE].

3.4 Thermal specifications

3.4.1 Thermal operating requirements

Table 17. Thermal operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
TA	Ambient temperature [1]	-40	25	125	°C	—
TJ	Die junction temperature [2,3,4]	—	—	125	°C	—

1. The device may operate at maximum TA rating as long as TJ maximum of 125 °C is not exceeded. The simplest method to determine TJ is: TJ = TA + RθJA*chip power dissipation.
2. Operating at maximum conditions for extended periods may affect device reliability. Refer to Product Lifetime Usage Estimates application note (AN14194)
3. The device operating specification is not guaranteed beyond 125 °C TJ.
4. The maximum operating requirement applies to all chapters unless otherwise specifically stated.

3.4.2 Thermal attributes

Table 18. Thermal attributes

Rating	Board Type[1]	Symbol	64 LFBGA	100 LQFP	112 VFBGA	Unit
Junction to Ambient Thermal Resistance [2]	JESD51-9, 2s2p	$R_{\theta JA}$	51.1	52.7	53.0	°C/W
Junction-to-Top of Package Thermal Characterization Parameter [2]	JESD51-9, 2s2p	Ψ_{JT}	8.4	6.0	4.8	°C/W
Junction to Case Top Thermal Resistance [3]	NA	$R_{\theta JC}$	46.9	24.0	13.1	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9)
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment
3. Junction-to-Case top thermal resistance determined using an isothermal cold plate.

4 Peripheral operating requirements and behaviors

4.1 Core modules

4.1.1 Debug trace operating behaviors

Table 19. Debug trace operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Frequency of operation	—	—	36	MHz	SD mode
—	Frequency of operation	—	—	25	MHz	MD mode
T1	Clock period	27.78	—	—	ns	SD mode
T1	Clock period	40	—	—	ns	MD mode

Table continues on the next page...

Table 19. Debug trace operating behaviors (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
T2	Low pulse width	2	—	—	ns	—
T3	High pulse width	2	—	—	ns	—
T4	Clock and data rise time	—	—	3	ns	—
T5	Clock and data fall time	—	—	3	ns	—
T6	Data setup	1.5	—	—	ns	—
T7	Data hold	1.0	—	—	ns	—

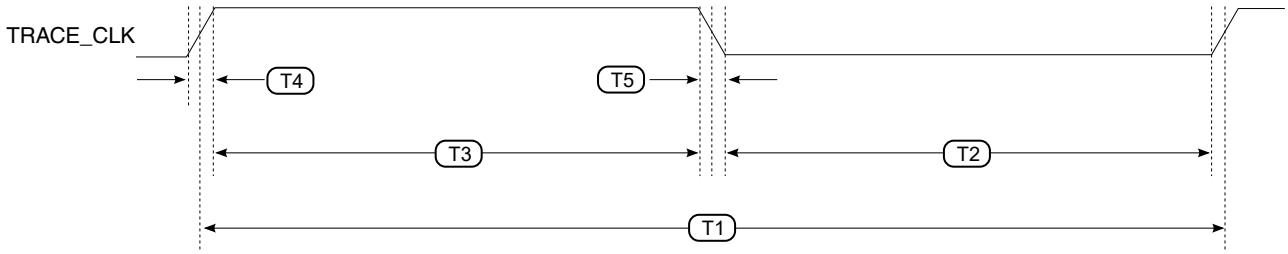


Figure 4. TRACE_CLKOUT specifications

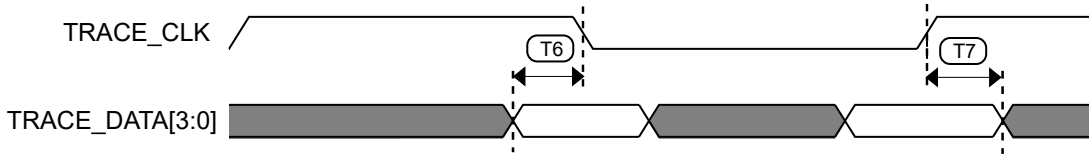


Figure 5. Trace data specifications

4.1.2 JTAG Debug Interface Timing

The following table gives the JTAG specifications in debug interface mode.

Table 20. JTAG Debug Interface Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
J1	TCLK frequency of operation	—	—	25	MHz	Boundary Scan (SD mode)
J1	TCLK frequency of operation	—	—	12.5	MHz	Boundary Scan (MD mode)
J1	TCLK frequency of operation	—	—	25	—	JTAG-DP/TAP (SD mode)

Table continues on the next page...

Table 20. JTAG Debug Interface Timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
J1	TCLK frequency of operation	—	—	12.5	—	JTAG-DP/TAP (MD mode)
J2	TCLK cycle period	1000/J1	—	—	ns	—
J3	TCLK clock pulse width	J2/2	—	—	ns	—
J4	TCLK rise and fall times	—	—	3	ns	—
J5	Boundary scan input data setup time to TCLK rise	8	—	—	ns	SD mode
J5	Boundary scan input data setup time to TCLK rise	16	—	—	ns	MD mode
J6	Boundary scan input data hold time after TCLK rise	-1	—	—	ns	SD mode
J6	Boundary scan input data hold time after TCLK rise	-1	—	—	ns	MD mode
J7	TCLK low to boundary scan output data valid	—	—	18	ns	SD mode
J7	TCLK low to boundary scan output data valid	—	—	38	—	MD mode
J8	TCLK low to boundary scan output high-Z	—	—	18	ns	SD mode
J8	TCLK low to boundary scan output high-Z	—	—	38	—	MD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	8	—	—	ns	SD mode
J9	JTAG-DP/TAP TMS, TDI input data setup time to TCLK rise	16	—	—	—	MD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	ns	SD mode
J10	JTAG-DP/TAP TMS, TDI input data hold time after TCLK rise	1	—	—	—	MD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	18	—	SD mode
J11	TCLK low to JTAG-DP/TAP TDO data valid	—	—	38	ns	MD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	18	ns	SD mode
J12	TCLK low to JTAG-DP/TAP TDO high-Z	—	—	38	—	MD mode

TDOC represents the TDO bit frame of the scan packet in compact JTAG 2-wire mode.

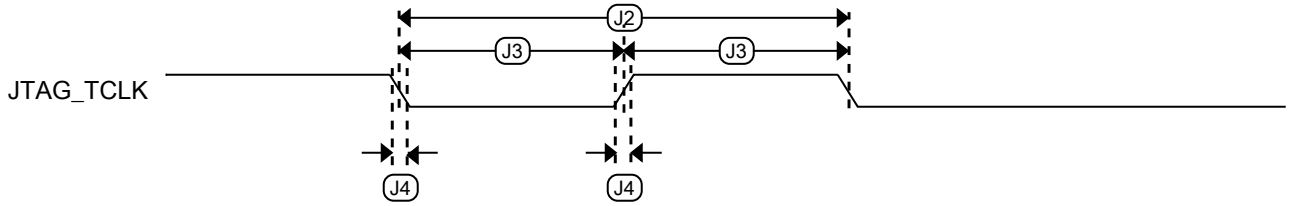


Figure 6. Test clock input timing

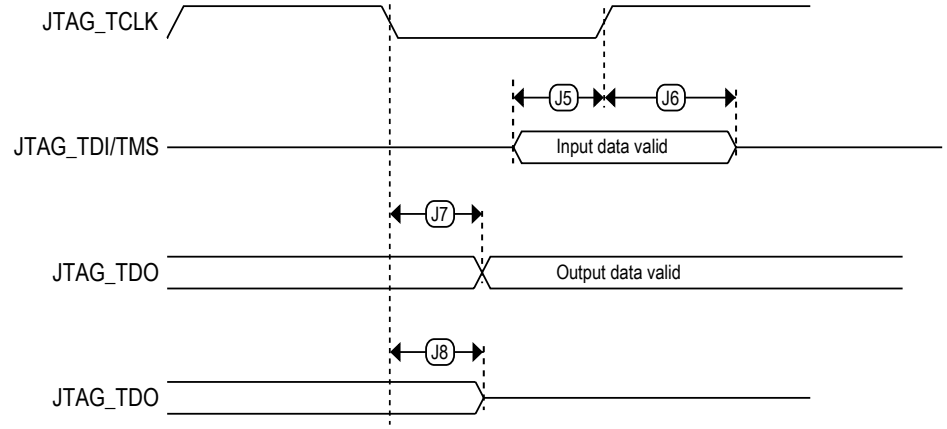


Figure 7. Boundary scan (JTAG) timing

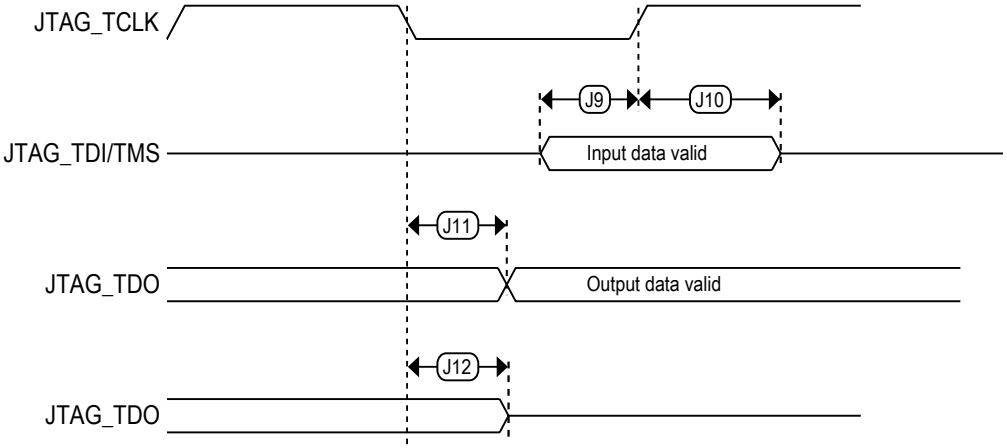


Figure 8. JTAG-DP/TAP timing

4.1.3 Serial Wire Debug (SWD) Timing

The following table gives the Serial Wire Debug specifications for the device.

Table 21. Serial Wire Debug (SWD) Timing

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Operating voltage	1.71	—	3.6	V	—
S1	SWD_CLK frequency of operation	—	—	25	MHz	SD mode
S1	SWD_CLK frequency of operation	—	—	20	MHz	MD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	SD mode
S2	SWD_CLK cycle period	1000/S1	—	—	ns	MD mode
S3	SWD_CLK clock pulse width	20	—	—	ns	SD mode
S3	SWD_CLK clock pulse width	25	—	—	ns	MD mode
S4	SWD_CLK rise and fall times	—	—	3	ns	—
S5	SWD_DIO input data setup time to SWD_CLK rise	10	—	—	ns	SD mode
S5	SWD_DIO input data setup time to SWD_CLK rise	12.5	—	—	ns	MD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	SD mode
S6	SWD_DIO input data hold time after SWD_CLK rise	0	—	—	ns	MD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	25	ns	SD mode
S7	SWD_CLK high to SWD_DIO data valid	—	—	30	ns	MD mode
S8	SWD_CLK high to SWD_DIO high-Z	25	—	—	ns	SD mode
S8	SWD_CLK high to SWD_DIO high-Z	30	—	—	ns	MD mode

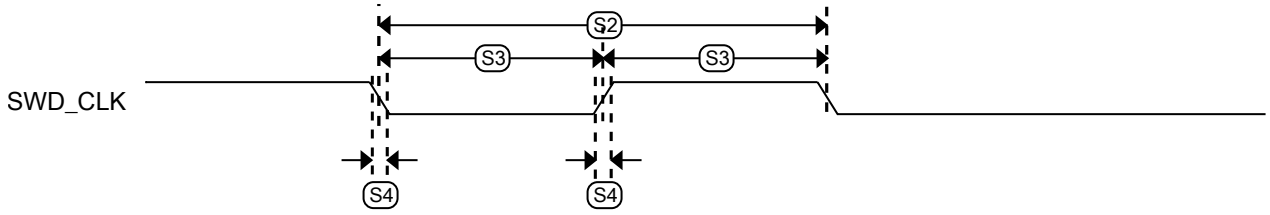


Figure 9. Serial Wire clock input timing

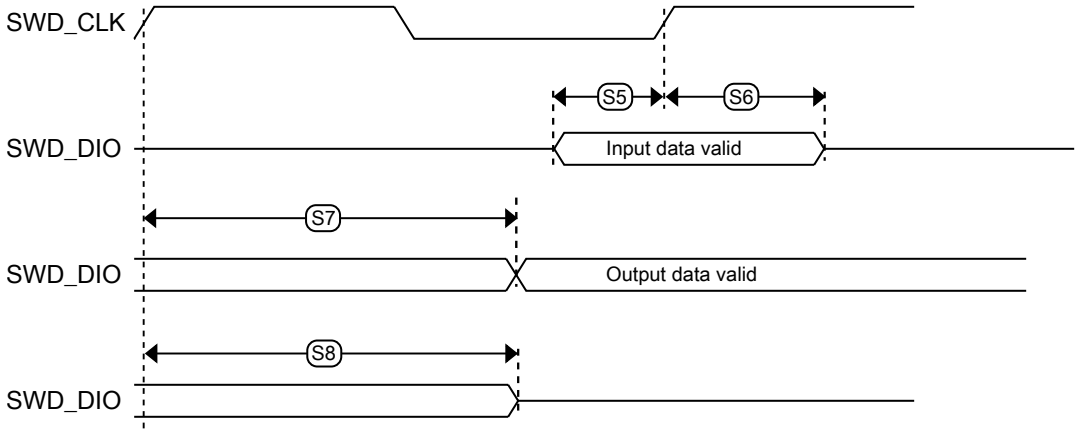


Figure 10. Serial Wire data timing

4.2 Clock modules

4.2.1 Reference Oscillator Specification

This chip is designed to meet targeted specifications with a ±40 ppm frequency error over the life of the part, which includes the temperature, mechanical, and aging excursions.

The table below shows typical specifications for the Crystal Oscillator.

4.2.1.1 System Crystal Oscillator Specification

Table 22. System Crystal Oscillator Specification

Symbol	Description	Min	Typ	Max	Unit	Condition
fosc	Crystal Frequency	8	—	50	MHz	—
Tol	Frequency tolerance	—	±10	±40	ppm	—
Jitosc	Jitter	—	70	—	—	Period jitter (RMS)
Vpp	Peak-to-peak amplitude of oscillation [1]	—	0.6	—	V	—
fec	Externally provided input clock frequency [2]	0	—	50	MHz	—
tDC_EXTAL	External clock duty cycle	45	50	55	%	—
Vec	Externally provided input clock amplitude [2]	Refer to VIH and VIL specification	—	—	—	—

1. When a crystal is being used with the oscillator, the EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.
2. This specification is for an externally supplied clock driven to EXTAL and does not apply to any other clock input.

4.2.1.2 System Oscillator Crystal Specifications.

Table 23. System Oscillator Crystal Specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
CP	Shunt Capacitance	—	1	2	pF	—
ESR	Crystal equivalent series resistance [1]	—	20	50	Ω	—
Cpara	Parasitic capacitance of EXTAL	—	—	8	pF	—
Cpara	Parasitic capacitance of XTAL	—	—	10	pF	—
Cm	Motional capacitance Cm	2.05	2.05	2.665	fF	—
Lm	Motional inductance Lm	7.7	—	—	mH	—
tstart	Crystal start-up time [2]	—	350	500	µs	—
IOSC	Current consumption	—	270	—	µA	Normal mode
IOSC	Current consumption	—	1	465	—	Sleep mode

1. Maximum crystal equivalent series resistance for 16 MHz is 80 ohms with 2 pF shunt capacitance.
2. Dependent on crystal specifications, proper PC board layout procedures must be followed to achieve specifications

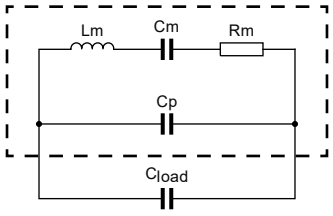


Figure 11. Crystal Electrical Block Diagram

4.2.1.3 System Oscillator Crystal Specifications

Table 24. System Oscillator Crystal Specifications.

Freq Crystal (MHz)	R_m(ohms)	C_p(pF)	C_{load}(pF)	C_m(pF)	L_m(mH)	Typical startup (µs)[1]	Typical Current consumption (µA)[1]	Drive level (µW)	
								min	max
8	100	5.00	18.0	0.008	49.47	1240	168	24	34
16	80	2.00	8.00	0.008	12.37	215	168.3	16	22
16	200	1.00	8.00	0.008	12.37	186	200.4	31	46
25	60	3.00	11.0	0.008	5.07	224	245.6	70	93
25	60	2.00	10.0	0.008	5.07	128	232.5	61	80
25	100	1.00	8.00	0.008	5.07	73.6	232.7	62	82
32	60	3.00	9.00	0.008	3.09	233	269.6	71	95

Table continues on the next page...

Table 24. System Oscillator Crystal Specifications. (continued)

32	60	2.00	8.00	0.008	3.09	116	253.2	59	80
32	100	1.00	8.00	0.008	3.09	52.4	289.3	91	123
40	50	2.00	8.00	0.008	1.98	80.4	296.9	73	99
40	60	3.00	9.00	0.008	1.98	162	333.2	99	135
48	50	2.00	8.00	0.008	1.37	73.1	359.6	104	140
48	60	3.00	9.00	0.008	1.37	155	407.9	138	188

1. This is based on simulation

4.2.2 FRO-192M specifications

Table 25. FRO-192M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro192m	FRO-192M frequency (nominal)	—	192	—	MHz	—
Δffro192m	Frequency deviation (Ta = 0 °C – 85 °C)	—	—	±1.5	%	Open loop
Δffro192m	Frequency deviation (Ta = –40 °C – 125 °C)	—	—	±3	%	Open loop
Δffro192m	Frequency deviation (Ta = –40 °C – 125 °C)	—	—	±0.25	%	Closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	2	—	µs	Oscillation time with initial accuracy of -20 % to +2 % of enable signal assertion
tstartup	Start-up time	—	—	20	µs	Oscillation time within +/- 2 % from enable signal assertion
fos	Frequency overshoot during startup	—	—	2	%	—
jitper	Period jitter RMS [1]	—	70	—	ps	—
jitper	Accumulated jitter over 10K cycles [1]	—	800	—	ps	—
jitcyc	Cycle to cycle jitter [1]	—	100	—	ps	—
Ifro192m_vdd1p8	Current consumption for vdd1p8	—	70	—	µA	—
Ifro192m_vddlv	Current consumption for vddlv	—	35	—	µA	—

1. Tested at 96 MHz

4.2.3 FRO-12M specifications

Table 26. FRO-12M specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro12m	FRO-12M frequency (nominal)	—	12	—	MHz	—
Δffro12m	Frequency deviation	—	—	±3	%	open loop
Δffro12m	Frequency deviation	—	—	±0.6	%	closed loop (using accurate clock source as reference)
tstartup	Start-up time	—	5	—	µs	—
fos	Frequency overshoot during startup	—	10	20	%	—
Ifro12m	Current consumption	—	7	—	µA	—

4.2.4 FRO16K specifications

Table 27. FRO16K specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
ffro16k	FRO16K frequency (nominal)	—	16.384	—	kHz	—
Δffro16k	Frequency deviation over –40 °C to 125 °C Ta	—	—	±6	%	open loop
TRIMstep	Trimming step	—	1.5	—	%	—
tstartup	Start-up time	—	310	—	µs	—
Ifro16k	Current consumption	—	50	—	nA	—

4.3 Memories and memory interfaces

4.3.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

4.3.1.1 Timing specifications

The following command times assume a flash bus clock frequency of 24 MHz. Command times will be increased by up to 10 µs at 24 MHz if the module is exiting Sleep mode when the command is launched. The time to abort a command is not included in the following table.

4.3.1.1.1 Flash command time specifications

Table 28. Flash command time specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1all256k	Read 1s All execution time (256 KB)	—	—	1700	µs	—
trd1all512k	Read 1s All execution time (512 KB)	—	—	3200	µs	—

Table continues on the next page...

Table 28. Flash command time specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
trd1all1MB	Read 1s All execution time (1 MB)	—	—	6200	µs	—
trd1blk256k	Read 1s Block execution time (256 KB)	—	—	1500	µs	—
trd1blk512k	Read 1s Block execution time (512KB)	—	—	3050	µs	—
trd1blk1MB	Read 1s Block execution time (1MB)	—	—	6000	µs	—
trd1scr	Read 1s Sector execution time (8 KB) [1]	—	—	50	µs	—
trd1pg	Read 1s Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1pglv	Read 1s Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1phr	Read 1s Phrase execution time (16B) [1]	—	—	3.8	µs	—
trd1phrlv	Read 1s Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdmisr8k	Read into MISR (8 KB) [1]	—	—	50	µs	—
trdmisr256k	Read into MISR (256 KB)	—	—	1500	µs	—
trdmisr512k	Read into MISR (512 KB)	—	—	3050	µs	—
trdmisr1M	Read into MISR (1 MB) [1]	—	—	6000	µs	—
trd1iscr	Read 1s IFR Sector execution time (8 KB) [1]	—	—	50	µs	—
trd1ipg	Read 1s IFR Page execution time (128 B) [1]	—	—	4.4	µs	—
trd1ipglv	Read 1s IFR Page at low voltage execution time (128 B)	—	—	5.8	µs	—
trd1iphr	Read 1s IFR Phrase execution time (16 B) [1]	—	—	3.8	µs	—
trd1iphrlv	Read 1s IFR Phrase at low voltage execution time (16 B)	—	—	4.8	µs	—
trdimisr8k	Read IFR into MISR (8 KB) [1]	—	—	50	µs	—
trdimisrk32k	Read IFR into MISR (32 KB) [1]	—	—	190	µs	—
tpgmpg_initial	Program Page execution time at < 1k cycles (128 B) [2]	—	450	600	µs	—
tpgmpg_lifetime	Program Page execution time at < 1k cycles (128 B)	—	450	750	µs	—

Table continues on the next page...

Table 28. Flash command time specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tpgmphr_initial	Program Phrase execution time at > 1k cycles (16 B) [2]	—	135	180	µs	—
tpgmphr_lifetime	Program Phrase execution time at > 1k cycles (16 B)	—	135	225	µs	—
tersall256k	Erase All execution time (256 KB)	—	—	800	ms	—
tersall512k	Erase All execution time (512 KB)	—	—	1500	ms	—
tersall1M	Erase All execution time (1 MB)	—	—	2800	ms	—
tmasers256k	Mass Erase execution time (via sideband) (256 KB)	—	—	800	ms	—
tmasers512k	Mass Erase execution time (via sideband) (512 KB)	—	—	1500	ms	—
tmasers1M	Mass Erase execution time (via sideband) (1 MB)	—	—	2800	ms	—
terrscr	Erase Sector execution time (8 KB) [2]	—	2	22	ms	—
tersall128k	Erase All execution time (128 KB)	—	—	400	ms	—

1. Time to abort the command may significantly impact the time to execute the command.
2. Measured from the time FSTAT[PERDY] is cleared.

4.3.1.2 Flash high voltage current behavior

Table 29. Flash high voltage current behavior

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_IO_PGM	Average current adder to VDD during flash programming operation [1]	—	—	6	mA	—
IDD_IO_ERS	Average current adder to VDD during flash erase operation [1]	—	—	4	mA	—

1. See the Power Management chapter in the reference manual for the specific VDD voltage supply powering the flash array.

4.3.1.3 Flash reliability specifications.

Table 30. Flash reliability specifications.

Symbol	Description	Min	Typ	Max	Unit	Condition
tnvmretp10k	Data retention after up to 10 K cycles	10	50	—	years	Program Flash
nnvmcycscr	Sector cycling endurance [1]	10 K	500 K	—	cycles	Program Flash

Table continues on the next page...

Table 30. Flash reliability specifications. (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
Tnvmretp1k	Data retention after up to 1 K cycles	20	100	—	years	Program Flash
Tnvmretp100k	Data retention after up to 100 K cycles	5	50	—	years	Program Flash
Nnvmcyc256k	Sector cycling endurance for 256 KB [2]	100 K	500 K	—	Cycles	Program Flash

1. Sector cycling endurance represents the number of Program/Erase cycles on a single sector at -40°C ≤ Tj ≤ 125°C.
2. For devices with a single flash block, sectors must be located within the last 256 KB of the flash main memory. For devices with two flash blocks, sectors must be located within the last 256 KB of each flash main memory but must not total more than 256 KB per device.

NOTE

Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile.

4.4 Analog

4.4.1 ADC electrical specifications

ADC operating conditions apply when the ADC is used in differential mode.

All other ADC channels meet the 12-bit single-ended accuracy specifications.

4.4.1.1 ADC operating conditions

Table 31. ADC operating conditions

Symbol	Description	Min	Typ	Max	Unit	Condition
VDDAD	Supply voltage	1.71	—	3.6	V	—
VSSAD	Ground voltage	-0.1	0	0.1	V	—
ΔVDD	— [1]	-0.1	0	0.1	V	—
ΔVSS	— [1]	0.1	0	0.1	V	—
VREFH	Reference Voltage High [2]	0.99	VDDAD	VDDAD	V	—
VREFL	Reference Voltage Low [3]	VSSAD	VSSAD	VSSAD	V	—
VADIN	Input Voltage [3,4,5]	VREFL	—	VREFH	V	—
FADCK	ADC conversion clock frequency	6	—	24	MHz	Low-power mode, PWRSEL=0
FADCK	ADC conversion clock frequency	6	—	60	MHz	Normal Mode, 16b, PWRSEL=1
FADCK	ADC conversion clock frequency	6	—	64	MHz	Normal Mode, 12b , PWRSEL=1
RAS	Analog source resistance (external) [6]	—	—	5	kΩ	—

Table continues on the next page...

Table 31. ADC operating conditions (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
RADIN	Input Resistance ADC channels 7:0 [7,8]	—	—	1.65	kΩ	VDDAD ≥ 1.71 V
RADIN	Input Resistance ADC channels 7:0 [7,8]	—	—	1.525	kΩ	VDDAD ≥ 2.1 V
RADIN	Input Resistance ADC channels 7:0 [7,8]	—	0.925	1.35	kΩ	VDDAD ≥ 2.5 V
CADIN	Input Capacitance	—	1.92	2.4	pF	—

1. DC potential difference
2. Minimum VDDAD/VREFH is 2.4 V in high-speed mode
3. For devices that do not have a dedicated VREFL and VSS_ANA pins, VREFL and VSS_ANA are tied to VSS internally.
4. ADC selected inputs and unselected dedicated inputs must not exceed VDD_ANA during an ADC conversion. Unselected muxed inputs may exceed VDD_ANA but must not exceed the IO supply associated with the inputs (VDD) when a conversion is in progress. If an ADC input may exceed these levels, then a minimum of 1 K series resistance must be used between the source and the ADC input pin.
5. If VREFH is less than VDD_ANA, then voltage inputs greater than VREFH but less than VDD_ANA are allowed but result in a full-scale conversion result
6. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible.
7. If the input come through a mux in the IO pad, add the IO Mux Resistance Adder value to the resistance for the channel type
8. There are several types of ADC inputs. To see which channels correspond to which type of ADC inputs, see channel index map in reference manual

4.4.1.2 I/O mux resistance table

Table 32. I/O mux resistance table

Symbol	Description	Min	Typ	Max	Unit	Condition
RIOMUX	I/O MUX Resistance	—	—	5.35	kΩ	VDD ≥ 1.71v
RIOMUX	I/O MUX Resistance	—	—	1	kΩ	VDD ≥ 2.1v
RIOMUX	I/O MUX Resistance	—	0.35	0.66	kΩ	VDD ≥ 2.5 v

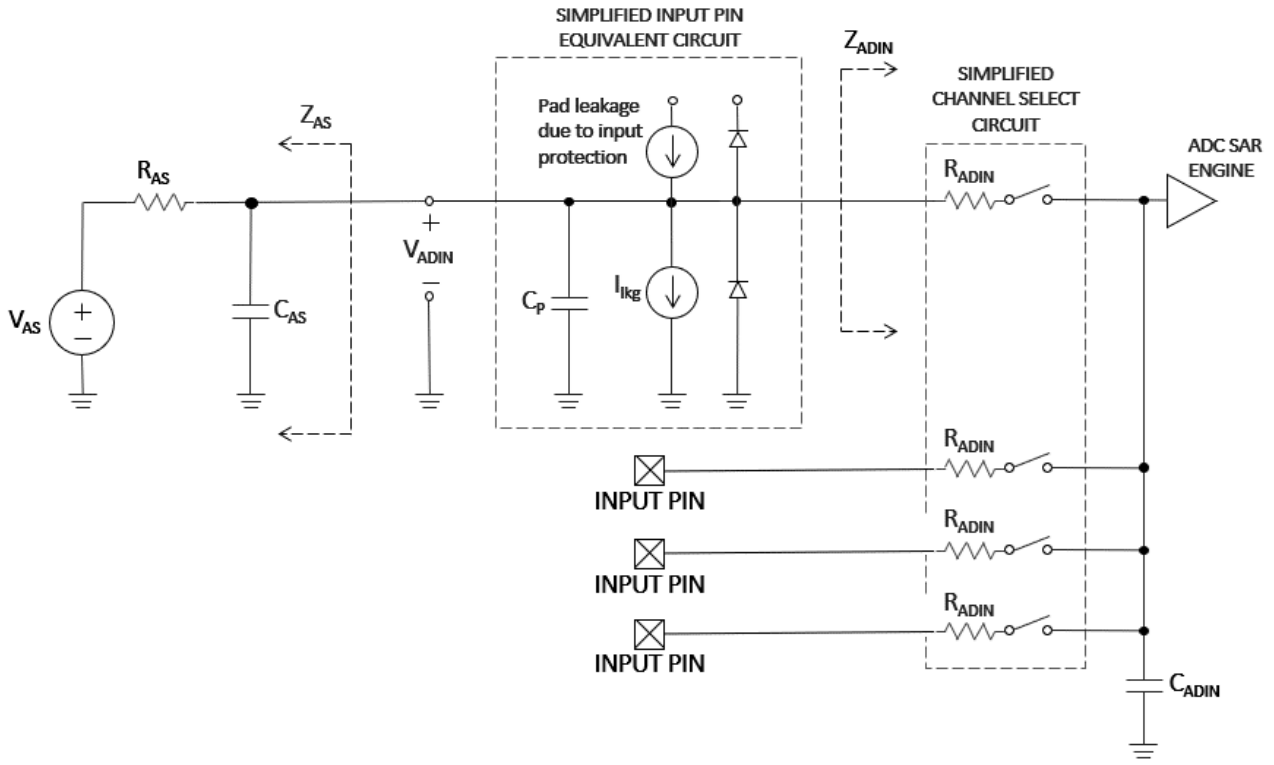


Figure 12. ADC input impedance equivalency diagram

4.4.1.3 ADC electrical characteristics

Table 33. ADC electrical characteristics

Symbol	Description	Min	Typ	Max	Unit	Condition
—	Supply current [1]	—	7	—	—	PWREN=0, Conversions triggered at 10 kS/s
IDDAD	Supply current [1]	—	60	—	μA	PWREN=1, No Conversions
IDDAD	Supply current [1]	—	200	—	μA	Low-power mode, 6 MHz Clock, PWRSEL=0
IDDAD	Supply current [1]	—	230	—	μA	Low-power mode, 24 MHz clock, PWRSEL=0
IDDAD	Supply current [1]	—	550	—	μA	Normal Mode, 60 MHz, PWRSEL=1

Table continues on the next page...

Table 33. ADC electrical characteristics (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
IDDAD	Supply cuurent	—	625	—	µA	High Speed Mode, 60 MHz Clock, PWRSEL=1, HS=1
IDDTS	Temp Sensor Supply Current	—	50	—	µA	Temperature Sensor Adder
CSMP	ADC Sample cycles [2]	3.5	—	131.5	cycles	Low-power mode and High speed mode
Fconv	ADC conversion rate [3]	—	—	4.0	MS/s	12b mode, (HS=1)
Fconv	ADC conversion rate [4]	—	—	3.0	MS/s	16b mode, (HS=1)
TSMP_REQ	Required Sample Time [5]	—	—	—	ns	Use equation based on RAS, RIOMUX, RADIN, CADIN, RAS, CAS, CP and desired accuracy (B)
TSMP	Sample Time [6]	145.8	TSMP_REQ	—	ns	Low-power mode
TSMP	Sample Time [7]	58.3	TSMP_REQ	—	ns	High-speed 16b mode
TSMP	Sample Time [8]	54.7	TSMP_REQ	—	ns	High-speed 12b mode
TSMPINT	Internal channel sample time inputs [9]	2.0	—	—	µs	—
DNL	Differential non-linearity [10,11]	—	±1	—	12b LSB	—
INL	Integral non-linearity [10,11]	—	±1	—	12b LSB	—
ZSE	Zero-scale error (V_ADIN = V_REFL) [10,11]	—	±1	—	12b LSB	—
FSE	Full-scale error (V_ADIN = V_REFH) [10,11]	—	±2	—	12b LSB	—
TUE	Total Unadjusted Error [10,11]	—	±3	—	12b LSB	—
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [11,12]	—	14.1	—	bits	23.4 kS/s (FADCK = 60 MHz, HS =1, AVGS=0111)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input [11,12]	—	13.2	—	bits	187 kS/s (FADCK = 60 MHz, HS=1, AVGS =0100)
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	12.6	—	bits	750 kS/s (FADCK = 60 MHz, HS=1, AVGS =0010)

Table continues on the next page...

Table 33. ADC electrical characteristics (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
ENOB16	Effective number of bits, 16b Mode, 1 kHz input	—	12.0	—	bits	3.0 MS/s (FADCK = 60 MHz, HS=1, AVGS =0000)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [11,12]	—	11.5	—	bits	1.0 MS/s (FADCK = 64 MHz, HS =1, AVGS=0010)
ENOB12	Effective number of bits, 12b Mode, 1 kHz input [11,12]	—	11.0	—	bits	4.0 MS/s (FADCK = 64 MHz, HS =1,AVGS=0000)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [11,12]	—	86.6	—	dB	23.4 kS/s (FADCK=60 MHz, HS=1, AVGS=0111)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [11,12]	—	81.2	—	dB	187.5 kS/s (FADCK=60 MHz, HS=1, AVGS=0100)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input [11,12]	—	77.6	—	dB	750 kS/s (FADCK=60MHz, HS=1, AVGS=0010)
SNDR16	Signal-to-noise plus distortion, 16b Mode, 1 kHz input	—	74	—	dB	3.0 MS/s (FADCK=60 MHz, HS=1, AVGS=0000)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [11,12]	—	71.0	—	dB	1.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0010)
SNDR12	Signal-to-noise plus distortion, 12b Mode, 1 kHz input [11,12]	—	68.0	—	dB	4.0 MS/s (FADCK=64 MHz, HS=1, AVGS=0000)
SFDR	Spurious free dynamic range [11,12]	—	88.0	—	dB	12b/16b Mode, 1kHz input, AVGS =0010
SFDR	Spurious free dynamic range [11,12]	—	82.0	—	dB	12b/16b Mode, 1kHz input, AVGS =0000
Tsu	Start-up time [13]	5	—	—	µs	—
E_TS	Temperature sensor error [14]	—	±1	±3	˚C	Tj=-40 to 105 ˚C
E_TS	Temperature sensor error [14]	—	±2	±4	˚C	Tj=-40 to 125 ˚C
A	Temp Sensor Slope Constant [15]	—	738	—	˚C	—
B	Temp Sensor Offset Constant [15]	—	287.5	—	˚C	—
α	Temp Sensor Bandgap Constant [15]	—	10.06	—	˚C	—

1. The ADC supply current depends on the ADC conversion clock speed, conversion rate, and power mode. Typical value show is at 6 MHz, 24 MHz, and 48 MHz. For lowest power operation, PWRSEL should be set to 00.
2. Must meet minimum TSMP requirement
3. fADCK=64 MHz (HS Mode)

4. fADCK=60 MHz (HS Mode)
5. Required sample time is dictated by external components RAS, CAS, internal components RADIN, CADIN, CP, and desired sample accuracy in bits (B). Calculate it with formula: TSMP_REQ = B*ln(2)*[RAS*(CAS+CP)+ (RAS + RIOMUX + RADIN)* CADIN(typ). RIOMUX=0 unless the ADC input channel goes through an analog mux in the IO”
6. Min based on 3.5 cycles
7. Min based on 3.5 cycles @ 60 MHz
8. Min based on 3.5 cycles @ 64 MHz
9. Internal channel inputs are those that do not come from external source (temperature sensor, bandgap).
10. 1 LSB = (VREFH - VREFL)/2N (N=14 bits), for 16- bit specifications, multiply by 4.
11. All accuracy numbers assume that the ADC is calibrated with VREFH=VDD_ANA and using a high- speed- dedicated input channel. Typical values assume VDD_ANA = 3.0 V, Temp = 25 °C, fADCK = 24 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
12. Dynamic results assume Fin=1 kHz sinewave, no averaging unless otherwise specified
13. Delay required if PWREN=0
14. The temperature sensor can be calibrated to a +/- 1 % precision after board assembly by using a 3-temperature calibration flow with accurate ± 0.15 % temperature chamber
15. T(°C) = A*[°α(Vbe8 - Vbe1)/(Vbe8 + α(Vbe8 - Vbe1))] - B where Vbe1 is the first value stored to FIFO as a result of the temperature sensor channel conversion, Vbe8 is the second value stored to FIFO as a result of the temperature sensor channel conversion, A is the slope factor, B is the offset factor, α is the bandgap coefficient

Set the power-up delay (PUDLY) according to the ADC start-up time if PWREN=0.

Ilkg = leakage current (Refer to pin leakage specification in the voltage and current operating behaviours of packaged device)

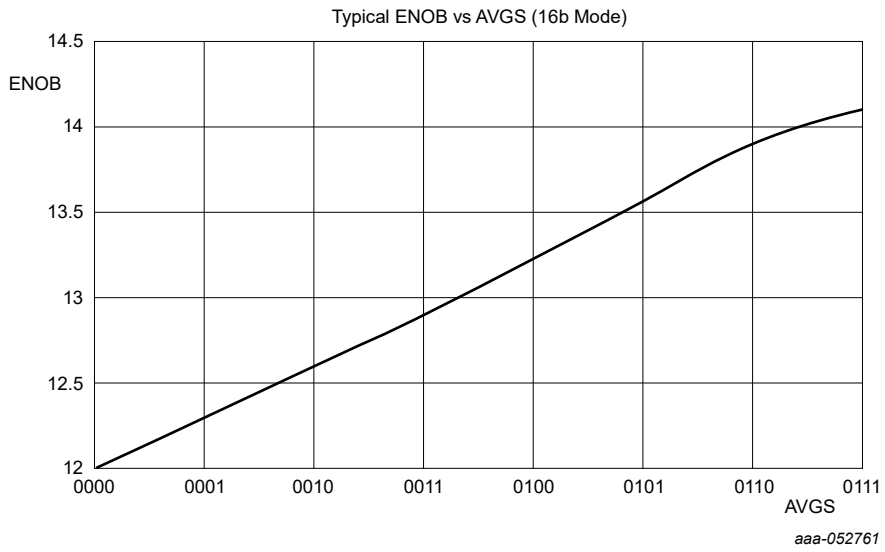


Figure 13. ENOB vs ADC (16b HS Mode)

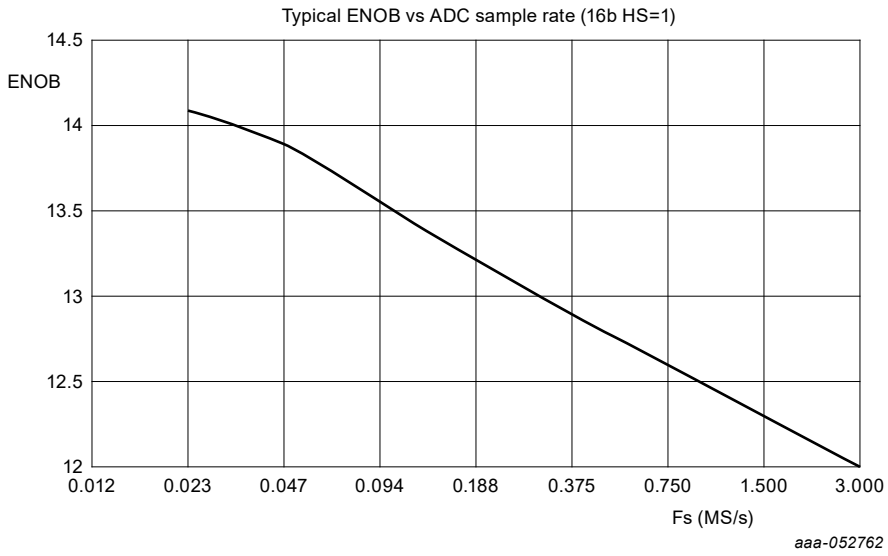


Figure 14. ENOB vs ADC sample rate

4.4.2 12-bit DAC electrical characteristics

4.4.2.1 12-bit DAC operating requirements

Table 34. 12-bit DAC operating requirements

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ANA	Supply voltage	1.71	—	3.6	V	—
VDACR	Reference Voltage [1]	0.97	—	VDD_ANA	V	—
CL	Output load capacitance [2]	—	50	100	pF	—
IL	Output load current [3]	-1	—	1	mA	—
DAC_c_rate	DAC conversion rate	—	—	1	MSPS	—

1. The DAC reference can be selected to be VDD_ANA or VREFH or VREFO PAD, keep VDD_ANA be the highest voltage.
2. A small load capacitance (50 pF) can improve the bandwidth performance of the DAC.
3. Sink or source current availability

4.4.2.2 12-bit DAC operating behaviors

Table 35. 12-bit DAC operating behaviors

Symbol	Description	Min	Typ	Max	Unit	Condition
IDD_DAC	Supply Current	—	300	500	µA	Normal mode
IDD_DAC	Supply Current	—	100	150	µA	Low-power mode
IDD_DAC	Supply Current	—	10	—	nA	Disabled
tDAC	Full-scale settling time (0x100 to 0xF00) [1]	—	2.5	3	µs	Normal mode

Table continues on the next page...

Table 35. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tDAC	Full-scale settling time (0x100 to 0xF00) [1]	—	5	6	µs	Low-power mode
tccDAC	Code-to-code settling time (0xBF8 to 0xC08) [1]	—	0.7	1	µs	—
Vdacoutl	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	—
Vdacouth	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	VDACR-100	—	VDACR	mV	—
INL	Integral non-linearity error [2]	—	—	±3	LSB	—
DNL	Differential non-linearity error [3]	—	—	±1	LSB	—
EOFFSET	Offset error [4]	—	± 0.4	± 0.8	%FSR	—
EG	Gain error [4]	—	± 0.3	± 0.6	%FSR	VDACR < 2.1 V
EG	Gain error [4]	—	± 0.1	± 0.3	%FSR	VDACR > 2.1 V
PSRR	Power supply rejection ratio, VDD_ANA ≥ 2.4 V	—	70	—	dB	—
TCO	Temperature coefficient offset voltage at middle scale [5]	—	—	—	µV/C	—
TEO	Temperature coefficient offset error	—	30	—	µV/C	—
TGE	Temperature coefficient gain error	—	10	—	PPM/C	—
ROP	Output resistance (load = 10 kΩ)	—	200	—	Ω	—
SR	Slew rate 100 h ->F00 h or F00 h ->100 h	—	3.6	—	V/µs	—
SR	Slew rate 100 h ->F00 h or F00 h ->100 h	—	0.5	—	V/µs	—
CT	DAC to DAC crosstalk [6]	—	—	-80	dB	—
TPU	Power-up time	—	2.5	—	µs	—

1. Settling within ±1 LSB measured with a 47 pF load.
2. The INL is measured for 0 + 100 mV to VDACR −100 mV
3. The DNL is measured for 0 + 100 mV to VDACR −100 mV
4. Calculated by a best fit curve from VSS_ANA + 100 mV to VDACR − 100 mV
5. VDD_ANA = 3.0 V, reference select set for VDD_ANA (DACx_CO:DACRFS = 1), high- power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device.
6. If two DACs are used and share same VREFH

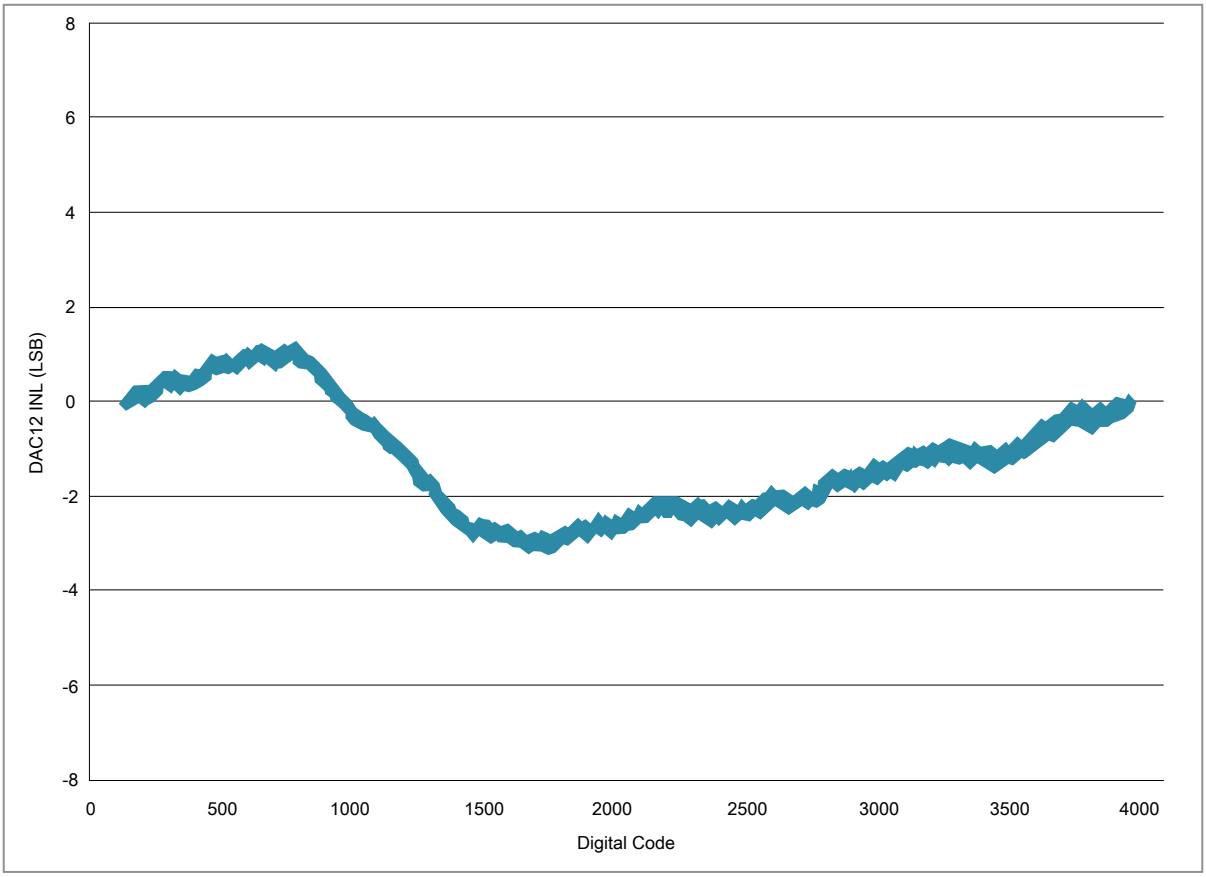


Figure 15. Typical INL error vs. digital code

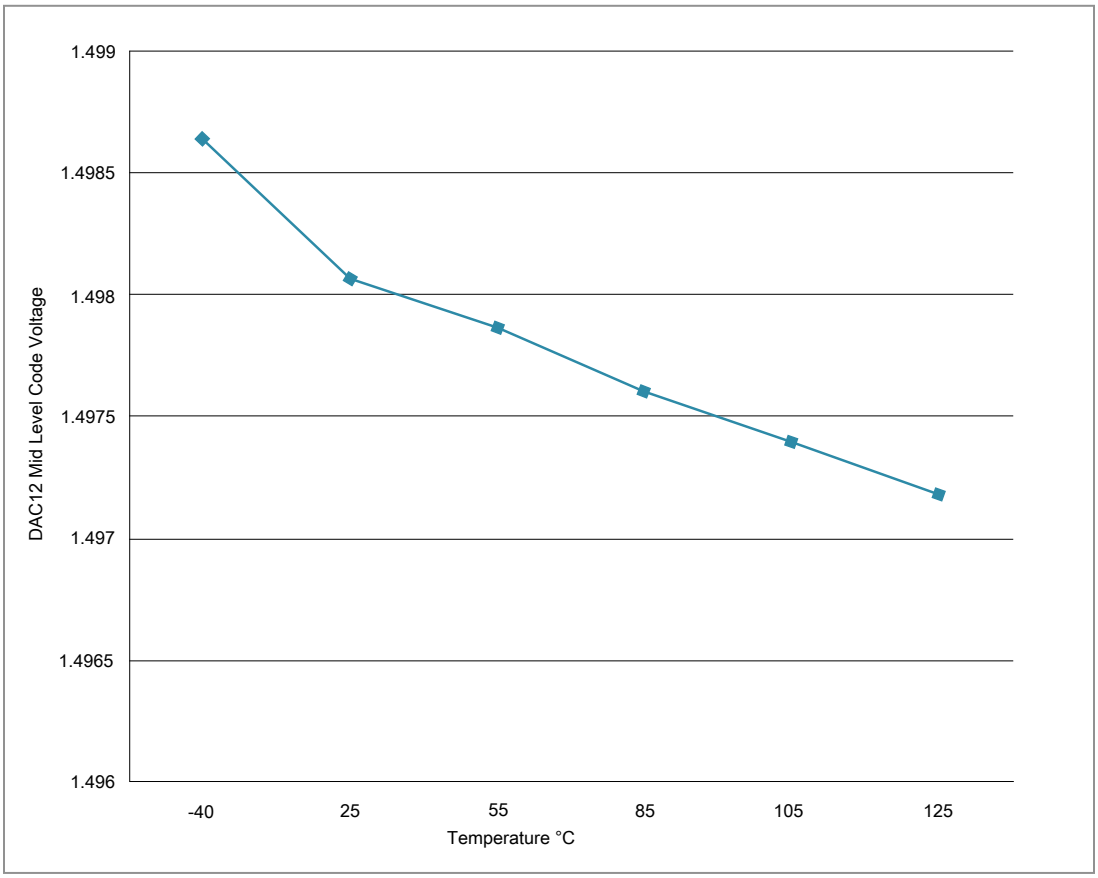


Figure 16. Offset at half scale vs. temperature

4.4.3 Comparator and 8-bit DAC electrical specifications

Table 36. Comparator and 8-bit DAC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD	Supply voltage	1.71	—	3.6	V	—
VREFH	8-bit DAC reference voltage high	0.97	—	VDD	V	—
IDD_CMP	Supply current	—	200	—	µA	High speed mode (EN=1, HPMD=1)
IDD_CMP	Supply current	—	10	—	µA	Normal mode (EN=1, HPMD=0, NPMD=0)
IDD_CMP	Supply current	—	400	—	nA	Low-power mode (EN=1, HPMD=0, NPMD=1)
VAIN	Analog input voltage	VSS	—	VDD	V	—
VAIO	Analog input offset voltage	—	—	20	mV	High speed mode

Table continues on the next page...

Table 36. Comparator and 8-bit DAC electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
VAIO	Analog input offset voltage	—	—	20	mV	Normal mode
VAIO	Analog input offset voltage	—	—	40	mV	Low-power mode
VH	Analog comparator hysteresis [1]	—	0	—	mV	CR0[HYSTCTR] = 00
VH	Analog comparator hysteresis [1]	—	10	—	mV	CR0[HYSTCTR] = 01
VH	Analog comparator hysteresis [1]	—	20	—	mV	CR0[HYSTCTR] = 10
VH	Analog comparator hysteresis [1]	—	30	—	mV	CR0[HYSTCTR] = 11
VCMPOh	Output high	VDD - 0.2	—	—	V	—
VCMPOl	Output low	—	—	0.2	V	—
tD	Propagation delay [2]	—	—	25	ns	High speed mode, 100 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	50	ns	High speed mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	600	ns	Normal mode, 30 mV overdrive, power > 1.71V
tD	Propagation delay [2]	—	—	5	µs	Low-power mode, 30 mV overdrive, power > 1.71V
tinit	Analog comparator initialization delay [3]	—	—	40	µs	—
IDAC8b	8-bit DAC current adder (enabled)	—	10	—	µA	High power mode (EN=1, PMODE=1)
IDAC8b	8-bit DAC current consumption	—	1	—	µA	Low power mode (EN=1, PMODE=0)
INL	8-bit DAC integral non-linearity [4]	-1	—	+1.0	LSB	Low/High power mode, supply power > 1.71V
DNL	8-bit DAC differential non-linearity	-1	—	+1.0	LSB	Low/High power mode, power > 1.71V

1. Typical hysteresis is measured with input voltage range limited to 0.6 to VDD_ANA–0.6 V.
2. Overdrive does not include input offset voltage or hysteresis. The propagation delay is defined as the time delay between the change of the voltage on input pin and the output change of the comparator analog part
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
4. 1 LSB = Vreference/256

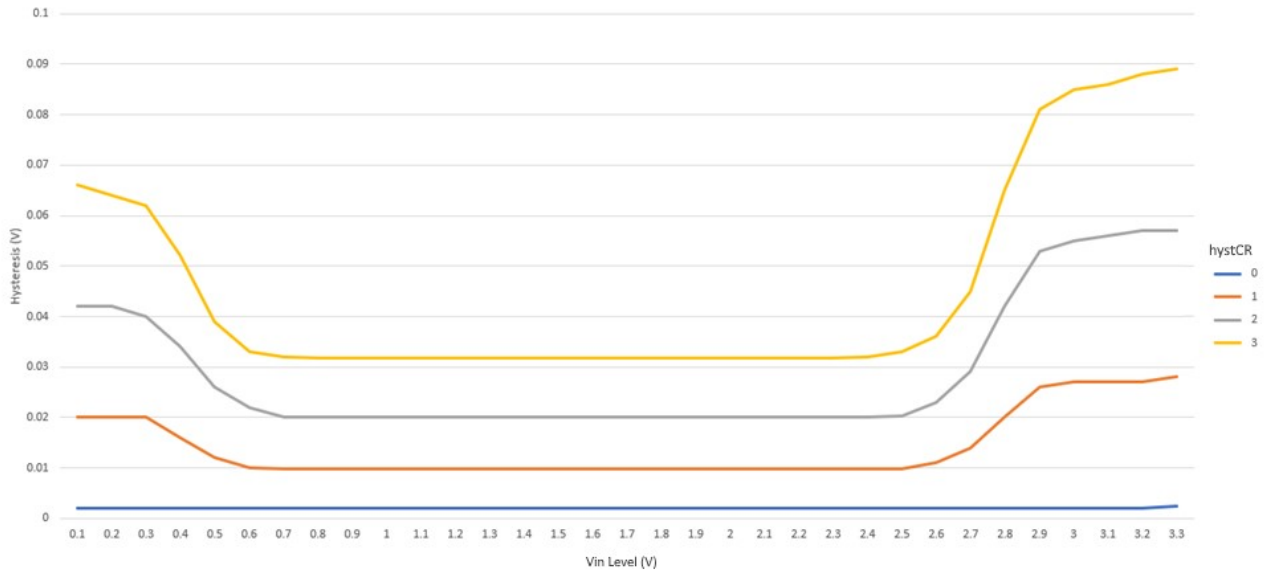


Figure 17. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

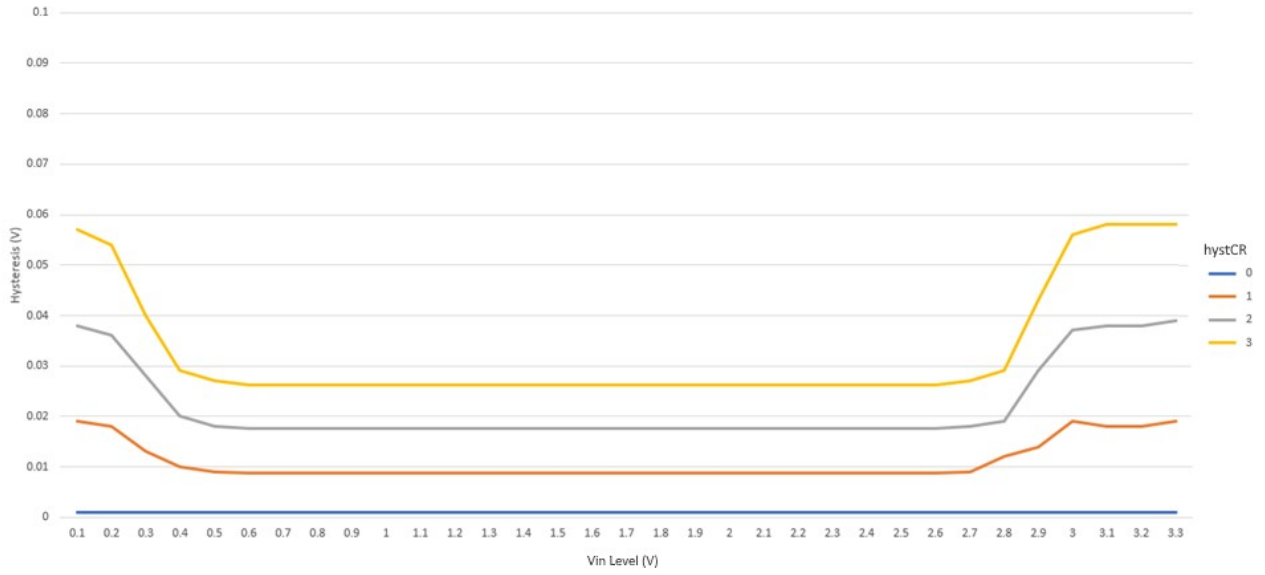


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

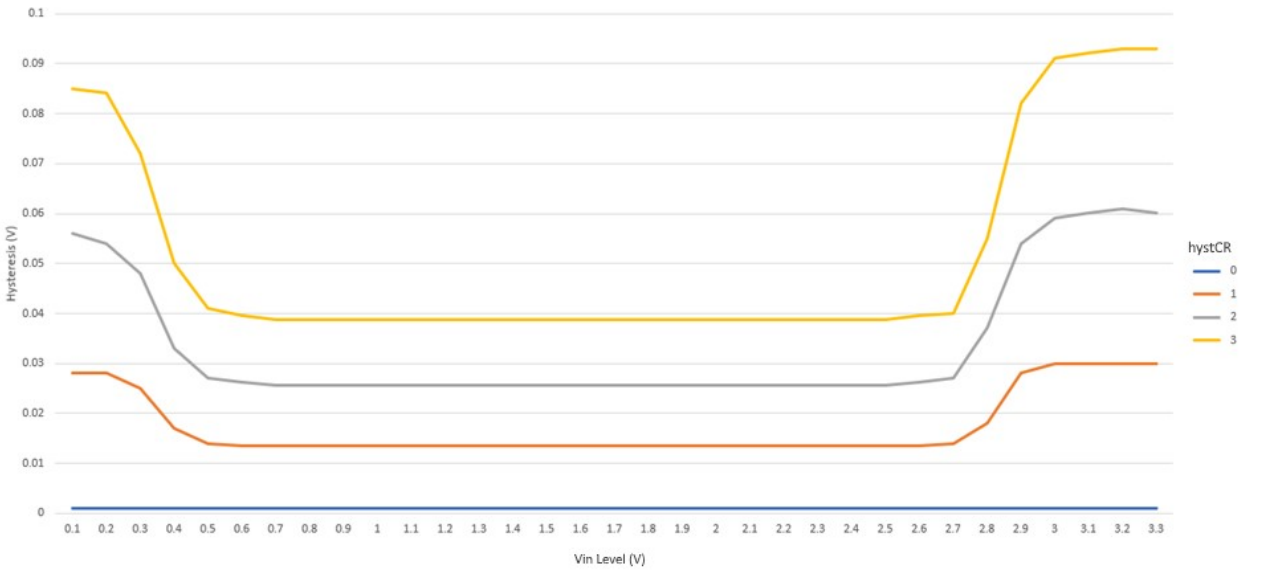


Figure 19. Typical hysteresis vs Vin level (VDD =3.3 V, HPMD = 0, NPMD = 1)

4.4.4 OpAmp electrical specifications

Table 37. OpAmp electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
VDD_ANA	Operating Voltage	1.71	3	3.6	V	—
ISUPPLY1	Supply Current (IOUT=0 mA high-speed mode)	—	450	—	µA	—
ISUPPLY2	Supply Current (IOUT=0 mA high-speed mode)	—	120	—	µA	—
VOS	Input Offset Voltage	-5	—	5	mV	—
αVOS	Input Offset Voltage Temperature Coefficient	—	5	—	µV/C	—
VCML	Input Common Mode Voltage Low	0	—	—	V	—
VCMH	Input Common Mode Voltage High	—	—	VDD_ANA	V	—
PSRR	Power Supply Rejection Ration @ DC	—	80	—	dB	—
SRh	Slew Rate positive (ΔVIN=1 V, high- speed mode)	—	6	—	V/µs	—

Table continues on the next page...

Table 37. OpAmp electrical specifications (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
SRl	Slew Rate positive (ΔVIN=1 V, low- speed mode)	—	1	—	V/µs	—
GBWh	Unity Gain Bandwidth (high-speed mode)	—	6	—	MHz	—
GBWl	Unity Gain Bandwidth (low-speed mode)	—	1	—	MHz	—
AV	DC Open Loop Voltage Gain	—	110	—	dB	—
CL	Load Capacitance Driving Capability	—	—	20	pF	—
RL	Load resistance (low-power mode)	3 K	—	—	Ω	—
PM	Phase Margin	—	60	—	deg	—
Vn	Voltage noise density @1 kHz (high-speed mode)	—	100	—	nv/sqrtHz	—
Vo	Output swing	0.2	—	VDD_ANA-0.2	V	—
Tsettle	Settling time (high-speed mode invert gain=4 input=10 mV with +/-730 µV settling accuracy)	—	1	—	µs	—
Cin	Input Capacitance	—	5	—	pF	—
T_start	Startup Time (high-speed mode buffer with input 1 V)	—	5	—	µs	—

4.4.5 PGA electrical specifications

NOTE

Gain is PGA mode gain and gain is 2.4.8

Table 38. PGA electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
Error gain	PGA gain accuracy	—	±1	—	%	—
—	PGA bandwidth	—	6/(gain+1)	—	MHz	Inverting mode, gain = 1, 2, 4
—	PGA bandwidth	—	32/(gain+1)	—	MHz	Inverting mode, gain = 8, 16, 33, 64
—	PGA bandwidth	—	6/(gain+1)	—	MHz	Non-inverting mode, gain = 1, 2, 4
—	PGA bandwidth	—	32/(gain+1)	—	MHz	Non-inverting mode, gain = 8, 16, 33, 64

4.5 Timers

See General switching specifications.

4.6 Communication Interfaces

4.6.1 LPUART

The Low Power Universal Asynchronous Receiver / Transmitter (LPUART) provides an asynchronous serial bus with master and slave operations, can reach to 24Mbps maximum transfer rate, based on characterization but not covered by test limits in production. See General switching specifications.

4.6.2 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

4.6.2.1 LPSPI master mode timing

Table 39. LPSPI master mode timing

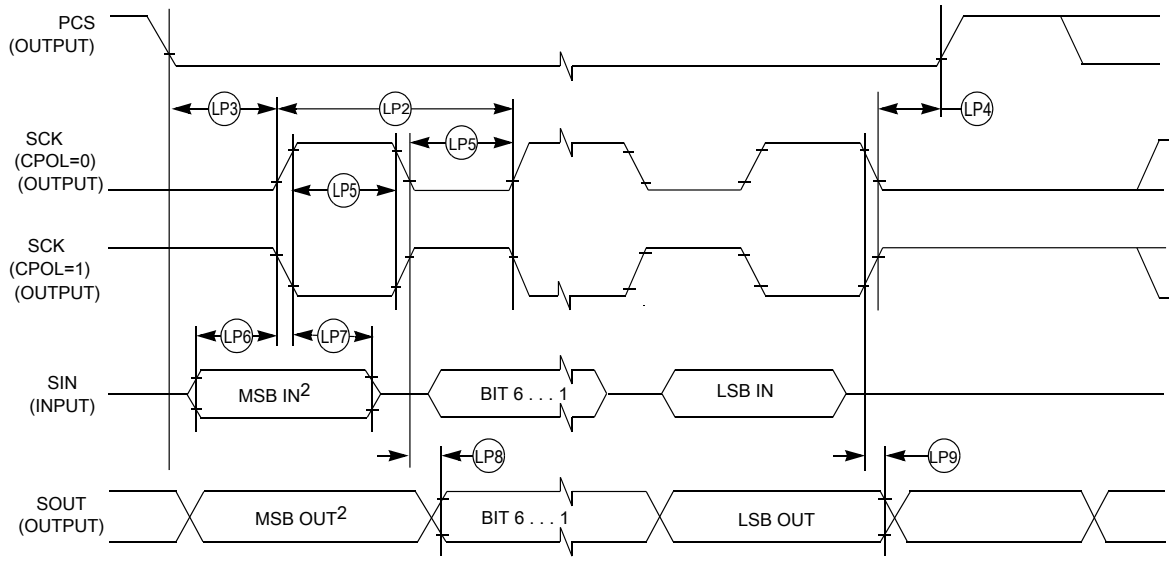
Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation [1]	—	—	—	MHz	—
LP1	LPSPI0 ~ LPSPI1 medium speed pad	—	—	48	MHz	Master in SD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad	—	—	24	MHz	Master in SD mode
LP1	LPSPI0 ~ LPSPI1 medium speed pad	—	—	24	MHz	Master in MD mode
LP1	LPSPI0 ~ LPSPI1 slow speed pad	—	—	24	MHz	Master in MD mode
LP2	SPSCK period	1000/LP1	—	—	ns	—
LP3	Enable lead time [2]	1/2	—	—	tperiph	—
LP4	Enable lag time [2]	1/2	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSCK/2-3	—	tSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	LPSPI0 ~ LPSPI1 medium speed pad	7.2	—	—	ns	Master in SD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad	14.4	—	—	ns	Master in SD mode
LP6	LPSPI0 ~ LPSPI1 medium speed pad	14.4	—	—	ns	Master in MD mode
LP6	LPSPI0 ~ LPSPI1 slow speed pad	14.4	—	—	ns	Master in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—

Table continues on the next page...

Table 39. LPSPI master mode timing (continued)

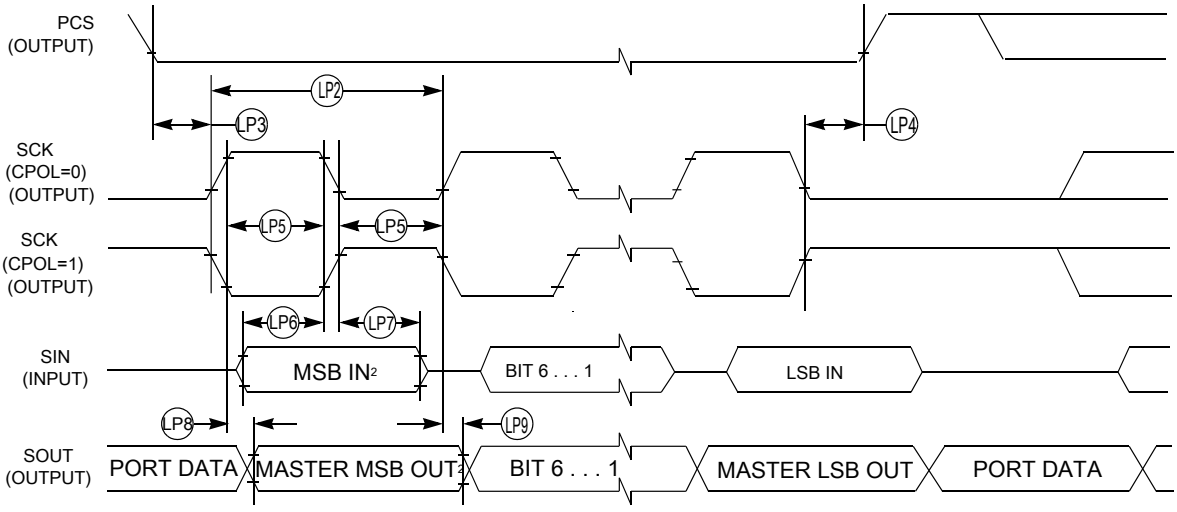
Symbol	Description	Min	Typ	Max	Unit	Condition
LP7	LPSPI0 ~ LPSPI1 medium speed pad	0	—	—	ns	Master in SD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad	0	—	—	ns	Master in SD mode
LP7	LPSPI0 ~ LPSPI1 medium speed pad	0	—	—	ns	Master in MD mode
LP7	LPSPI0 ~ LPSPI1 slow speed pad	0	—	—	ns	Master in MD mode
LP8	Data valid (after SPSCK edge)	—	—	—	ns	—
LP8	LPSPI0 ~ LPSPI1 medium speed pad	—	—	7.2	ns	Master in SD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad	—	—	14.4	ns	Master in SD mode
LP8	LPSPI0 ~ LPSPI1 medium speed pad	—	—	14.4	ns	Master in MD mode
LP8	LPSPI0 ~ LPSPI1 slow speed pad	—	—	14.4	ns	Master in MD mode
LP9	Data hold time (outputs)	—	—	—	ns	—
LP9	LPSPI0 ~ LPSPI1 medium speed pad	—	—	-1	ns	Master in SD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad	—	—	-1	ns	Master in SD mode
LP9	LPSPI0 ~ LPSPI1 medium speed pad	—	—	-1	ns	Master in MD mode
LP9	LPSPI0 ~ LPSPI1 slow speed pad	—	—	-1	ns	Master in MD mode

1. The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/2, where fperiph is the LPSPI peripheral functional clock.
2. tperiph = 1/fperiph



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 20. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 21. LPSPI master mode timing (CPHA = 1)

4.6.2.2 LPSPI slave mode timing

Table 40. LPSPI slave mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	Frequency of operation in OD mode [1]	—	—	—	—	—
LP1	lpspi0~lpspi1 medium speed pad [1]	—	—	24	MHz	Slave Tx in SD mode

Table continues on the next page...

Table 40. LPSPI slave mode timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
LP1	lpspi0~lpspi1 slow speed pad [1]	—	—	12	MHz	Slave Tx in SD mode
LP1	lpspi0~lpspi1 medium speed pad [1]	—	—	48	MHz	Slave Rx in SD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	24	MHz	Slave Rx in SD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Slave Tx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Slave Tx in MD mode
LP1	lpspi0~lpspi1 medium speed pad	—	—	12	MHz	Slave Rx in MD mode
LP1	lpspi0~lpspi1 slow speed pad	—	—	12	MHz	Slave Rx in MD mode
LP2	SPSCK period	4 x tperiph	—	2048 x tperiph	ns	—
LP3	Enable lead time [2]	1	—	—	tperiph	—
LP4	Enable lag time [2]	1	—	—	tperiph	—
LP5	Clock (SPSCK) high or low time	tSPSCK/2 - 5	—	tSPSCK/2	ns	—
LP6	Data setup time (inputs)	—	—	—	ns	—
LP6	lpspi0~lpspi1 medium speed pad	3.6	—	—	ns	Slave Rx in SD mode
LP6	lpspi0~lpspi1 slow speed pad	7.2	—	—	ns	Slave Rx in SD mode
LP6	lpspi0~lpspi1 medium speed pad	14.4	—	—	ns	Slave Rx in MD mode
LP6	lpspi0~lpspi1 slow speed pad	14.4	—	—	ns	Slave Rx in MD mode
LP7	Data hold time (inputs)	—	—	—	ns	—
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Slave Rx in SD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Slave Rx in SD mode
LP7	lpspi0~lpspi1 medium speed pad	0	—	—	ns	Slave Rx in MD mode
LP7	lpspi0~lpspi1 slow speed pad	0	—	—	ns	Slave Rx in MD mode
LP8	Slave access time [2,3]	—	—	tperiph	ns	—
LP9	Slave MISO disable time [2,4]	—	—	tperiph	ns	—
LP10	Data valid (after SPSCK edge)	—	—	—	ns	—
LP10	lpspi0~lpspi1 medium speed pad	—	—	15.6	ns	Slave Tx in SD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	31.2	ns	Slave Tx in SD mode

Table continues on the next page...

Table 40. LPSPI slave mode timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
LP10	lpspi0~lpspi1 medium speed pad	—	—	31.2	ns	Slave Tx in MD mode
LP10	lpspi0~lpspi1 slow speed pad	—	—	31.2	ns	Slave Tx in MD mode
LP11	Data hold time (outputs)	—	—	—	ns	—
LP11	lpspi0~lpspi1 medium speed pad	—	—	-1	ns	Slave Tx in SD mode
LP11	lpspi0~lpspi1 slow speed pad	—	—	-1	ns	Slave Tx in SD mode
LP11	lpspi0~lpspi1 medium speed pad	—	—	-1	ns	Slave Tx in MD mode
LP11	lpspi0~lpspi1 slow speed pad	—	—	-1	ns	Slave Tx in MD mode

1. The frequency of operation is also limited to a minimum of fperiph/2048 and a max of fperiph/4, where fperiph is the LPSPI peripheral functional clock.
2. tperiph = 1/fperiph
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

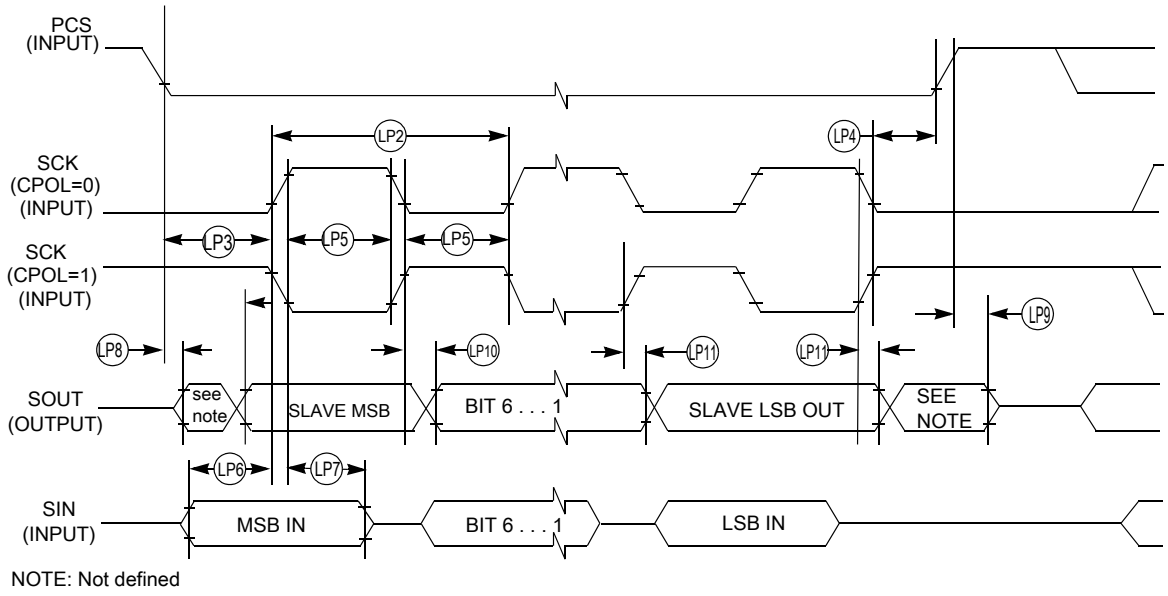


Figure 22. LPSPI slave mode timing (CPHA = 0)

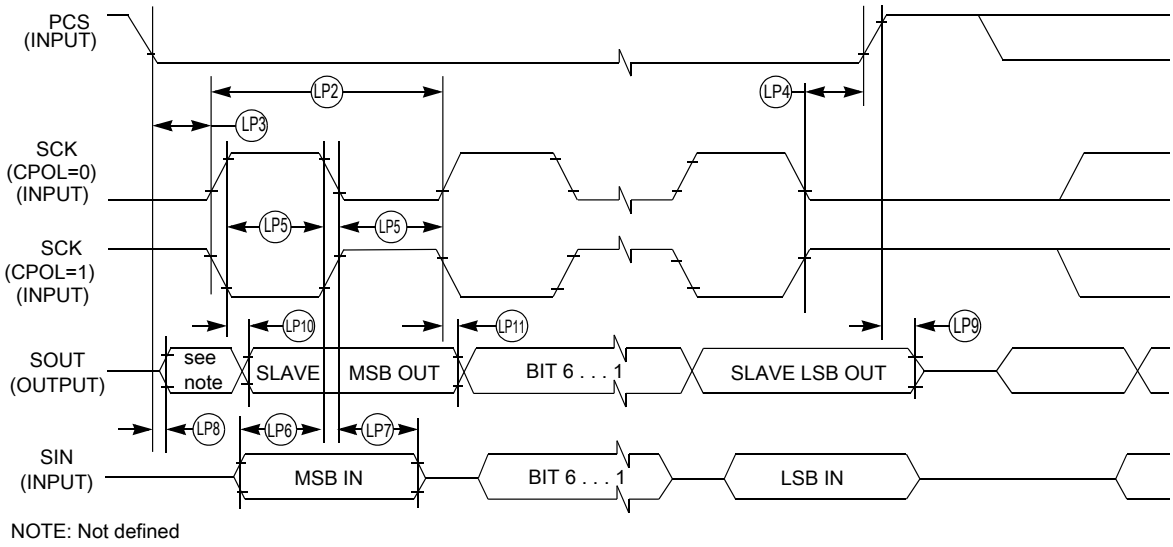


Figure 23. LPSPI slave mode timing (CPHA = 1)

4.6.3 LPI2C timing

Table 41. LPI2C timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency in standard mode	0	—	100	kHz	—
fSCL	SCL Clock Frequency in fast mode	0	—	400	kHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in standard mode	4	—	—	µs	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated in fast mode	0.6	—	—	µs	—
tLOW	LOW period of the SCL clock in standard mode	4.7	—	—	µs	—
tLOW	LOW period of the SCL clock in fast mode	1.25	—	—	µs	—
tHIGH	HIGH period of the SCL clock in standard mode	4	—	—	µs	—
tHIGH	HIGH period of the SCL clock in fast mode	0.6	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition in standard mode	4.7	—	—	µs	—

Table continues on the next page...

Table 41. LPI2C timing (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tSU; STA	Set-up time for a repeated START condition in fast mode	0.6	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices in standard mode [1,2]	0	—	3.45	µs	—
tHD; DAT	Data hold time for I2C bus devices in fast mode [1,3]	0	—	0.9	µs	—
tSU; DAT	Data set-up time in standard mode [4]	250	—	—	ns	—
tSU; DAT	Data set-up time in fast mode [2,5]	100A	—	—	ns	—
tr	Rise time of SDA and SCL signals in standard mode [6]	—	—	1000	ns	—
tr	Rise time of SDA and SCL signals in fast mode [6]	20 +0.1Cb	—	300	ns	—
tf	Fall time of SDA and SCL signals in standard mode [5]	—	—	300	ns	—
tf	Fall time of SDA and SCL signals in fast mode [5]	20 +0.1Cb	—	300	ns	—
tSU; STO	Set-up time for STOP condition in standard mode	4	—	—	µs	—
tSU; STO	Set-up time for STOP condition in fast mode	0.6	—	—	µs	—
tBUF	Bus free time between STOP and START condition in standard mode	4.7	—	—	µs	—
tBUF	Bus free time between STOP and START condition in fast mode	1.3	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter in standard mode	N/A	—	N/A	ns	—
tSP	Pulse width of spikes that must be suppressed by the input filter in fast mode	0	—	50	ns	—

1. The master mode I2C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum tHD; DAT must be met only if the device does not stretch the LOW period (tLOW) of the SCL signal
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I2C bus device can be used in a Standard mode I2C bus system, but the requirement tSU; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line trmax + tSU; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I2C bus specification) before the SCL line is released.

6. Cb = total capacitance of the one bus line in pF.

4.6.4 I2C 1 Mbps timing

Table 42. I2C 1 Mbps timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	1	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	HIGH period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices	0	—	—	µs	—
tSU; DAT	Data set-up time	50	—	—	ns	—
tr	Rise time of SDA and SCL signals [1]	20 +0. 1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [1]	20 +0. 1Cb	—	120	ns	—
tSU; STO	Set-up time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

1. Cb = total capacitance of the one bus line in pF for maximum value

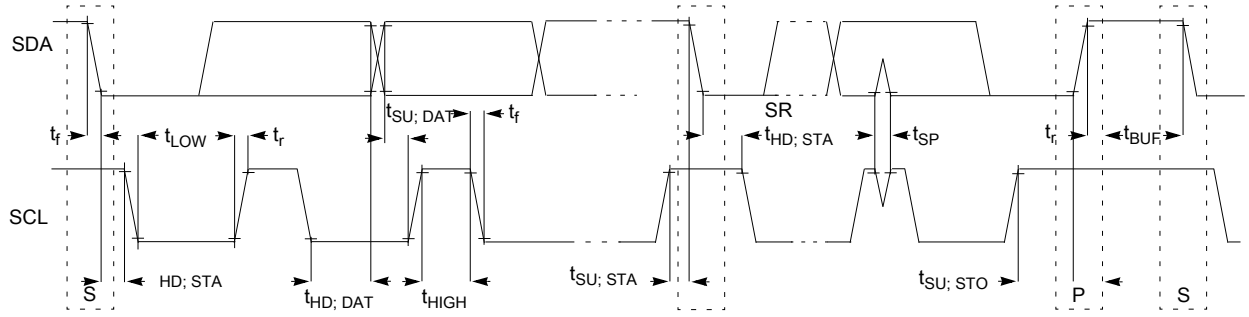


Figure 24. Timing definition for devices on the I2C bus

4.6.5 I2C HS mode timing

Table 43. I2C HS mode timing

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0	—	3.4	MHz	—
tHD; STA	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26	—	—	µs	—
tLOW	LOW period of the SCL clock	0.5	—	—	µs	—
tHIGH	High period of the SCL clock	0.26	—	—	µs	—
tSU; STA	Set-up time for a repeated START condition	0.26	—	—	µs	—
tHD; DAT	Data hold time for I2C bus devices [1]	0	—	—	µs	—
tSU; DAT	Data setup time	34	—	—	ns	—
tr	Rise time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tf	Fall time of SDA and SCL signals [2]	20 +0.1Cb	—	120	ns	—
tSU; STO	Setup time for STOP condition	0.26	—	—	µs	—
tBUF	Bus free time between STOP and START condition	0.5	—	—	µs	—
tSP	Pulse width of spikes that must be suppressed by the input filter	0	—	50	ns	—

1. A device must internally provide a data hold time to bridge the undefined part between VIH and VIL of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time in maximum value.
2. Cb = total capacitance of the one bus line in pF. The max Cb value is 50 pF. Applicable for maximum value.

NOTE

Only PTB4/5, PTA18/19, PTC0/1, PTC4/5 pin can support Fast+ (3 MHz) mode.

4.6.6 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pf, input transition of 1 ns. GPIO-Standard-plus pad configured with DSE = 1'b1 and GPIO-Medium pad with DSE = 1'b1 and SRE = 1'b1. SCL, SDA and PUR combination should be of same pad type. For e.g. I3C medium Data Pads to be used with I3C Medium Clock and PUR Pads Only. I3C Standard plus Data Pads to be used with I3C standard plus Clock and PUR pads only.

Table 44. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0.01	12.5	12.9	MHz	FSCL = 1 / (tDIG_L + tDIG_H)
tDIG_L	SCL Clock Low Period [1,2]	32	—	—	ns	—

Table continues on the next page...

Table 44. I3C Push-Pull Timing Parameters for SDR Mode (continued)

Symbol	Description	Min	Typ	Max	Unit	Condition
tDIG_H	SCL Clock High Period [2]	32	—	—	ns	—
tSCO	Clock in to Data Out for Slave [3,4]	—	—	12	ns	—
tCR	SCL Clock Rise Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tCF	SCL Clock Fall Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Slave [6]	0	—	—	—	Applicable for slave and master loopback modes
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	N/A	ns	Applicable for slave and master loopback modes.

1. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.
2. tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
3. Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Master to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.
4. Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Master may be a Slave in a multi-Master system, and thus shall also adhere to this requirement
5. The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
6. tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Master mode vs. Slave mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

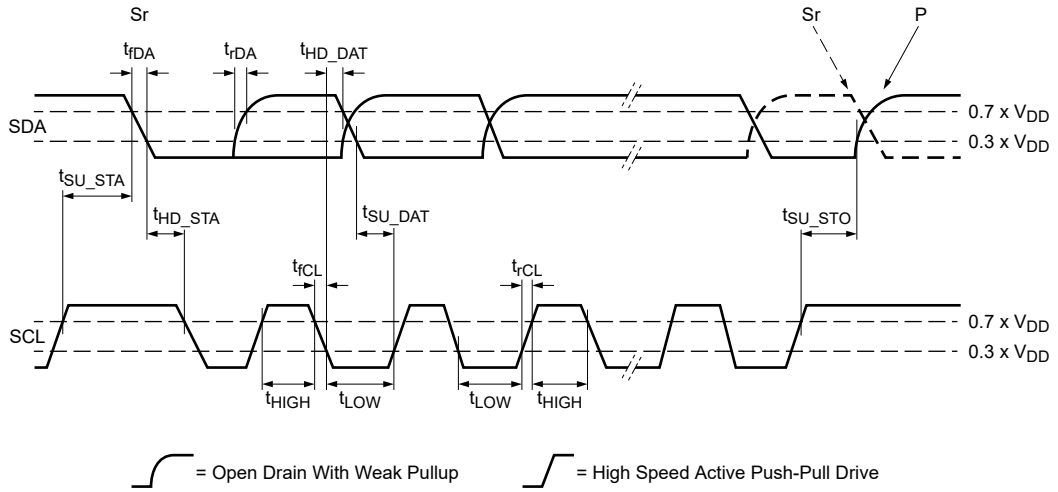


Figure 25. Legacy mode timing

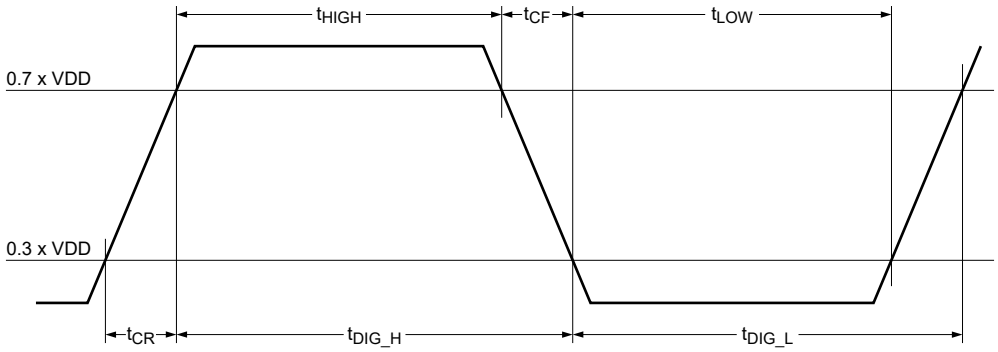


Figure 26. tDIG_H and tDIG_L

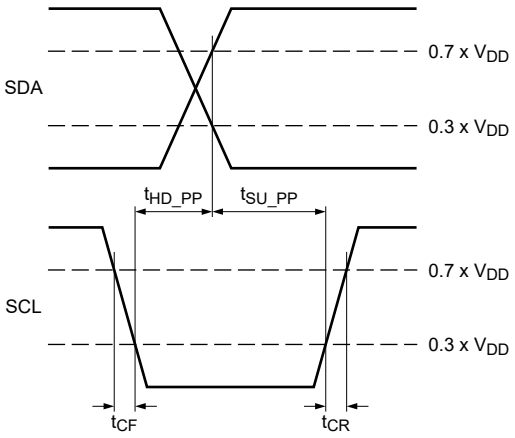


Figure 27. Master out timing

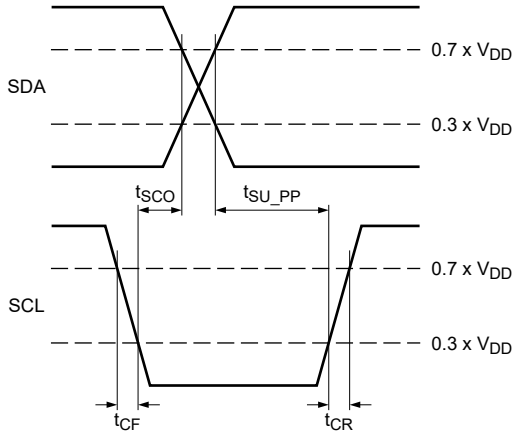


Figure 28. Slave out timing

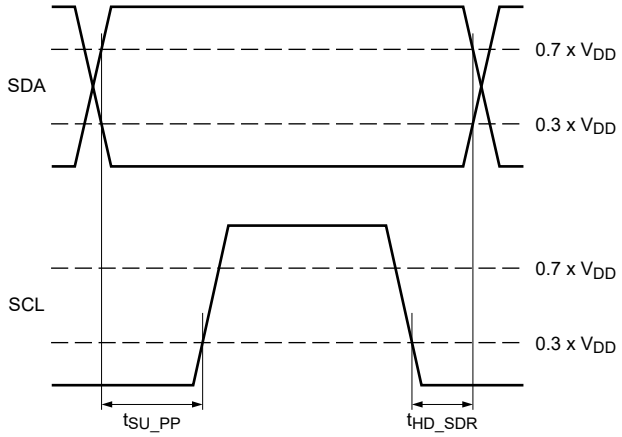


Figure 29. Master SDR timing

4.6.7 USB Full-speed device electrical specifications

This section describes the USB0 port Full Speed/Low Speed transceiver. The USB0 (FS/LS Transceiver) meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 Specification with the amendments below.

- USB ENGINEERING CHANGE NOTICE
  - Title: 5 V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0

This SoC does not have a dedicated pin to monitor the state of the USB VBUS signal. Please refer to the USBFS chapter in the Reference Manual for methods which can be used for VBUS Session_Valid detection with either a P4-12/ALT1 pin using an external resistive divider.

4.6.8 FlexCAN

See General switching specifications.

4.6.9 Flexible I/O controller (FLEXIO) electrical specifications

The following table shows FlexIO timing specifications.

Table 45. Flexible I/O controller (FLEXIO) electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Condition
tODS	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	8	ns	—
tIDS	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	8	ns	—

4.7 Human Machine Interface (HMI) modules

4.7.1 General Purpose Input/Output (GPIO)

See General switching specifications.

5 Package dimensions

5.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
LQFP100	98ASS23308W
LFBGA64	98ASA02085D
VFBGA112	98ASA02081D

6 Pinout

6.1 MCXA156, A155, A154, A146, A145, A144 Signal Multiplexing and Pin Assignments

The signal multiplexing and pin assignments are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.

2. Double-click on the Excel file to open it.
3. Select the “Pinout” tab.

The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

However the pinout table is as given below

Table 46. Pinout

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
P1_8	A1	1	B2	**ALT0** - P1_8 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPUART1_RXD **ALT3** - LPI2C2_SDA **ALT4** - CT_INP8 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D16 **ALT10** - I3C0_SDA	**IO Supply** - VDD **Pad type** - HD+I3C **Default** - DIS	**ISP** - I2C_SDA **VDD SYS** - WUU0_IN10
P1_9	B1	2	C2	**ALT0** - P1_9 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPUART1_TXD **ALT3** - LPI2C2_SCL **ALT4** - CT_INP9 **ALT5** - CT0_MAT3 **ALT6** - FLEXIO0_D17 **ALT10** - I3C0_SCL	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ISP** - I2C_SCL
P1_10	C3	3	D2	**ALT0** - P1_10 **ALT2** - LPUART1_RTS_B **ALT3** - LPI2C2_SDAS **ALT4** - CT2_MAT0 **ALT6** - FLEXIO0_D18 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A8
P1_11	D3	4	D1	**ALT0** - P1_11 **ALT1** - TRIG_OUT2 **ALT2** - LPUART1_CTS_B **ALT3** - LPI2C2_SCLS **ALT4** - CT2_MAT1 **ALT6** - FLEXIO0_D19 **ALT10** - I3C0_PUR **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A9 **VDD SYS** - WUU0_IN11
P1_12	D2	5	--	**ALT0** - P1_12	**IO Supply** - VDD	**ANALOG** - ADC1_A10

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT2 - LPI2C1_SDA **ALT3** - LPUART2_RXD **ALT4** - CT2_MAT2 **ALT6** - FLEXIO0_D20 **ALT11** - CAN0_RXD	**Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN12
P1_13	D1	6	--	**ALT0** - P1_13 **ALT1** - TRIG_IN3 **ALT2** - LPI2C1_SCL **ALT3** - LPUART2_TXD **ALT4** - CT2_MAT3 **ALT6** - FLEXIO0_D21 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A11
P1_14	E4	7	--	**ALT0** - P1_14 **ALT2** - LPI2C1_SCLS **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP10 **ALT5** - CT3_MAT0 **ALT6** - FLEXIO0_D22	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A12
P1_15	F4	8	--	**ALT0** - P1_15 **ALT2** - LPI2C1_SDAS **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP11 **ALT5** - CT3_MAT1 **ALT6** - FLEXIO0_D23	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A13
P1_29	F3	9	E1	**ALT0** - P1_29 **ALT1** - RESET_B **ALT2** - SPC_LPREQ	**IO Supply** - VDD **Pad type** - RST **Default** - ALT1	**VDD SYS** - RESET_B
P1_30	F1	10	E2	**ALT0** - P1_30 **ALT1** - TRIG_OUT3 **ALT3** - LPI2C0_SDA **ALT4** - CT_INP16 **ALT6** - FLEXIO0_D30 **ALT10** - I3C0_SDA	**IO Supply** - VDD **Pad type** - HD+I3C **Default** - DIS	**ANALOG** - XTAL48M
P1_31	F2	11	F2	**ALT0** - P1_31 **ALT1** - TRIG_IN4	**IO Supply** - VDD **Pad type** - HD	**ANALOG** - EXTAL48M

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT3 - LPI2C0_SCL **ALT4** - CT_INP17 **ALT6** - FLEXIO0_D31 **ALT10** - I3C0_SCL	**Default** - DIS	
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	12	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD	
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	12	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD	
VREFL	H7	12	E4		**IO Supply** - VDD	
VREFH	H6	13	F4		**IO Supply** - VDD	
VDD_ANA	J5	14	E3		**IO Supply** - VDD	
VDD	E5,F6,H8,J9	15	G3		**IO Supply** - VDD	
P4_2	H1	16	--	**ALT0** - P4_2 **ALT1** - CLKOUT **ALT2** - LPI2C2_SDAS **ALT3** - LPUART3_RXD **ALT4** - CT4_MAT0 **ALT5** - PWM0_A2 **ALT6** - FLEXIO0_D10	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN16
P4_3	H3	17	--	**ALT0** - P4_3 **ALT2** - LPI2C2_SCL **ALT3** - LPUART4_TXD **ALT4** - CT4_MAT1 **ALT5** - PWM0_B2 **ALT6** - FLEXIO0_D11	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_4	J3	18	--	**ALT0** - P4_4 **ALT2** - LPI2C2_SDA **ALT3** - LPUART4_RXD **ALT4** - CT4_MAT2 **ALT5** - PWM0_A1 **ALT6** - FLEXIO0_D12	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN17
P4_5	K3	19	--	**ALT0** - P4_5 **ALT1** - TRIG_OUT3 **ALT2** - LPI2C2_SCLS **ALT3** - LPUART3_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT4 - CT4_MAT3 **ALT5** - PWM0_B1 **ALT6** - FLEXIO0_D13		
P4_6	K1	20	--	**ALT0** - P4_6 **ALT1** - TRIG_IN4 **ALT2** - LPI2C2_HREQ **ALT3** - LPUART3_CTS_B **ALT4** - CT_INP6 **ALT5** - PWM0_A0 **ALT6** - FLEXIO0_D14	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P4_7	K2	21	--	**ALT0** - P4_7 **ALT1** - TRIG_IN5 **ALT3** - LPUART3_RTS_B **ALT4** - CT_INP7 **ALT5** - PWM0_B0 **ALT6** - FLEXIO0_D15	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	
P2_0	L2	22	G2	**ALT0** - P2_0 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RXD **ALT3** - LPUART4_CTS_B **ALT4** - CT_INP16 **ALT5** - CT2_MAT0 **ALT6** - FLEXIO0_D8	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A0 **VDD SYS** - WUU0_IN18
P2_1	M2	23	G1	**ALT0** - P2_1 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_TXD **ALT3** - LPUART4_RTS_B **ALT4** - CT_INP17 **ALT5** - CT2_MAT1 **ALT6** - FLEXIO0_D9	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A1
P2_2	M1	24	H1	**ALT0** - P2_2 **ALT1** - TRIG_IN6 **ALT2** - LPUART0_RTS_B **ALT3** - LPUART2_TXD **ALT4** - CT_INP12 **ALT5** - CT2_MAT2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A4/ CMP0_IN0/DAC0_OUT

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT6 - FLEXIO0_D10		
P2_3	N1	25	J1	**ALT0** - P2_3 **ALT1** - TRIG_IN7 **ALT2** - LPUART0_CTS_B **ALT3** - LPUART2_RXD **ALT4** - CT_INP13 **ALT5** - CT2_MAT3 **ALT6** - FLEXIO0_D11	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - CMP1_IN0/ADC1_A4 **VDD SYS** - WUU0_IN19
P2_4	N2	26	J2	**ALT0** - P2_4 **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP14 **ALT5** - CT1_MAT0 **ALT6** - FLEXIO0_D12	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A0
P2_5	L3	27	H2	**ALT0** - P2_5 **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP15 **ALT5** - CT1_MAT1 **ALT6** - FLEXIO0_D13	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A1
P2_6	M4	28	H3	**ALT0** - P2_6 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI1_PCS1 **ALT3** - LPUART4_RXD **ALT4** - CT_INP18 **ALT5** - CT1_MAT2 **ALT6** - FLEXIO0_D14	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A3
P2_7	N4	29	H4	**ALT0** - P2_7 **ALT1** - TRIG_IN5 **ALT3** - LPUART4_TXD **ALT4** - CT_INP19 **ALT5** - CT1_MAT3 **ALT6** - FLEXIO0_D15	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_7	N4	29	H4		**IO Supply** - VDD **Pad type** - ANA	**ANALOG** - VREFI/ ADC0_A7/ADC1_A7
P2_10	L4	30	--	**ALT0** - P2_10 **ALT1** - TRIG_OUT5	**IO Supply** - VDD **Pad type** - SLOW	

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT3 - LPUART2_TXD **ALT4** - CT3_MAT2 **ALT6** - FLEXIO0_D18	**Default** - DIS	
P2_11	K5	31	--	**ALT0** - P2_11 **ALT1** - TRIG_IN4 **ALT3** - LPUART2_RXD **ALT4** - CT3_MAT3 **ALT6** - FLEXIO0_D19	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	32	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD	
VDD	E5,F6,H8,J9	33	G3		**IO Supply** - VDD	
P2_12	K6	34	J4	**ALT0** - P2_12 **ALT1** - USB0_VBUS_DET **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_RXD **ALT4** - CT4_MAT0 **ALT5** - CT0_MAT0 **ALT6** - FLEXIO0_D20 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ISP** - USB0_VBUS_DET **ANALOG** - ADC0_A5/OPAMP0_INP0 **VDD SYS** - WUU0_IN20
P2_13	L6	35	J5	**ALT0** - P2_13 **ALT1** - TRIG_IN8 **ALT2** - LPSPI1_SDO **ALT3** - LPUART1_TXD **ALT4** - CT4_MAT1 **ALT5** - CT0_MAT1 **ALT6** - FLEXIO0_D21 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A5
P2_13	L6	35	J5		**IO Supply** - VDD **Pad type** - LOLK	**ANALOG** - OPAMP0_INN
P2_15	N6	36	H5	**ALT0** - P2_15 **ALT1** - TRIG_OUT4 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_RTS_B **ALT4** - CT4_MAT3 **ALT5** - CT0_MAT2	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - OPAMP0_OUT/ADC0_A2

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT6 - FLEXIO0_D23		
P2_16	M6	37	--	**ALT0** - P2_16 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_RTS_B **ALT4** - CT3_MAT0 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D24	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A6
P2_17	M7	38	--	**ALT0** - P2_17 **ALT1** - TRIG_IN9 **ALT2** - LPSPI1_PCS0 **ALT3** - LPUART1_CTS_B **ALT4** - CT3_MAT1 **ALT5** - CT0_MAT3 **ALT6** - FLEXIO0_D25	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A6
P2_19	M8	39	--	**ALT0** - P2_19 **ALT1** - TRIG_OUT5 **ALT4** - CT3_MAT3 **ALT6** - FLEXIO0_D27	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A2
P2_20	N8	40	--	**ALT0** - P2_20 **ALT1** - TRIG_IN8 **ALT2** - LPSPI1_PCS2 **ALT4** - CT2_MAT0 **ALT6** - FLEXIO0_D28	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_21	L8	41	--	**ALT0** - P2_21 **ALT1** - TRIG_IN9 **ALT2** - LPSPI1_PCS3 **ALT4** - CT2_MAT1 **ALT6** - FLEXIO0_D29	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
P2_23	L9	42	--	**ALT0** - P2_23 **ALT1** - TRIG_OUT5 **ALT4** - CT2_MAT3 **ALT6** - FLEXIO0_D31	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	
VDD_USB	M11	43	H6		**IO Supply** - VDD_USB	
USB0_DM	M10	44	H7		**IO Supply** - VDD_USB	**ANALOG** - USB0_DM **VDD SYS** - WUU0_IN28

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
USB0_DP	N10	45	J7		**IO Supply** - VDD_USB	**ANALOG** - USB0_DP **VDD SYS** - WUU0_IN29
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	46	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD_P3	
VDD_P3	E9,F8	47	G5		**IO Supply** - VDD_P3	
P3_31	N12	48	J8	**ALT0** - P3_31 **ALT1** - TRIG_IN10 **ALT2** - LPI2C3_SDAS **ALT3** - LPUART4_CTS_B **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D31	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A20 **VDD SYS** - LPTMR0_ALT2
P3_30	N13	49	J9	**ALT0** - P3_30 **ALT1** - TRIG_OUT6 **ALT2** - LPI2C3_SCLS **ALT3** - LPUART4_RTS_B **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D30	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC1_A21
P3_29	M13	50	H9	**ALT0** - P3_29 **ALT1** - ISPMODE_N **ALT2** - LPI2C3_HREQ **ALT4** - CT_INP3 **ALT5** - CT3_MAT3 **ALT6** - FLEXIO0_D29	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - ALT1	**ANALOG** - ADC1_A22 **VDD SYS** - WUU0_IN27
P3_28	L11	51	G7	**ALT0** - P3_28 **ALT1** - TRIG_IN11 **ALT2** - LPI2C3_SDA **ALT3** - LPUART4_RXD **ALT4** - CT_INP12 **ALT5** - CT3_MAT2 **ALT6** - FLEXIO0_D28	**IO Supply** - VDD_P3 **Pad type** - 5VTOL **Default** - DIS	**VDD SYS** - WUU0_IN26
P3_27	K11	52	E7	**ALT0** - P3_27 **ALT1** - TRIG_OUT7 **ALT2** - LPI2C3_SCL **ALT3** - LPUART4_TXD **ALT4** - CT_INP13	**IO Supply** - VDD_P3 **Pad type** - 5VTOL **Default** - DIS	**VDD SYS** - WUU0_IN30

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT5 - CT3_MAT1 **ALT6** - FLEXIO0_D27		
P3_22	K13	53	--	**ALT0** - P3_22 **ALT3** - LPUART1_RTS_B **ALT4** - CT_INP10 **ALT6** - FLEXIO0_D30 **ALT7** - PWM1_X2	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_21	J10	54	--	**ALT0** - P3_21 **ALT1** - TRIG_OUT1 **ALT2** - LPI2C3_SCL **ALT3** - LPUART1_TXD **ALT4** - CT2_MAT3 **ALT6** - FLEXIO0_D29	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_20	H10	55	--	**ALT0** - P3_20 **ALT1** - TRIG_OUT0 **ALT2** - LPI2C3_SDA **ALT3** - LPUART1_RXD **ALT4** - CT2_MAT2 **ALT5** - PWM0_X2 **ALT6** - FLEXIO0_D28	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_19	G11	56	--	**ALT0** - P3_19 **ALT2** - LPUART4_TXD **ALT4** - CT2_MAT1 **ALT5** - PWM0_X1 **ALT6** - FLEXIO0_D27 **ALT7** - PWM1_X1	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_18	F10	57	--	**ALT0** - P3_18 **ALT2** - LPUART4_RXD **ALT4** - CT2_MAT0 **ALT5** - PWM0_X0 **ALT6** - FLEXIO0_D26 **ALT7** - PWM1_X0	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_17	H11	58	--	**ALT0** - P3_17 **ALT2** - LPUART4_CTS_B **ALT4** - CT_INP9	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT6 - FLEXIO0_D25 **ALT7** - PWM1_B0		
P3_16	H13	59	--	**ALT0** - P3_16 **ALT2** - LPUART4_RTS_B **ALT4** - CT_INP8 **ALT6** - FLEXIO0_D24 **ALT7** - PWM1_A0	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_15	H12	60	H8	**ALT0** - P3_15 **ALT2** - LPUART2_TXD **ALT3** - LPUART3_RTS_B **ALT4** - CT_INP7 **ALT6** - FLEXIO0_D23 **ALT7** - PWM1_B1	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_14	G12	61	G8	**ALT0** - P3_14 **ALT2** - LPUART2_RXD **ALT3** - LPUART3_CTS_B **ALT4** - CT_INP6 **ALT5** - PWM0_X2 **ALT6** - FLEXIO0_D22 **ALT7** - PWM1_A1	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	**VDD SYS** - WUU0_IN25
P3_13	F12	62	F8	**ALT0** - P3_13 **ALT2** - LPUART2_CTS_B **ALT3** - LPUART3_RXD **ALT4** - CT1_MAT3 **ALT5** - PWM0_X1 **ALT6** - FLEXIO0_D21 **ALT7** - PWM1_B2	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
P3_12	F13	63	F9	**ALT0** - P3_12 **ALT2** - LPUART2_RTS_B **ALT3** - LPUART3_TXD **ALT4** - CT1_MAT2 **ALT5** - PWM0_X0 **ALT6** - FLEXIO0_D20 **ALT7** - PWM1_A2	**IO Supply** - VDD_P3 **Pad type** - SLOW **Default** - DIS	
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	64	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD_P3	

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
VDD_P3	E9,F8	65	G5		**IO Supply** - VDD_P3	
P3_11	F11	66	E9	**ALT0** - P3_11 **ALT1** - TRIG_IN6 **ALT2** - LPSPI1_PCS0 **ALT3** - LPUART1_CTS_B **ALT4** - CT1_MAT1 **ALT5** - PWM0_B2 **ALT6** - FLEXIO0_D19	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN24
P3_10	E11	67	E8	**ALT0** - P3_10 **ALT1** - TRIG_IN5 **ALT2** - LPSPI1_SCK **ALT3** - LPUART1_RTS_B **ALT4** - CT1_MAT0 **ALT5** - PWM0_A2 **ALT6** - FLEXIO0_D18	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	
P3_9	D11	68	D8	**ALT0** - P3_9 **ALT1** - TRIG_IN4 **ALT2** - LPSPI1_SDI **ALT3** - LPUART1_TXD **ALT4** - CT_INP5 **ALT5** - PWM0_B1 **ALT6** - FLEXIO0_D17	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	
P3_8	D13	69	C8	**ALT0** - P3_8 **ALT1** - TRIG_IN3 **ALT2** - LPSPI1_SDO **ALT3** - LPUART1_RXD **ALT4** - CT_INP4 **ALT5** - PWM0_A1 **ALT6** - FLEXIO0_D16 **ALT12** - CLKOUT	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	**VDD SYS** - WUU0_IN23
P3_7	D12	70	C9	**ALT0** - P3_7 **ALT1** - TRIG_IN2 **ALT2** - LPSPI1_PCS2 **ALT3** - LPUART3_CTS_B **ALT4** - CT4_MAT3 **ALT5** - PWM0_B0	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT6 - FLEXIO0_D15 **ALT7** - PWM1_B0		
P3_6	C12	71	B9	**ALT0** - P3_6 **ALT1** - CLKOUT **ALT2** - LPSPI1_PCS3 **ALT3** - LPUART3_RTS_B **ALT4** - CT4_MAT2 **ALT5** - PWM0_A0 **ALT6** - FLEXIO0_D14 **ALT7** - PWM1_A0 **ALT12** - FREQME_CLK_OUT1	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	
P3_2	B12	--	--	**ALT0** - P3_2 **ALT2** - LPSPI1_PCS1 **ALT4** - CT4_MAT0 **ALT6** - FLEXIO0_D10 **ALT7** - PWM1_X2	**IO Supply** - VDD_P3 **Pad type** - MED **Default** - DIS	
P3_1	B13	72	A9	**ALT0** - P3_1 **ALT1** - TRIG_IN1 **ALT3** - LPUART3_TXD **ALT4** - CT_INP17 **ALT5** - PWM0_B0 **ALT6** - FLEXIO0_D9 **ALT7** - PWM1_X1 **ALT12** - FREQME_CLK_OUT0	**IO Supply** - VDD_P3 **Pad type** - HD **Default** - DIS	
P3_0	A13	73	A8	**ALT0** - P3_0 **ALT1** - TRIG_IN0 **ALT3** - LPUART3_RXD **ALT4** - CT_INP16 **ALT5** - PWM0_A0 **ALT6** - FLEXIO0_D8 **ALT7** - PWM1_X0	**IO Supply** - VDD_P3 **Pad type** - HD **Default** - DIS	**VDD SYS** - WUU0_IN22
VSS	D4,D10,F7,G2,G6,G8,K4,K10,M12	74	D4,D5,D6,E6,F5,F6		**IO Supply** - VDD_P3	
VDD_P3	E9,F8	75	G5		**IO Supply** - VDD_P3	

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
VDD	E5,F6,H8,J9	--	G3		**IO Supply** - VDD	
P0_0	A12	76	B8	**ALT0** - P0_0 **ALT1** - TMS/SWDIO **ALT2** - LPUART0_RTS_B **ALT3** - LPSPI0_PCS0 **ALT4** - CT_INP0 **ALT6** - FLEXIO0_D0	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	
P0_1	C11	77	B7	**ALT0** - P0_1 **ALT1** - TCLK/SWCLK **ALT2** - LPUART0_CTS_B **ALT3** - LPSPI0_SDI **ALT4** - CT_INP1 **ALT6** - FLEXIO0_D1	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	
P0_2	C10	78	B6	**ALT0** - P0_2 **ALT1** - TDO/SWO **ALT2** - LPUART0_RXD **ALT3** - LPSPI0_SCK **ALT4** - CT0_MAT0 **ALT5** - UTICK_CAP0 **ALT6** - FLEXIO0_D2 **ALT10** - I3C0_PUR	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	**ISP** - UART_RXD
P0_3	B10	79	A6	**ALT0** - P0_3 **ALT1** - TDI **ALT2** - LPUART0_TXD **ALT3** - LPSPI0_SDO **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP1 **ALT6** - FLEXIO0_D3 **ALT8** - CMP0_OUT	**IO Supply** - VDD **Pad type** - MED **Default** - ALT1	**ISP** - UART_TXD **ANALOG** - CMP1_IN1/ADC0_A14
P0_6	A10	80	C7	**ALT0** - P0_6 **ALT1** - ISPMODE_N **ALT2** - LPI2C0_HREQ **ALT3** - LPSPI0_PCS1 **ALT4** - CT_INP2 **ALT6** - FLEXIO0_D6 **ALT8** - CMP1_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - ALT1	**ISP** - ISPMODE_N **ANALOG** - ADC0_A15

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT12 - CLKOUT		
VDD	E5,F6,H8,J9	81	G3		**IO Supply** - VDD	
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	82	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD	
P0_16	D9	83	C5	**ALT0** - P0_16 **ALT2** - LPI2C0_SDA **ALT3** - LPSPI0_PCS2 **ALT4** - CT0_MAT0 **ALT5** - UTICK_CAP2 **ALT6** - FLEXIO0_D0 **ALT10** - I3C0_SDA	**IO Supply** - VDD **Pad type** - HD+I3C **Default** - DIS	**ANALOG** - NVM_TM0 **VDD SYS** - WUU0_IN2
P0_17	D8	84	C3	**ALT0** - P0_17 **ALT2** - LPI2C0_SCL **ALT3** - LPSPI0_PCS3 **ALT4** - CT0_MAT1 **ALT5** - UTICK_CAP3 **ALT6** - FLEXIO0_D1 **ALT10** - I3C0_SCL	**IO Supply** - VDD **Pad type** - HD **Default** - DIS	**ANALOG** - NVM_TM1
P0_18	C8	85	--	**ALT0** - P0_18 **ALT2** - LPI2C0_SCLS **ALT4** - CT0_MAT2 **ALT6** - FLEXIO0_D2 **ALT8** - CMP0_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A8
P0_19	A8	86	--	**ALT0** - P0_19 **ALT2** - LPI2C0_SDAS **ALT4** - CT0_MAT3 **ALT6** - FLEXIO0_D3 **ALT8** - CMP1_OUT	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A9
P0_20	B8	87	--	**ALT0** - P0_20 **ALT3** - LPUART0_RXD **ALT4** - CT_INP0 **ALT6** - FLEXIO0_D4	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A10
P0_21	B7	88	--	**ALT0** - P0_21 **ALT3** - LPUART0_TXD **ALT4** - CT_INP1	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A11

Table continues on the next page...

Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT6 - FLEXIO0_D5		
P0_22	B6	89	--	**ALT0** - P0_22 **ALT3** - LPUART0_RTS_B **ALT4** - CT_INP2 **ALT5** - CT0_MAT0 **ALT6** - FLEXIO0_D6	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A12
P0_23	A6	90	--	**ALT0** - P0_23 **ALT3** - LPUART0_CTS_B **ALT4** - CT_INP3 **ALT5** - CT0_MAT1 **ALT6** - FLEXIO0_D7	**IO Supply** - VDD **Pad type** - SLOW **Default** - DIS	**ANALOG** - ADC0_A13
P1_0	C6	91	A5	**ALT0** - P1_0 **ALT1** - TRIG_IN0 **ALT2** - LPSPI0_SDO **ALT3** - LPI2C1_SDA **ALT4** - CT_INP4 **ALT5** - CT0_MAT2 **ALT6** - FLEXIO0_D8	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - SPI_SDO **ANALOG** - ADC0_A16/CMP0_IN3 **VDD SYS** - WUU0_IN6/LPTMR0_ALT3
P1_1	C5	92	B5	**ALT0** - P1_1 **ALT1** - TRIG_IN1 **ALT2** - LPSPI0_SCK **ALT3** - LPI2C1_SCL **ALT4** - CT_INP5 **ALT5** - CT0_MAT3 **ALT6** - FLEXIO0_D9	**IO Supply** - VDD **Pad type** - MED+I2C **Default** - DIS	**ISP** - SPI_SCK **ANALOG** - ADC0_A17/CMP1_IN3
P1_2	C4	93	B4	**ALT0** - P1_2 **ALT1** - TRIG_OUT0 **ALT2** - LPSPI0_SDI **ALT3** - LPI2C1_SDAS **ALT4** - CT1_MAT0 **ALT5** - CT_INP0 **ALT6** - FLEXIO0_D10 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ISP** - SPI_SDI **ANALOG** - ADC0_A18
P1_3	A4	94	B3	**ALT0** - P1_3 **ALT1** - TRIG_OUT1	**IO Supply** - VDD **Pad type** - MED	**ISP** - SPI_PCS **ANALOG** - ADC0_A19/CMP0_IN1

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Table 46. Pinout (continued)

Pin Name	A14xA15x BGA112	A14xA15x LQFP100	A14xA15x BGA64	Pinmux Assignment	Pad Settings	Alternate Functions
				ALT2 - LPSPI0_PCS0 **ALT3** - LPI2C1_SCLS **ALT4** - CT1_MAT1 **ALT5** - CT_INP1 **ALT6** - FLEXIO0_D11 **ALT11** - CAN0_RXD	**Default** - DIS	**VDD SYS** - WUU0_IN7
VDD	E5,F6,H8,J9	95	G3		**IO Supply** - VDD	
VSS	D4,D10,F7,G2,G6, G8,K4,K10,M12	96	D4,D5,D6,E6,F5,F 6		**IO Supply** - VDD	
P1_4	B4	97	A3	**ALT0** - P1_4 **ALT1** - FREQME_CLK_IN0 **ALT2** - LPSPI0_PCS3 **ALT3** - LPUART2_RXD **ALT4** - CT1_MAT2 **ALT6** - FLEXIO0_D12	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A20/CMP0_IN2 **VDD SYS** - WUU0_IN8
P1_5	B3	98	A2	**ALT0** - P1_5 **ALT1** - FREQME_CLK_IN1 **ALT2** - LPSPI0_PCS2 **ALT3** - LPUART2_TXD **ALT4** - CT1_MAT3 **ALT6** - FLEXIO0_D13	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A21/CMP1_IN2
P1_6	B2	99	A1	**ALT0** - P1_6 **ALT1** - TRIG_IN2 **ALT2** - LPSPI0_PCS1 **ALT3** - LPUART2_RTS_B **ALT4** - CT_INP6 **ALT5** - CT4_MAT0 **ALT6** - FLEXIO0_D14 **ALT11** - CAN0_TXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A22
P1_7	A2	100	B1	**ALT0** - P1_7 **ALT1** - TRIG_OUT2 **ALT3** - LPUART2_CTS_B **ALT4** - CT_INP7 **ALT5** - CT4_MAT1 **ALT6** - FLEXIO0_D15 **ALT11** - CAN0_RXD	**IO Supply** - VDD **Pad type** - MED **Default** - DIS	**ANALOG** - ADC0_A23 **VDD SYS** - WUU0_IN9

NOTE

- +I3C in Pad Type represents that strong pull up resistor is implemented on the pin. PV bit is implemented in Pin Control register of the pin.
- +I2C_FILT in Pad Type represents that I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- HD in Pad Type represents that the pin can support up to 20mA drive strength. I2C filter is implemented on the pin. PFE bit is implemented in Pin Control register of the pin.
- 5VTOL in Pad Type represents that the pin is 5V tolerant
- DIS in default column represents that the pin's input buffer is disabled by default
- RST pads support passive filter and 1M ohm pull resistor. PFE and PV bits are implemented in Pin Control register of the pin.
- PE, PS, SRE, ODE and DSE are supported in Pin Control register of all types of IO.
- 5VTol and HD pads support two DSE bits in Pin Control register of the pin.
- PWM1, OpAMP and DAC are not available in MCXA145 and MCXA146.
- In LQFP100, BGA112 and BGA64, the ISPMODE_n pin is on P0_6. In 64LQFP and smaller pin count package, ISPMODE_n pin is on P3_29.
- SLOW in Pad Type represents the IO supports 25 MHz. MED in Pad Type represents the Io supports 50 MHz.

6.2 MCXA156, A155, A154, A146, A145, A144 Pinout diagram

The pinout diagrams are provided in an Excel file attached to this document:

1. Click the paperclip symbol on the left side of the PDF window.
2. Double-click on the Excel file to open it.
3. Select the respective package tab.

Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, refer to the "Pinout" tab in the Excel file.

6.3 Recommended connection for unused analog and digital pins

Table 47 shows the recommended connections for pins if those pins are not used in the customer's application

Table 47. Recommended connection for unused interfaces

Pin Type	Pin Function	Recommendation	Comments
Power	VDD	Must be powered	VDD is the IO supply of P0,P1,P2 and P4, and supplies internal modules including Flash, CMP, and etc. It must be on.
Power	VDD_P3	Must be powered	VDD_P3 is the IO supply of P3. It must be ramp up together with or after VDD. If want to shut down VDD_P3, must assert the isolation in SPC EVD_CFG register before shut down VDD_P3 in Active mode.
Power	VDD_ANA	Must be powered	VDD_ANA must be same level with VDD, and ramps up together with VDD_ANA
Power	VDD_USB	Tie to ground through a 10 kΩ resistor if VDD_	

Table continues on the next page...

Table 47. Recommended connection for unused interfaces (continued)

Pin Type	Pin Function	Recommendation	Comments
		USB is an independent pin in the package version used	
Power	VREFH	Always connect to VDD_ANA potential	Always connect to VDD_ANA potential
Power	VREFL	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_ANA	Always connect to VSS potential	Always connect to VSS potential
Power	VSS_USB	Always connect to VSS potential	Always connect to VSS potential
Analog/non-GPIO	ADC*n_x*	Float	
Analog/non-GPIO	ADC*n_x*/DAC*n*_OUT	Float	
Analog/non-GPIO	EXTAL	Float	
Analog/non-GPIO	XTAL	Float	Analog output - Float
Analog/non-GPIO	USB0_DP	Float	Float
Analog/non-GPIO	USB0_DM	Float	Float
GPIO/Analog	Px/ADC*n_x*	Float	Float (default is analog input)
GPIO/Analog	Px/CMP*n*_IN*x*	Float	Float (default is analog input)
GPIO/Digital	JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	JTAG_TDI	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	Px	Float	Float (default is disabled)

7 Ordering parts

7.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to nxp.com and perform a part number search for the following device numbers: MCX A146

NOTE

For complete list of Orderable part numbers, please refer Table 1

8 Part identification

Part numbers for the device have fields that identify the specific part. Use the values of these fields to determine the specific part.

8.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

8.2 Part number format

Part numbers for this device have the following format:

B PS F C D FS T PG SR PT

Table 48. Part number fields descriptions

Field	Description	Values
B	Brand	• MCX
PS	Product series name	• A
F	Family	• 1 = First Device, Smallest Die size • 2 = 2nd Device w Always On Domain • 3 = 3rd Device w Advance Analog
C	Core Features	• 4 = 48 MHz, Motor PWM, USB FS • 5 = 96 MHz, Motor PWM, USB FS
FS	Flash Size	• 1 = 32 KB • 2 = 64 KB • 3 = 128 KB • 4 = 256 KB • 5 = 512 KB • 6 = 1024 KB • 7 = 2 M
T	Junction Temperature range (°C)	• V = –40 to 125
PG	Package	• LL = LQFP100 • MP = LFBGA64 • PJ = VFBGA112
SR	Silicon Revision	• A = Initial Mask set • B = 1st Major spin • C = 2nd Major spin
PT	Package Type	• R = Tape and Reel • T = Tray

8.3 Example

This is an example part number:

MCXA146VLH

8.4 Small package marking

8.4.1 Package marking information

Table 49. Package marking

	LQFP100 14*14	LFBGA64 5*5	VFBGA112 7*7
First line	AAAAAAAAAA	AAAAAA	AAAAAA
Second line	MMMMM	MMMMM	MMMMM
Third line	XXXXYYWWXX	XXYWXX	XXXYWXX

Identifier	Description
a	Part number code, refer to Ordering Information
m	Mask set
y	Year
w	Work week
x	NXP internal use

9 Terminology and guidelines

9.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that:

Table continues on the next page...

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Term	Definition
	• Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE** Typical values are provided as design guidelines and are neither tested nor guaranteed.

9.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

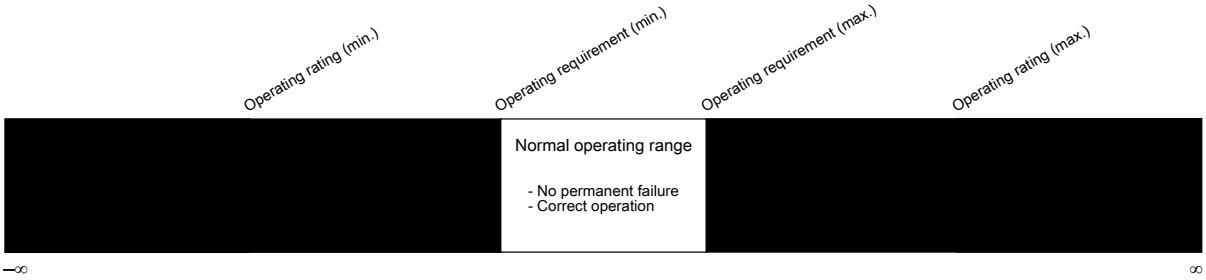
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

9.3 Typical-value conditions

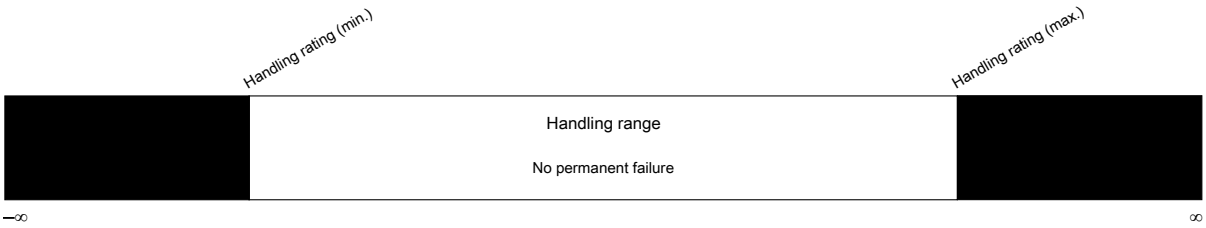
Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	3.3	V

9.4 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

9.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9.6 Specification Test Methods

Each specification is tested using one of these methods.

Code	Method	Description
P	Production direct	On every chip during production, testing the specification
I	Production indirect	On every chip during production, testing parts of a module that affect whether the chip meets the specification but not testing the specification itself
C	Characterization on a production tester	Measuring a statistically significant number of sample chips across process (matrix lot), voltage, and temperature
L	Characterization on lab equipment or a nonproduction tester	

Table continues on the next page...

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Code	Method	Description
		NOTE Typical values are not necessarily characterized across process.
D	Guaranteed by design	Specification based on scientific and engineering principles
O	Other	Using methods such as: • Performing silicon simulations • Performing package thermal simulations • Calculating specifications using reliability data

10 Revision History

The following table provides a revision history for this document.

Table 50. Revision History

Rev. No.	Date	Substantial Changes
5	July 2024	• Initial public release

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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