FS6500, FS4500

Safety power system basis chip with CAN FD and LIN transceivers

Rev. 7.0 — 11 November 2020 Product short data sheet

1 General description

The FS6500/FS4500 SMARTMOS devices are a multi-output, power supply, integrated circuit, including CAN Flexible Data (FD) and/or LIN transceivers, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32 µA) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS6500/FS4500 includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL D).

The built-in CAN FD interface fulfills the ISO 11898-2[(13)] and -5[(14)] standards. The LIN interface fulfills LIN protocol specifications 2.0, 2.1[(23)], 2.2[(24)], and SAE J2602-2[(25)].

High temperature capability up to T_A = 125 °C and T_J = 150 °C, compliant with AEC-Q100 Grade 1 automotive qualification.

2 Features and benefits

- Battery voltage sensing and MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (V_{CCA} tracker or independent), 5.0 V, or 3.3 V
- Linear voltage regulator dedicated to MCU Analog/Digital (A/D) reference voltage or I/Os supply (V_{CCA}), 5.0 V, or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT
- Five configurable I/Os

3 Applications

- Drive Train Electrification (BMS, Hybrid EV and HEV, Inverter, DC-DC, Alterno Starter)
- Drive Train - Chassis and Safety (Active Suspension, Steering, Safety Domain Gateway)
- Power Train (EMS, TCU, Gear Box)
- ADAS (LDW, Radar, Sensor Fusion Safety area)

4 Simplified application diagrams

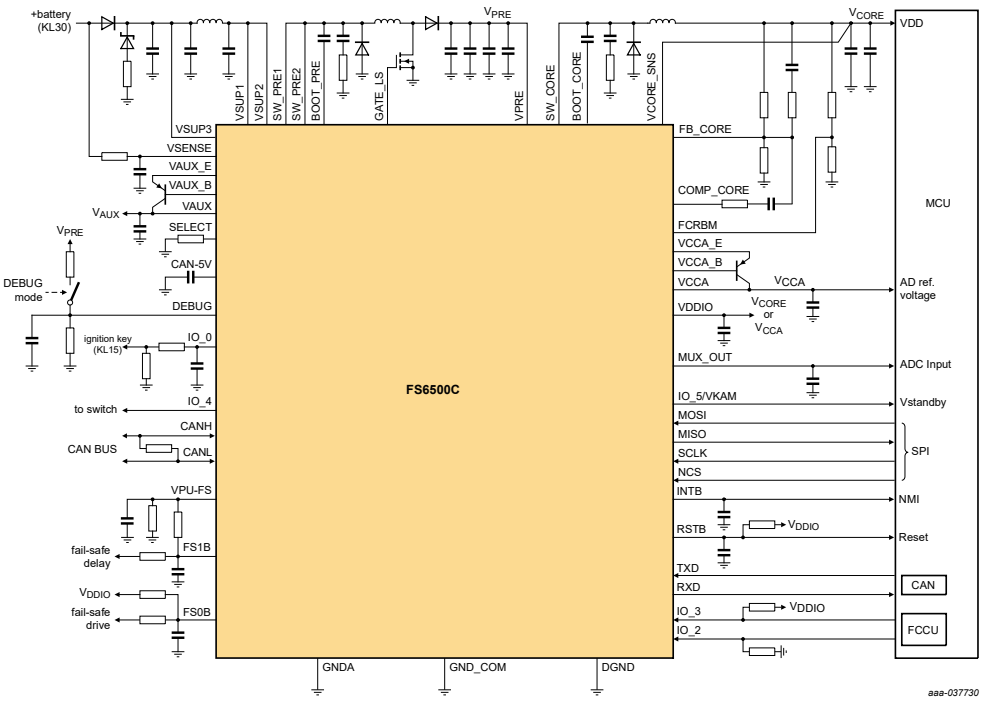


Figure 1. FS6500C simplified application diagram - buck boost configuration - FS1B

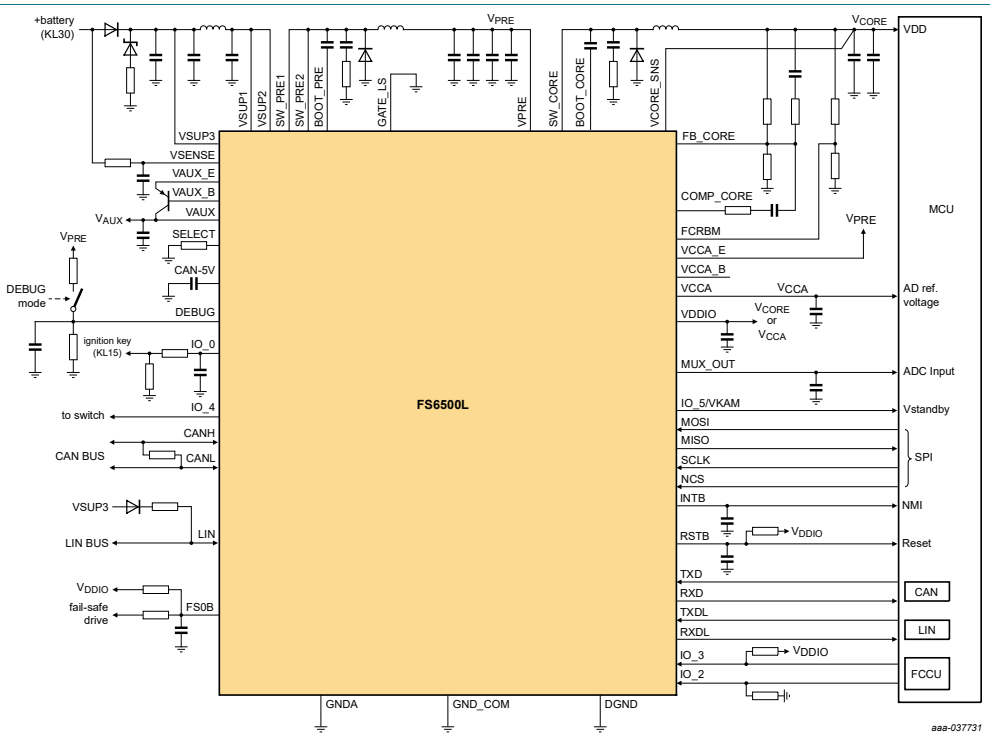


Figure 2. FS6500L simplified application diagram - buck configuration - LIN - V_{CCA} = 100 mA

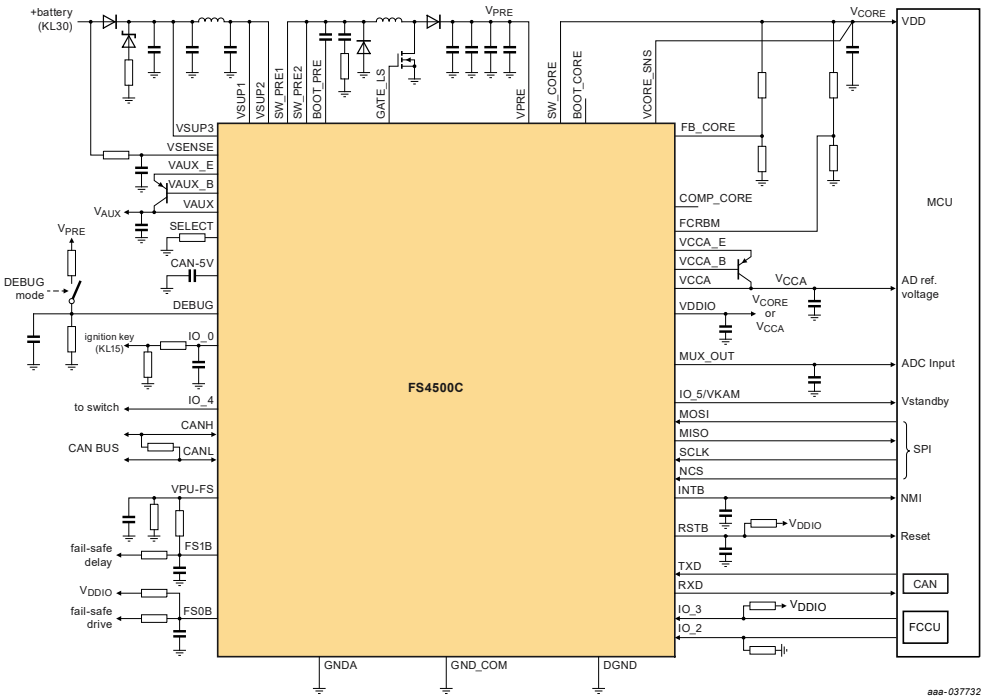


Figure 3. FS4500C simplified application diagram - buck boost configuration - FS1B

5 Ordering information

5.1 Part number definition

MC33FS **c** 5 **x** **y** **z** AE/R2

Table 1. Part number breakdown

Code	Option	Variable	Description
c	4 series	V_{CORE} type	Linear
	6 series		DC-DC
x	0	V_{CORE} current	0.5 A or 0.8 A
	1		1.5 A
	2		2.2 A
y	0	Functions	None
	1		FS1B
	2		LDT
	3		FS1B, LDT
	4		LDT, VKAM ON by default

Code	Option	Variable	Description
z	N	Physical interface	None
	C		CAN FD
	L		CAN FD and LIN

5.2 Part numbers list

Table 2. Orderable part variations

Part Number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	LIN	Notes
MC33FS4500CAE	–40 °C to 125 °C	48-pin LQFP exposed pad	0	0	0.5 A	Linear	by SPI	1	0	[1] [2]
MC33FS4500LAE			0	0	0.5 A	Linear	by SPI	1	1	
MC33FS4500NAE			0	0	0.5 A	Linear	by SPI	0	0	
MC33FS4501CAE			1	0	0.5 A	Linear	by SPI	1	0	
MC33FS4501NAE			1	0	0.5 A	Linear	by SPI	0	0	
MC33FS4502CAE			0	1	0.5 A	Linear	by SPI	1	0	
MC33FS4502LAE			0	1	0.5 A	Linear	by SPI	1	1	
MC33FS4502NAE			0	1	0.5 A	Linear	by SPI	0	0	
MC33FS4503CAE			1	1	0.5 A	Linear	by SPI	1	0	
MC33FS4503NAE			1	1	0.5 A	Linear	by SPI	0	0	
MC33FS6500CAE			0	0	0.8 A	DC-DC	by SPI	1	0	
MC33FS6500LAE			0	0	0.8 A	DC-DC	by SPI	1	1	
MC33FS6500NAE			0	0	0.8 A	DC-DC	by SPI	0	0	
MC33FS6501CAE			1	0	0.8 A	DC-DC	by SPI	1	0	
MC33FS6501NAE			1	0	0.8 A	DC-DC	by SPI	0	0	
MC33FS6502CAE			0	1	0.8 A	DC-DC	by SPI	1	0	
MC33FS6502LAE			0	1	0.8 A	DC-DC	by SPI	1	1	
MC33FS6502NAE			0	1	0.8 A	DC-DC	by SPI	0	0	
MC33FS6503CAE			1	1	0.8 A	DC-DC	by SPI	1	0	
MC33FS6503NAE			1	1	0.8 A	DC-DC	by SPI	0	0	
MC33FS6504LAE			0	1	0.8 A	DC-DC	by default	1	1	
MC33FS6510CAE			0	0	1.5 A	DC-DC	by SPI	1	0	
MC33FS6510LAE			0	0	1.5 A	DC-DC	by SPI	1	1	
MC33FS6510NAE			0	0	1.5 A	DC-DC	by SPI	0	0	
MC33FS6511CAE			1	0	1.5 A	DC-DC	by SPI	1	0	
MC33FS6511NAE			1	0	1.5 A	DC-DC	by SPI	0	0	
MC33FS6512CAE			0	1	1.5 A	DC-DC	by SPI	1	0	
MC33FS6512LAE			0	1	1.5 A	DC-DC	by SPI	1	1	
MC33FS6512NAE			0	1	1.5 A	DC-DC	by SPI	0	0	
MC33FS6513CAE			1	1	1.5 A	DC-DC	by SPI	1	0	
MC33FS6513NAE			1	1	1.5 A	DC-DC	by SPI	0	0	
MC33FS6514LAE			0	1	1.5 A	DC-DC	by default	1	1	
MC33FS6520CAE			0	0	2.2 A	DC-DC	by SPI	1	0	

Part Number	Temperature (T_A)	Package	FS1B	LDT	VCORE	VCORE type	VKAM on	CAN FD	LIN	Notes
MC33FS6520LAE			0	0	2.2 A	DC-DC	by SPI	1	1	
MC33FS6520NAE			0	0	2.2 A	DC-DC	by SPI	0	0	
MC33FS6521CAE			1	0	2.2 A	DC-DC	by SPI	1	0	
MC33FS6521NAE			1	0	2.2 A	DC-DC	by SPI	0	0	
MC33FS6522CAE			0	1	2.2 A	DC-DC	by SPI	1	0	
MC33FS6522LAE			0	1	2.2 A	DC-DC	by SPI	1	1	
MC33FS6522NAE			0	1	2.2 A	DC-DC	by SPI	0	0	
MC33FS6523CAE			1	1	2.2 A	DC-DC	by SPI	1	0	
MC33FS6523NAE			1	1	2.2 A	DC-DC	by SPI	0	0	

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. VKAM on by default is available on certain part numbers only.

6 Block diagram

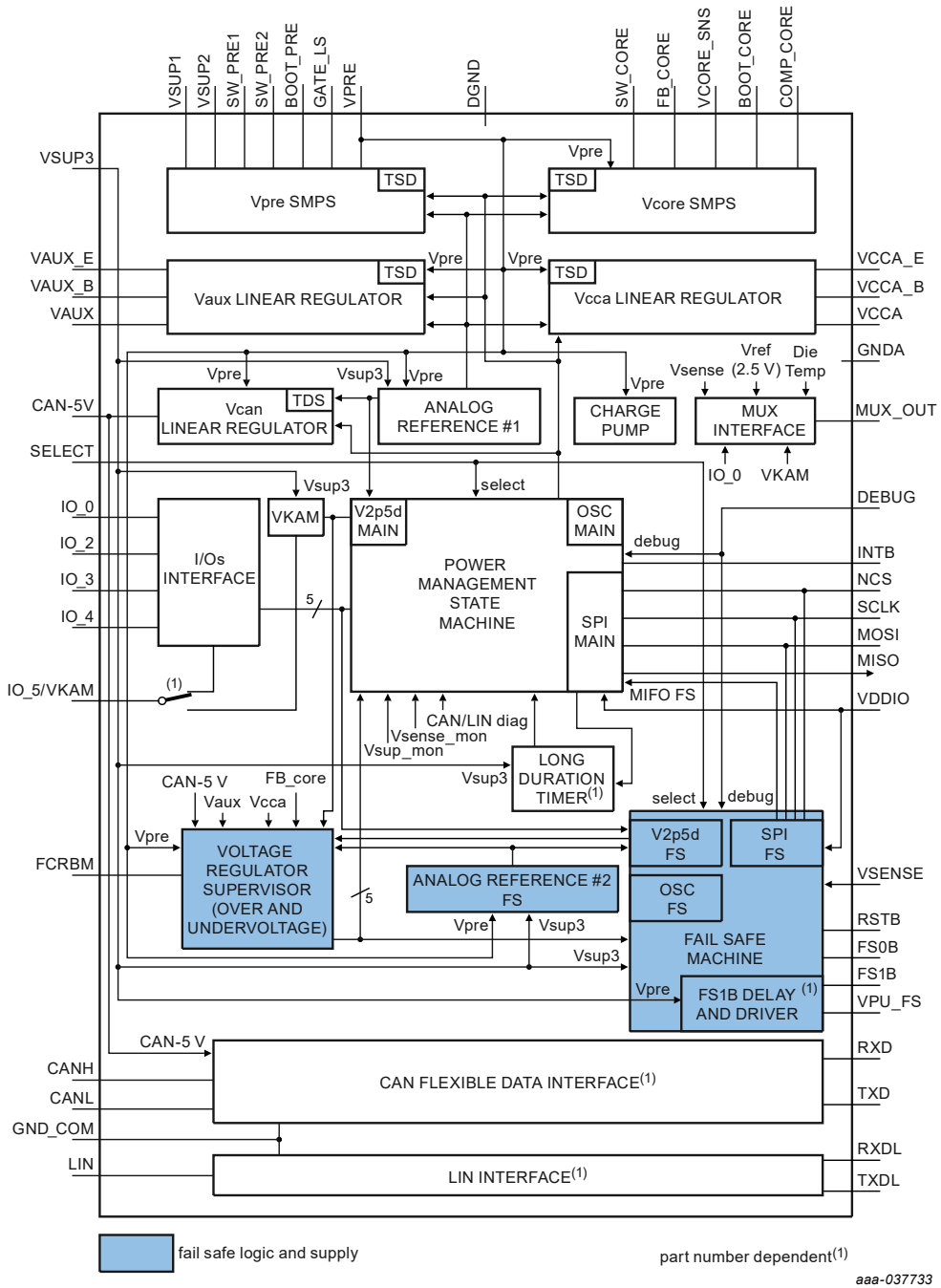


Figure 4. FS6500/FS4500 with CAN and LIN simplified internal block diagram

7 Pinning information

7.1 Pinning information

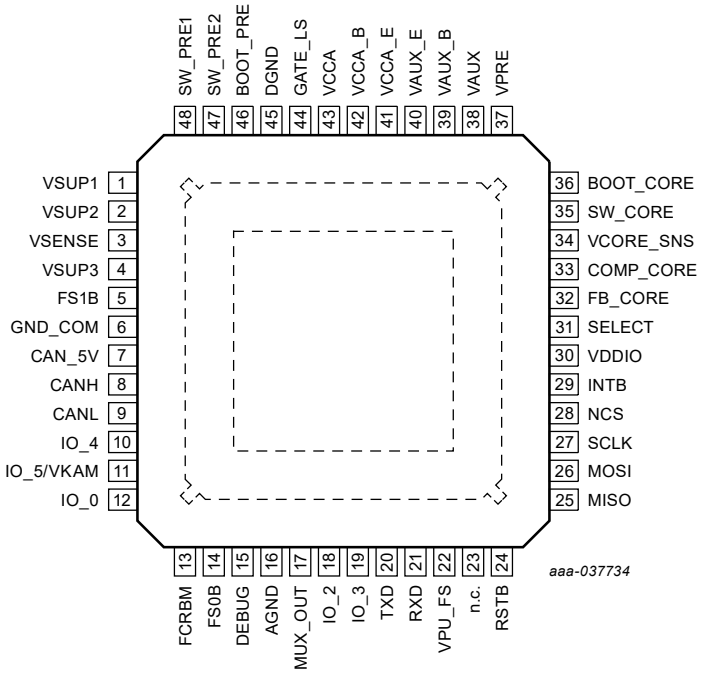


Figure 5. FS6500 pinout with CAN and FS1B

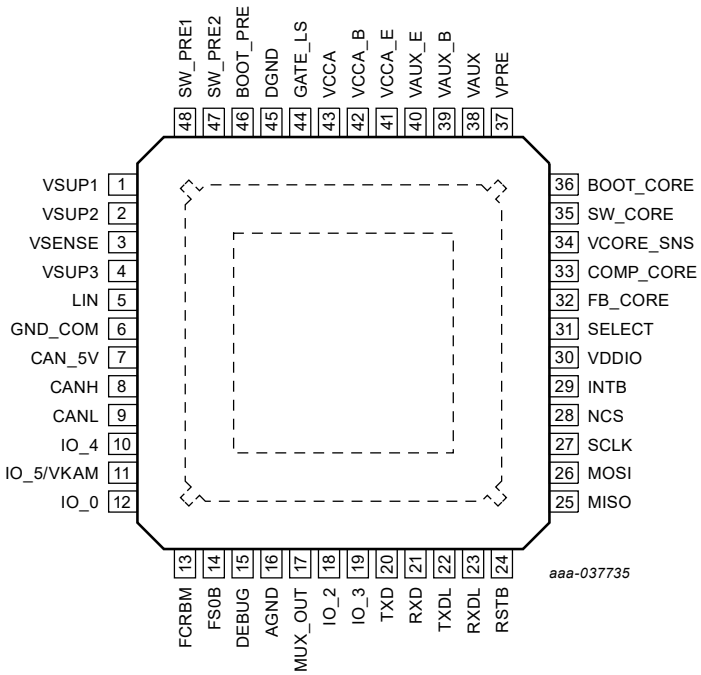


Figure 6. FS6500 pinout with CAN and LIN

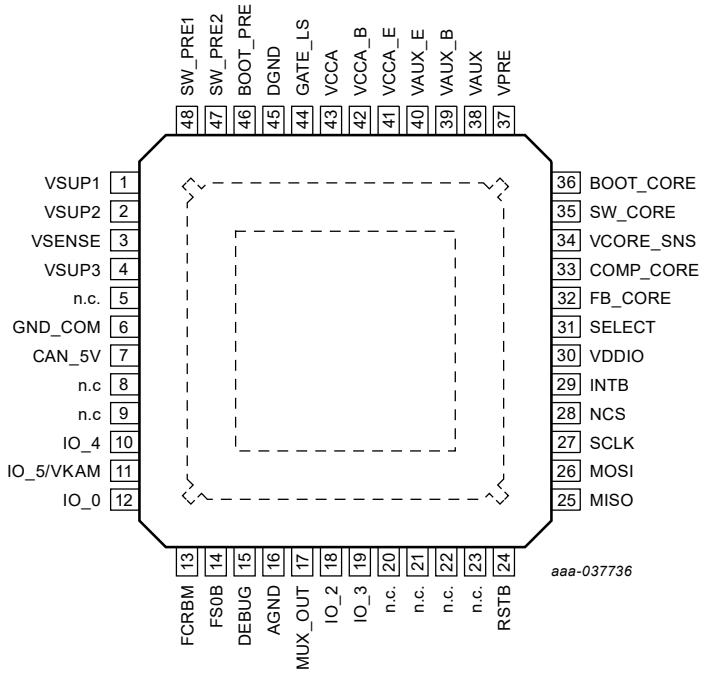


Figure 7. FS6500 pinout without CAN, without LIN

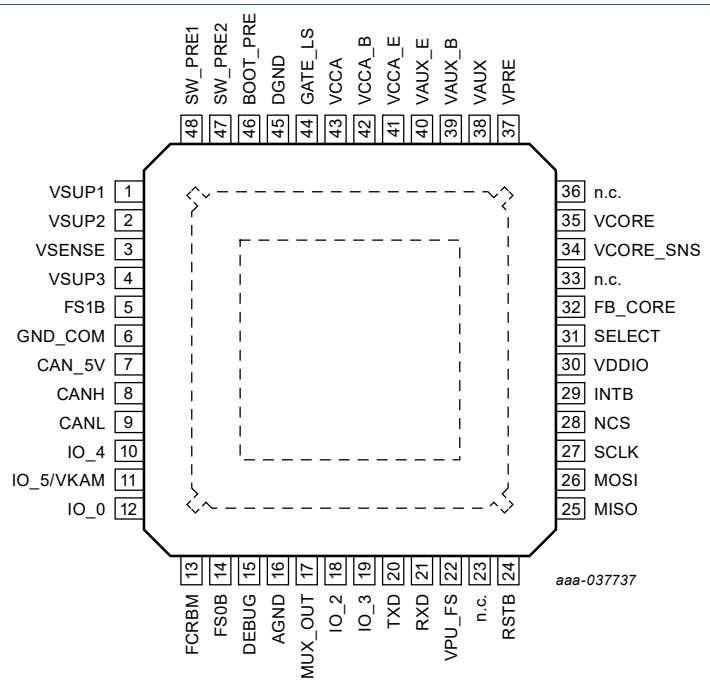


Figure 8. FS4500 pinout with CAN and FS1B

7.2 Pin description

A functional description of each pin can be found in the full data sheet.

Table 3. FS6500/FS4500 pin definition

Pin number	Pin name	Type	Definition
1	VSUP1	A_IN	Power supply of the device. An external reverse battery protection diode in series is mandatory
2	VSUP2	A_IN	Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.
3	VSENSE	A_IN	Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.
4	VSUP3	A_IN	Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.
5	LIN	A_IN/OUT	LIN single-wire bus transmitter and receiver.
	or FS1B	D_OUT	Second output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus FS0B output terminal. Open drain structure.
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
6	GND_COM	GROUND	Dedicated ground for physical layers
7	CAN_5V	A_OUT	Output voltage for the embedded CAN FD interface
8	CANH	A_IN/OUT	CAN output high. If CAN function is not used, this pin must be left open.
9	CANL	A_IN/OUT	CAN output low. If CAN function is not used, this pin must be left open.
10	IO_4	D_IN A_OUT	Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_5). **Wake-up capability:** Can be selectable to wake-up on edges or levels. **Output gate driver:** Can drive a logic level low-side NMOS transistor. Controlled by the SPI.
11	IO_5/VKAM	A_IN D_IN A_OUT	Can be used as digital input with wake-up capability or as an analog output providing keep alive memory supply in low-power mode. **Analog input**: Pin status can be read through the MUX output terminal **Digital input**: Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes (when used with IO_4). **Wake-up capability:** Can be selectable to wake-up on edges or levels. **Supply output:** Provide keep alive memory supply in low-power mode
	VKAM can be enabled or disabled by default at power up. The differentiation is made by part numbers.		
12	IO_0	A_IN D_IN	Can be used as analog or digital input (load dump proof) with wake-up capability (selectable) **Analog input**: Pin status can be read through the MUX output terminal **Digital input:** Pin status can be read through the SPI. **Wake-up capability:** Can be selectable to wake-up on edges or levels.

Pin number	Pin name	Type	Definition
13	FCRBM	A_IN	Feedback core resistor bridge monitoring: For safety purposes, this pin is used to monitor the middle point of a redundant resistor bridge connected on V_{CORE} (in parallel to the one used to set the V_{CORE} voltage). If not used, this pin must be connected directly to FB_CORE.
14	FS0B	D_OUT	First output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.
15	DEBUG	D_IN	Debug mode entry input
16	AGND	GROUND	Analog ground connection
17	MUX_OUT	A_OUT	Multiplexed output to be connected to a MCU ADC. Selection of the analog parameter is available at MUX-OUT through the SPI.
18 19	IO_2:3	D_IN	Digital input pin with wake-up capability (logic level compatible) **Digital input**: Pin status can be read through the SPI. Can be used to monitor FCCU error signals from MCU for safety purposes. **Wake-up capability:** Can be selectable to wake-up on edges or levels.
20	TXD	D_IN	Transceiver input from the MCU which controls the state of the CAN-bus. Internal pull-up to VDDIO. If CAN function is not used, this pin must be left open.
21	RXD	D_OUT	Receiver output which reports the state of the CAN-bus to the MCU If CAN function is not used, this pin must be left open.
22	TXDL	D_IN	Transceiver input from the MCU controlling the state of the LIN bus. Internal pull-up to VDDIO.
	or VPU_FS	A_OUT	Pull-up output for FS1B function.
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
23	RXDL	D_OUT	Receiver output reporting the state of the LIN bus to the MCU. If LIN function is not used, this pin must be left open.
24	RSTB	D_OUT	This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure.
25	MISO	D_OUT	SPI bus. Master input slave output
26	MOSI	D_IN	SPI bus. Master output slave input
27	SCLK	D_IN	SPI Bus. Serial clock
28	NCS	D_IN	Not chip select (active low)
29	INTB	D_OUT	This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.
30	VDDIO	A_IN	Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.
31	SELECT	D_IN	Hardware selection pin for VAUX and VCCA output voltages
32	FB_CORE	A_IN	VCORE voltage feedback. Input of the error amplifier.
33	COMP_CORE	A_OUT	Compensation network. Output of the error amplifier. For FS4500 series, this pin must be left open (NC).
34	VCORE_SNS	A_IN	VCORE input voltage sense

Pin number	Pin name	Type	Definition
35	SW_CORE	A_OUT	VCORE output switching point for FS6500 series
	or VCORE	A_OUT	VCORE output voltage for FS4500 series
36	BOOT_CORE	A_IN/OUT	Bootstrap capacitor for VCORE internal NMOS gate drive For FS4500 series, this pin must be left open (NC).
37	VPRE	A_IN	VPRE input voltage sense
38	VAUX	A_OUT	VAUX output voltage. External PNP ballast transistor. Collector connection
39	VAUX_B	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Base connection
40	VAUX_E	A_OUT	VAUX voltage regulator. External PNP ballast transistor. Emitter connection
41	VCCA_E	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Emitter connection
42	VCCA_B	A_OUT	VCCA voltage regulator. External PNP ballast transistor. Base connection
43	VCCA	A_OUT	VCCA output voltage. External PNP ballast transistor. Collector connection
44	GATE_LS	A_OUT	Low-side MOSFET gate drive for non-inverting buck-boost configuration
45	DGND	GROUND	Digital ground connection
46	BOOT_PRE	A_IN/OUT	Bootstrap capacitor for the VPRE internal NMOS gate drive
47	SW_PRE2	A_OUT	Second pre-regulator output switching point
48	SW_PRE1	A_OUT	First pre-regulator output switching point

8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
$V_{SUP1/2/3}$	DC voltage at power supply pins	–1.0 to 40	V	[1]
V_{SENSE}	DC voltage at battery sense pin (with ext R in series mandatory)	–14 to 40	V	
$V_{SW1,2}$	DC voltage at SW_PRE1 and SW_PRE2 Pins	–1.0 to 40	V	
V_{PRE}	DC voltage at VPRE Pin	–0.3 to 8	V	
V_{GATE_LS}	DC voltage at Gate_LS pin	–0.3 to 8	V	
V_{BOOT_PRE}	DC voltage at BOOT_PRE pin	–1.0 to 50	V	
V_{SW_CORE}	DC voltage at SW_CORE pin	–1.0 to 8	V	
V_{CORE_SNS}	DC voltage at VCORE_SNS pin	0.0 to 8	V	
V_{BOOT_CORE}	DC voltage at BOOT_CORE pin	0.0 to 15	V	
V_{FB_CORE}	DC voltage at FB_CORE pin	–0.3 to 2.5	V	
V_{COMP_CORE}	DC voltage at COMP_CORE pin	–0.3 to 2.5	V	
V_{FCRBM}	DC voltage at FCRBM pin	–0.3 to 8	V	
$V_{AUX\_B,E}$	DC voltage at VAUX_B, VAUX_E pins	–0.3 to 40	V	
V_{AUX}	DC voltage at VAUX pin	–2.0 to 40	V	
$V_{CCA\_B,E}$	DC voltage at VCCA_B, VCCA_E pins	–0.3 to 8	V	

Symbol	Ratings	Value	Unit	Notes
V_{CCA}	DC voltage at VCCA pin	–0.3 to 8	V	
V_{DDIO}	DC voltage at VDDIO pin	–0.3 to 8	V	
V_{CAN_5V}	DC voltage on CAN_5V pin	–0.3 to 8	V	
V_{PU_FS}	DC voltage at VPU_FS pin	–0.3 to 8	V	
V_{FSxB}	DC voltage at FS0B, FS1B pins (with ext R in series mandatory)	–0.3 to 40	V	
V_{DEBUG}	DC voltage at DEBUG pin	–0.3 to 40	V	
$V_{IO\_0,4}$	DC voltage at IO_0, IO_4 pins (with ext R in series mandatory)	–0.3 to 40	V	
V_{IO_5}	DC voltage at IO_5 pin	–0.3 to 20	V	
V_{KAM}	DC voltage at VKAM pin	–0.3 to 8	V	
V_{DIG}	DC voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, RXDL, TXDL, IO_2, IO_3 pins	–0.3 to 8	V	
V_{SELECT}	DC voltage at SELECT pin	–0.3 to 8	V	
V_{BUS_CAN}	DC voltage on CANL, CANH pins	–27 to 40	V	
V_{BUS_LIN}	DC voltage on LIN pin	–18 to 40	V	
I_Isense	V_{SENSE} maximum current capability	–5.0 to 5.0	mA	
$I\_IO_{0,4,5}$	IOs maximum current capability (IO_0, IO_4, IO_5)	–5.0 to 5.0	mA	
ESD voltage				
Human body model (JESD22/A114)[20] – 100 pF, 1.5 kΩ				
$V_{ESD-HBM1}$	• All pins	±2.0	kV	[2]
$V_{ESD-HBM2}$	• VSUP1, 2, 3, VSENSE, VAUX, IO_0,4, FS0B, FS1B, DEBUG	±4.0	kV	
$V_{ESD-HBM3}$	• CANH, CANL	±6.0	kV	
$V_{ESD-HBM4}$	• LIN	±8.0	kV	
Charge device model (JESD22/C101)[21]:				
$V_{ESD-CDM1}$	• All pins	±500	V	
$V_{ESD-CDM2}$	• Corner pins	±750	V	
System level ESD (gun test)				
	• VSUP1, 2, 3, VSENSE, VAUX, IO_0, 4, 5, FS0B, FS1B			
$V_{ESD-GUN1}$	330 Ω/150 pF unpowered according to IEC 61000-4-2:[17]	±8.0	kV	
$V_{ESD-GUN2}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±8.0	kV	
$V_{ESD-GUN3}$	2.0 kΩ/150 pF unpowered according to ISO 10605[16]	±8.0	kV	
$V_{ESD-GUN4}$	2.0 kΩ/330 pF powered according to ISO 10605[16]	±8.0	kV	
	• CANH, CANL			
$V_{ESD-GUN5}$	330 Ω/150 pF unpowered according to IEC 61000-4-2:[17]	±15.0	kV	
$V_{ESD-GUN6}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay Conformance	±12.0	kV	
$V_{ESD-GUN7}$	2.0 kΩ/150 pF unpowered according to ISO 10605[16]	±15.0	kV	
$V_{ESD-GUN8}$	2.0 kΩ/330 pF powered according to ISO 10605[16]	±12.0	kV	
	• LIN			
$V_{ESD-GUN9}$	330 Ω/150 pF unpowered according to IEC 61000-4-2:[17]	±12.0	kV	
$V_{ESD-GUN10}$	330 Ω/150 pF unpowered according to OEM LIN, CAN, FlexRay conformance	±12.0	kV	

Symbol	Ratings	Value	Unit	Notes
$V_{ESD-GUN11}$	2.0 kΩ/150 pF unpowered according to ISO 10605[16]	±12.0	kV	
$V_{ESD-GUN12}$	2.0 kΩ/330 pF powered according to ISO 10605[16]	±12.0	kV	
Thermal ratings				
T_A	Ambient temperature	–40 to 125	°C	
T_J	Junction temperature	–40 to 150	°C	
T_{STG}	Storage temperature	–55 to 150	°C	
Thermal resistance				
$R_{\theta JA}$	Thermal resistance junction to ambient	30	°C/W	[3]
$R_{\theta JCTOP}$	Thermal resistance junction to case top	23.8	°C/W	[4]
$R_{\theta JCBOTTOM}$	Thermal resistance junction to case bottom	0.9	°C/W	[5]

[1] All V_{SUPS} ($V_{SUP1/2/3}$) must be connected to the same supply (Figure 1).
[2] Compared to AGND.
[3] Per JEDEC JESD51-6[18] with the board (JESD51-7)[19] horizontal.
[4] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1)[22].
[5] Thermal resistance between the die and the solder pad on the bottom of the packaged based on simulation without any interface resistance.

9 Packaging

9.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 5. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00173D

9.2 Package outline

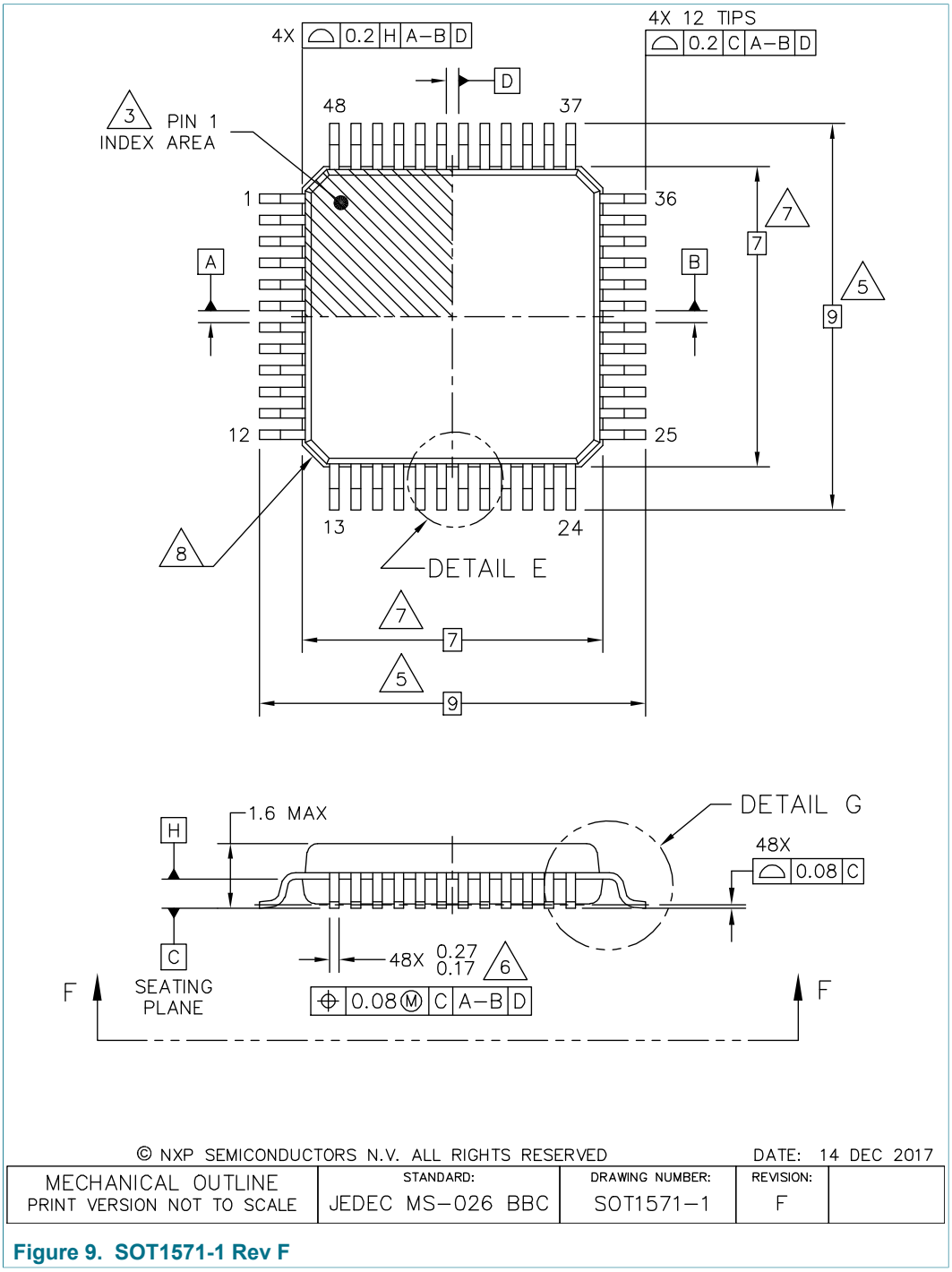


Figure 9. SOT1571-1 Rev F

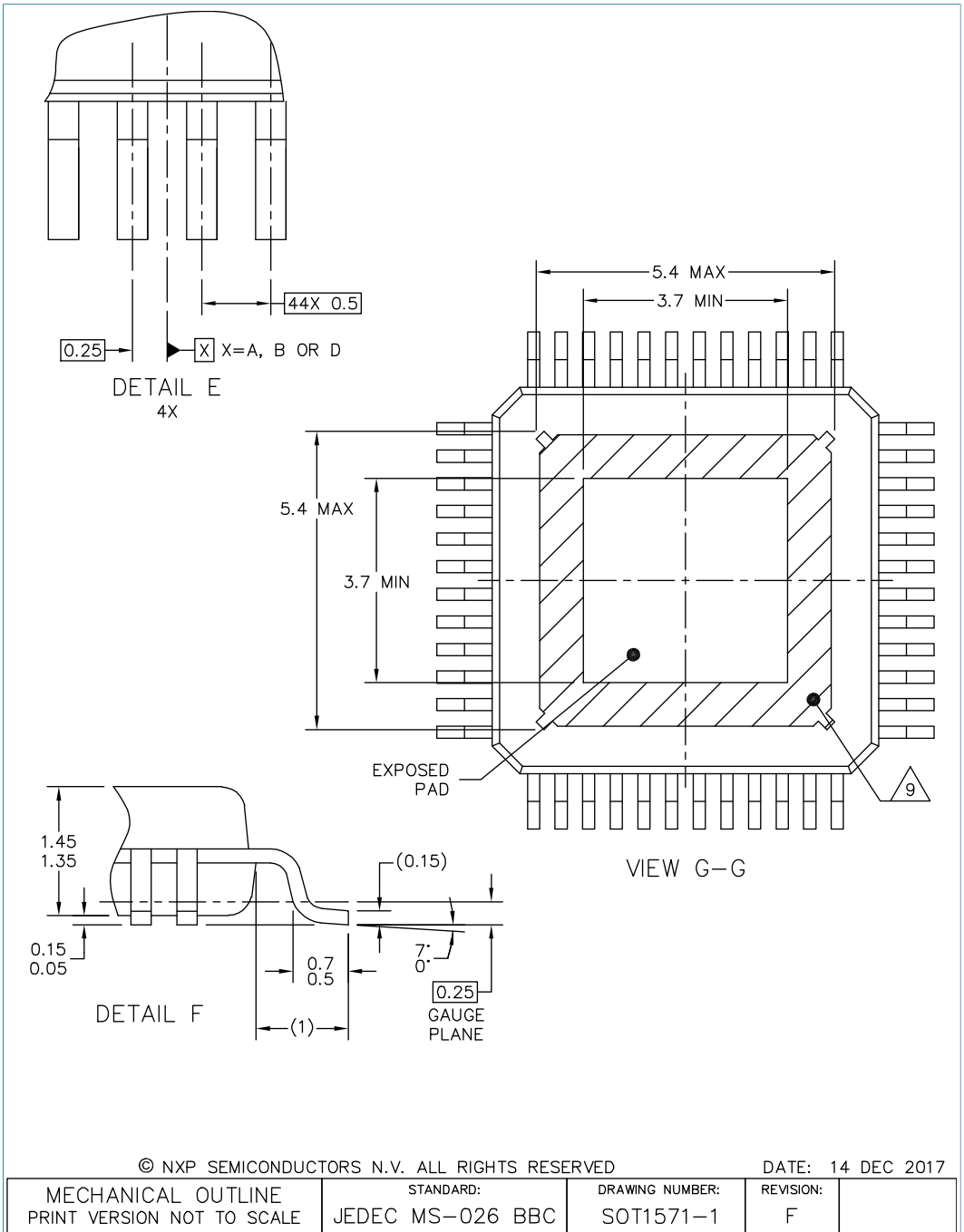


Figure 10. SOT1571-1 Rev. F Detail View

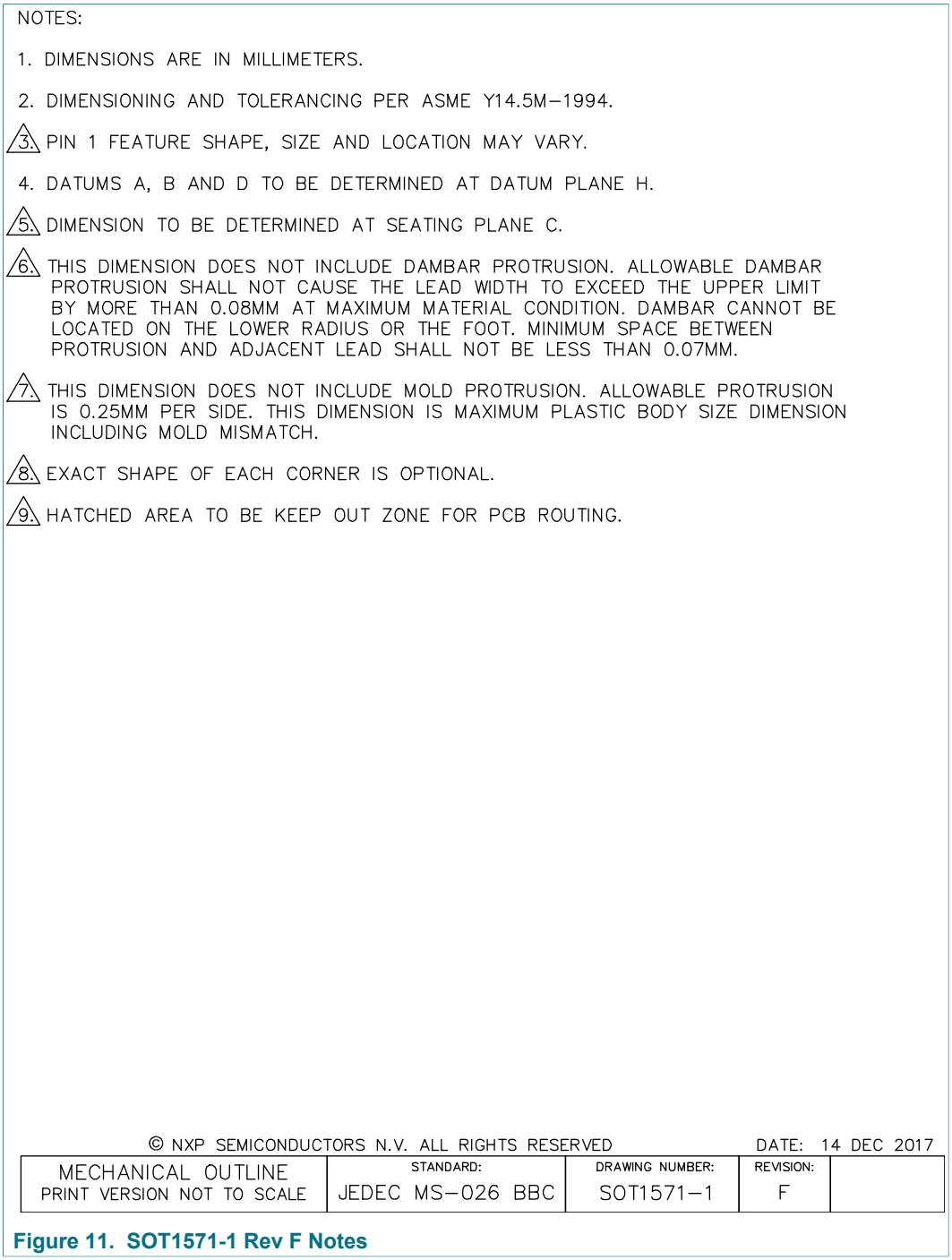
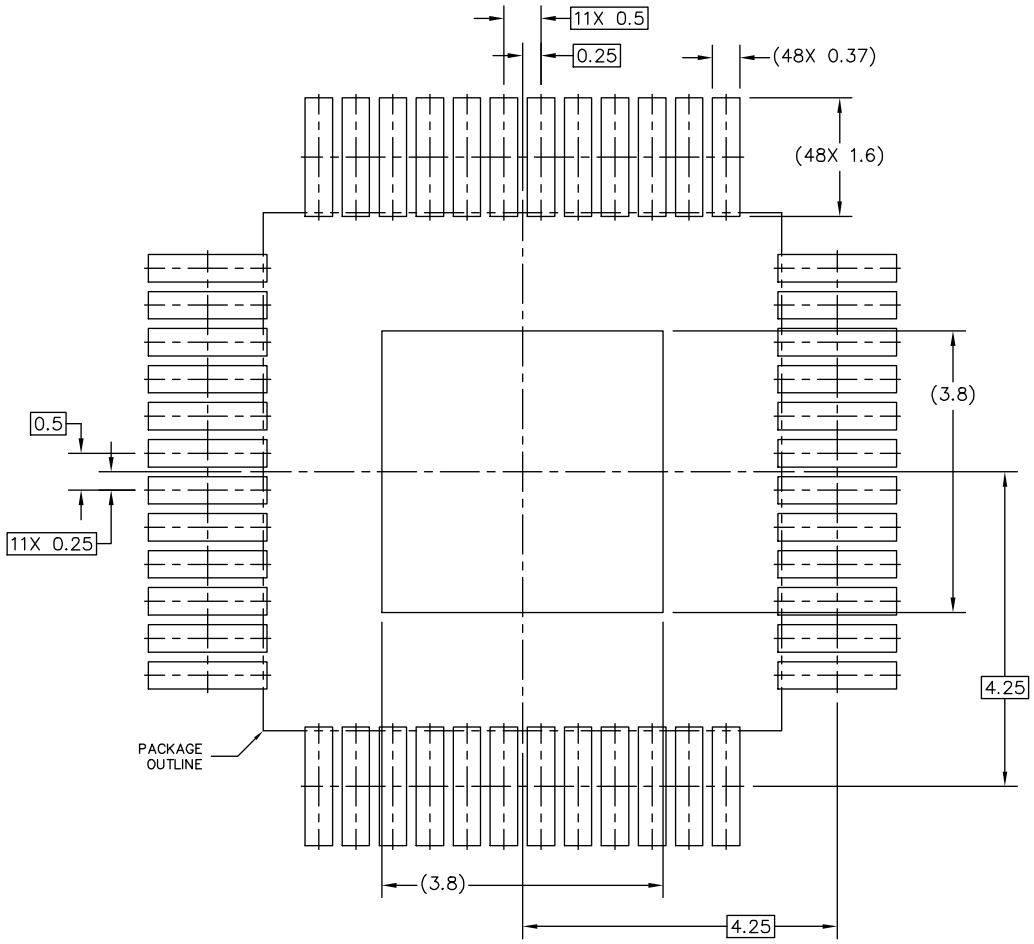


Figure 11. SOT1571-1 Rev F Notes

10 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

DATE: 14 DEC 2017

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: JEDEC MS–026 BBC	DRAWING NUMBER: SOT1571–1	REVISION: F	

Figure 12. SOT1571-1 Rev. F - PCB design guidelines - solder mask opening pattern

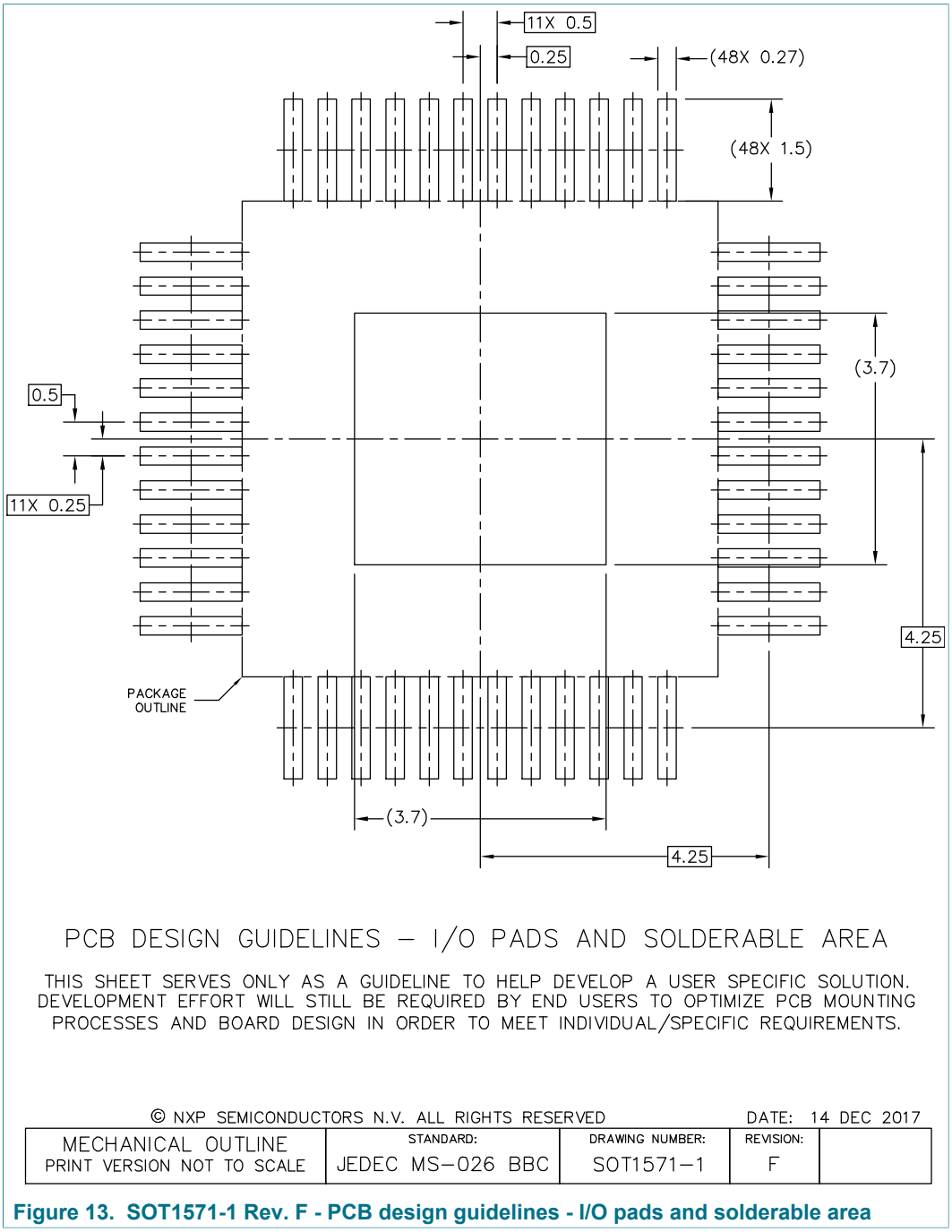


Figure 13. SOT1571-1 Rev. F - PCB design guidelines - I/O pads and solderable area

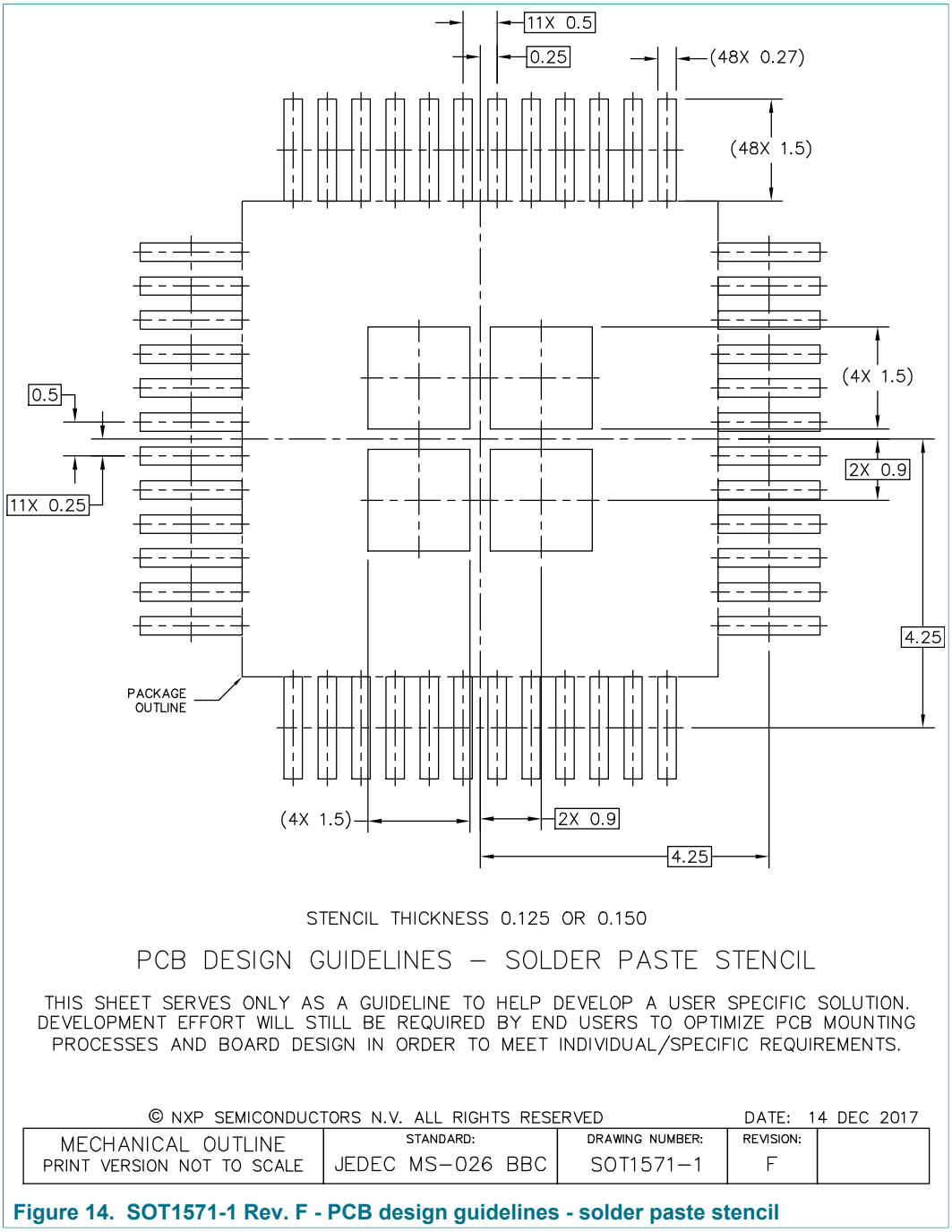


Figure 14. SOT1571-1 Rev. F - PCB design guidelines - solder paste stencil

11 References

Obtain additional information on related NXP products and application solutions through the documents and URLs listed below.

(1) **AN5238** - FS6500 and FS4500 Safe System Basis Chip Hardware Design and Product Guidelines - Application Note
https://www.nxp.com/AN5238-DOWNLOAD

(2) **AN4388** - Quad Flat Package (QFP)
https://www.nxp.com/files/analog/doc/app_note/AN4388.pdf

(3) **FS6500-FS4500PDTCALC** - Power dissipation tool (Excel File)
https://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx

(4) **V_{CORE} compensation network simulation tool (CNC)**[1]

(5) **FMEDA** - FS6500/FS4500 FMEDA[1]

(6) **FS6500-FS4500SMUG** - FS6500/FS4500 Safety manual – user guide
https://www.docstore.nxp.com/products/product-hierarchy?query=Sm5509

(7) **KITFS6522LAEEVM** - FS6522, System Basis Chip, DC-DC 2.2 A Vcore LDT, CAN, LIN
http://www.nxp.com/KITFS6522LAEEVM

(8) **KITFS6523CAEEVM** - FS6523, System Basis Chip, DC-DC 2.2A Vcore FS1B LDT CAN
https://www.nxp.com/KITFS6523CAEEVM

(9) **KITFS4503CAEEVM** - FS4503, System Basis Chip, Linear 0.5 A Vcore, FS1b, LDT, CAN
https://www.nxp.com/KITFS4503CAEEVM

(10) **FS6500 product summary page** -
https://www.nxp.com/FS6500

(11) **FS4500 product summary page** -
https://www.nxp.com/FS4500

(12) **Analog power management homepage** -
https://www.nxp.com/products/power-management

(13) **ISO 11898-2:2003** - Road vehicles — Controller area network (CAN) — Part 2: High-speed medium access unit
https://www.iso.org/standard/33423.html

(14) **ISO 11898-5:2007** - Road vehicles — Controller area network (CAN) — Part 5: High-speed medium access unit with low-power mode
https://www.iso.org/contents/data/standard/04/12/41284.html

(15) **ISO 7637-2:2011** - Road vehicles — Electrical disturbances from conduction and coupling — Part 2: Electrical transient conduction along supply lines only
https://www.iso.org/standard/50925.html

(16) **ISO 10605:2008** - Road vehicles — Test methods for electrical disturbances from electrostatic discharge
https://www.iso.org/standard/41937.html

(17) **IEC 61000-4-2:2008** - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test
https://webstore.iec.ch/publication/4189

(18) **JESD51- 6** - INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR)

(19) **JESD51-7** - HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES

(20) **JESD22-A114F** - ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM)

(21) **JESD22-C101F** - FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS

(22) **MIL-STD-883-1, Method 1012.1** - TEST METHOD STANDARD MICROCIRCUITS

(23) **LIN Specification Package Revision 2.1:2006**
https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN-Spec_Pac2_1.pdf

(24) **LIN Specification Package Revision 2.2A:2010**
https://www.lin-cia.org/fileadmin/microsites/lin-cia.org/resources/documents/LIN_2.2A.pdf

(25) **SAE J2602-2:201211 - LIN Network for Vehicle Applications Conformance Test**
https://www.sae.org/standards/content/j2602/2_201211/

[1] Available upon request.

12 Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
FS6500-FS4500SDS v.7.0	20201111	Product data sheet	—	FS6500-FS4500SDS v.1.0
Modifications	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors, N.V. Legal texts have been adapted to the new company name where appropriate. • Updated short data sheet revision number from v.1.0 to v.7.0 to align with the revision number of the full data sheet. • Changed product status from "Advance information" to "Product short data sheet". • Global: Performed minor grammar, punctuation, and typographical changes throughout the document. • Revised all images in Figures 1 through 7. • Section 1, added new paragraph beginning with "High temperature capability.…" • Section 2, removed the feature "36 V maximum input operating voltage". • Section 9.2, updated the package outline images and created separate figures for each drawing in Figure 9, Figure 10, and Figure 11 • Section 10, added new Soldering section and Figure 12, Figure 13, and Figure 14. • Section 11, Updated reference to FS6500-FS4500SMUG - FS6500/FS4500 Safety Manual – user guide and added industry standard documents referenced in the narrative.			
FS6500-FS4500SDS v.1.0	20171214	Data sheet: advance information	—	—
Modifications	• Initial release			

13 Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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