



# RF LDMOS Integrated Power Amplifiers

The AFIC31025N integrated circuit is designed with on-chip matching that makes it usable from 2400 to 3100 MHz. This multi-stage device is designed to support CW and pulse applications.

**Typical Performance:** In 2400–3100 MHz reference circuit,  $V_{DD} = 32 \text{ Vdc}$

Frequency (MHz)	Signal Type	$P_{out}$ (W)	$G_{ps}$ (dB)	$\eta_D$ (%)
2400–2500	CW	25	30.0	45.5
2700–3100	Pulse (300 $\mu\text{sec}$ , 15% Duty Cycle)	25 Peak	22.0	40.0

## Features

- On-chip matching (50 ohm input, DC blocked)
- Integrated quiescent current temperature compensation with enable/disable function (1)
- Qualified up to a maximum of 32  $V_{DD}$  operation
- Integrated ESD protection

## Typical Applications

- Civil S-Band radar
- Weather radar
- Maritime radar
- Industrial heating
- Data links
- Plasma generation

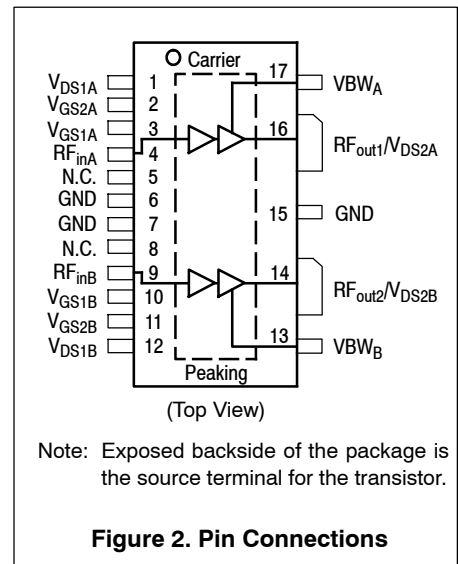
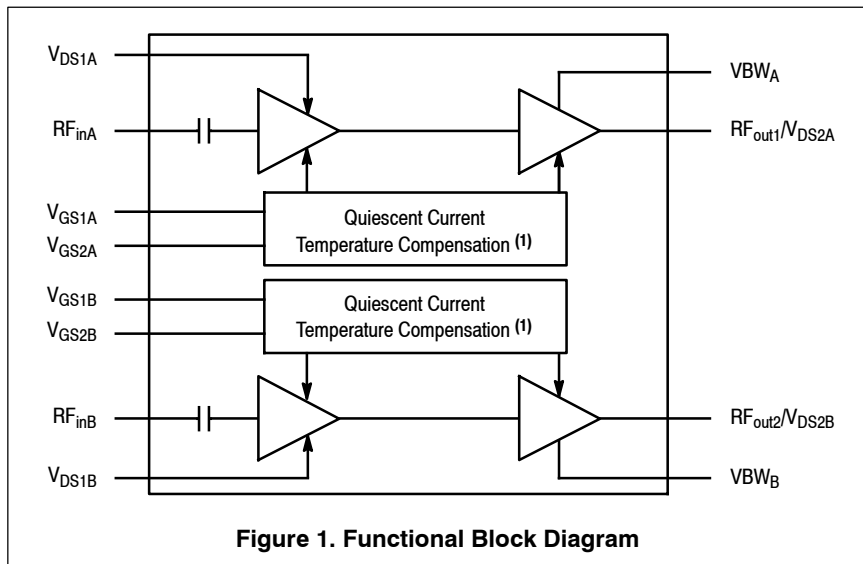
## AFIC31025N AFIC31025GN

2400–3100 MHz, 25 W PEAK, 32 V  
AIRFAST RF LDMOS  
INTEGRATED POWER AMPLIFIERS

TO-270WB-17  
PLASTIC  
AFIC31025N



TO-270WBG-17  
PLASTIC  
AFIC31025GN



1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*, and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.nxp.com/RF> and search for AN1977 or AN1987.



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +150	°C
Operating Junction Temperature Range (1)	$T_J$	-40 to +225	°C
Input Power	$P_{in}$	20	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, DC, Total $P_D = 29.3$ W Stage 1, 28 Vdc, $P_D = 3.8$ W Stage 2, 28 Vdc, $P_D = 25.5$ W	$R_{\theta JC}$	5.85 1.92	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B
Charge Device Model (per JESD22-C101)	II

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**Stage 1 - Off Characteristics** (3)

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.0$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 1 - On Characteristics**

Gate Threshold Voltage (3) ( $V_{DS} = 10$ Vdc, $I_D = 2.5$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1(A+B)} = 59$ mAdc)	$V_{GS(Q)}$	—	2.0	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_{DQ1(A+B)} = 59$ mAdc, Measured in Functional Test)	$V_{GG(Q)}$	4.6	5.3	6.1	Vdc

1. Continuous use at maximum temperature will affect MTF.

2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.

3. Each side of device measured separately.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 - Off Characteristics</b> <sup>(1)</sup>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.0\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>Stage 2 - On Characteristics</b>					
Gate Threshold Voltage <sup>(1)</sup> ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 16\ \mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2(A+B)} = 157\text{ mAdc}$ )	$V_{GS(Q)}$	—	1.9	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2(A+B)} = 157\text{ mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	4.3	5.0	5.8	Vdc
Drain-Source On-Voltage <sup>(1)</sup> ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 200\text{ mAdc}$ )	$V_{DS(on)}$	0.1	0.22	1.5	Vdc

1. Each side of device measured separately.

(continued)

**Table 5. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) **(continued)**

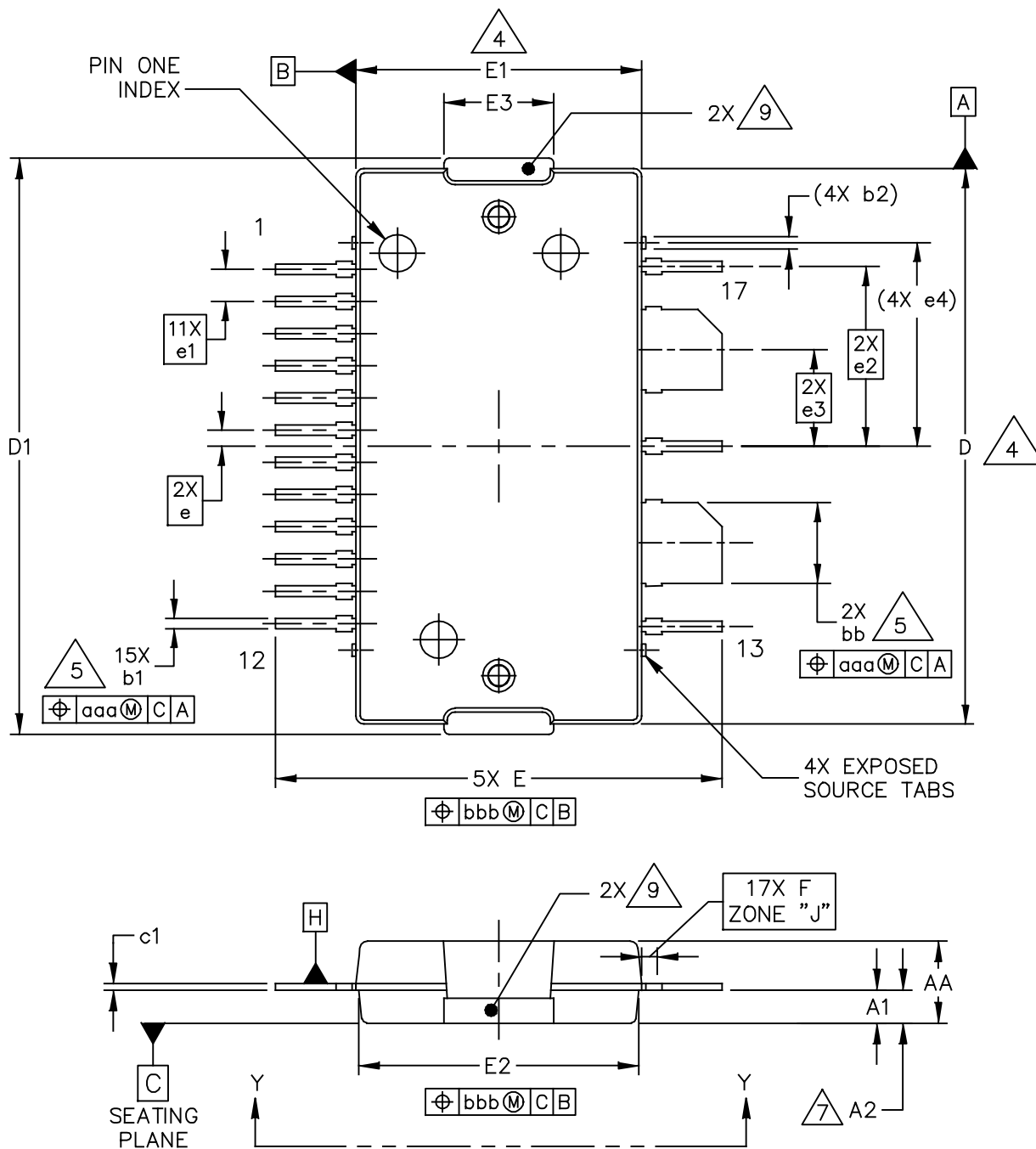
Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> (1,2) (In NXP Production Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1(A+B)} = 59\text{ mA}$ , $I_{DQ2(A+B)} = 157\text{ mA}$ , $P_{out} = 3.2\text{ W Avg.}$ , $f = 2690\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	30.5	31.9	34.5	dB
Power Added Efficiency	PAE	18.0	19.7	—	%
<b>Load Mismatch</b> (In NXP Production Test Fixture, 50 ohm system) $I_{DQ1(A+B)} = 59\text{ mA}$ , $I_{DQ2(A+B)} = 157\text{ mA}$ , $f = 2600\text{ MHz}$					
VSWR 10:1 at 32 Vdc, 36 W CW Output Power (3 dB Input Overdrive from 25 W CW Rated Power)	No Device Degradation				

**Table 6. Ordering Information**

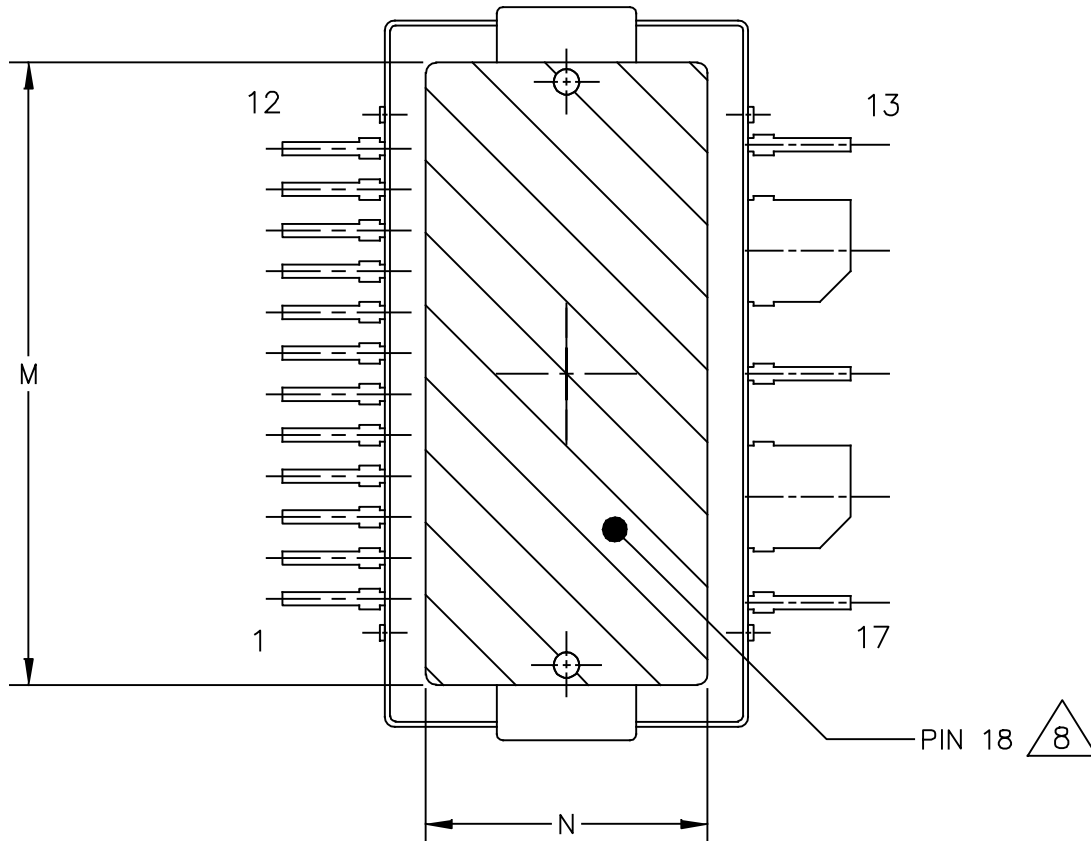
Device	Tape and Reel Information	Package
AFIC31025NR1	R1 Suffix = 500 Units, 44 mm Tape Width, 13-Reel	TO-270WB-17
AFIC31025GMR1		TO-270WBG-17

1. Part internally input and output matched.
2. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GN) parts.

PACKAGE DIMENSIONS



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE:  TO-270WB-17	DOCUMENT NO: 98ASA00583D	REV: B
	STANDARD: NON-JEDEC	
	SOT1730-1	21 JAN 2016



VIEW Y-Y

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE:  TO-270WB-17		DOCUMENT NO: 98ASA00583D	REV: B
		STANDARD: NON-JEDEC	
		SOT1730-1	21 JAN 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

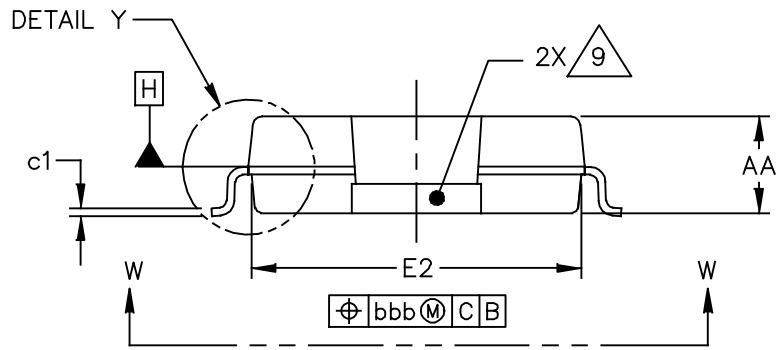
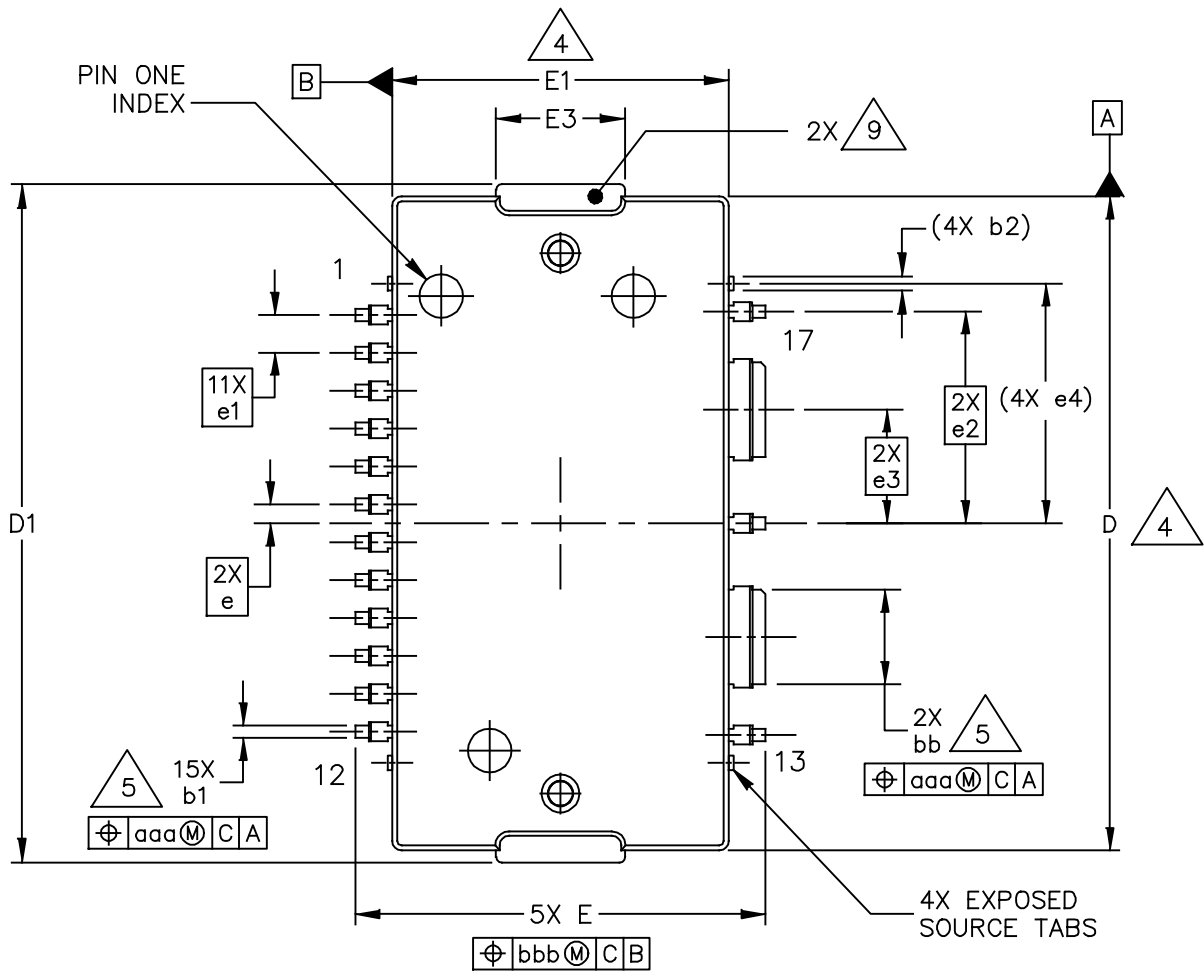
7. DIMENSION A2 APPLIES WITHIN ZONE J ONLY.

8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.

9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

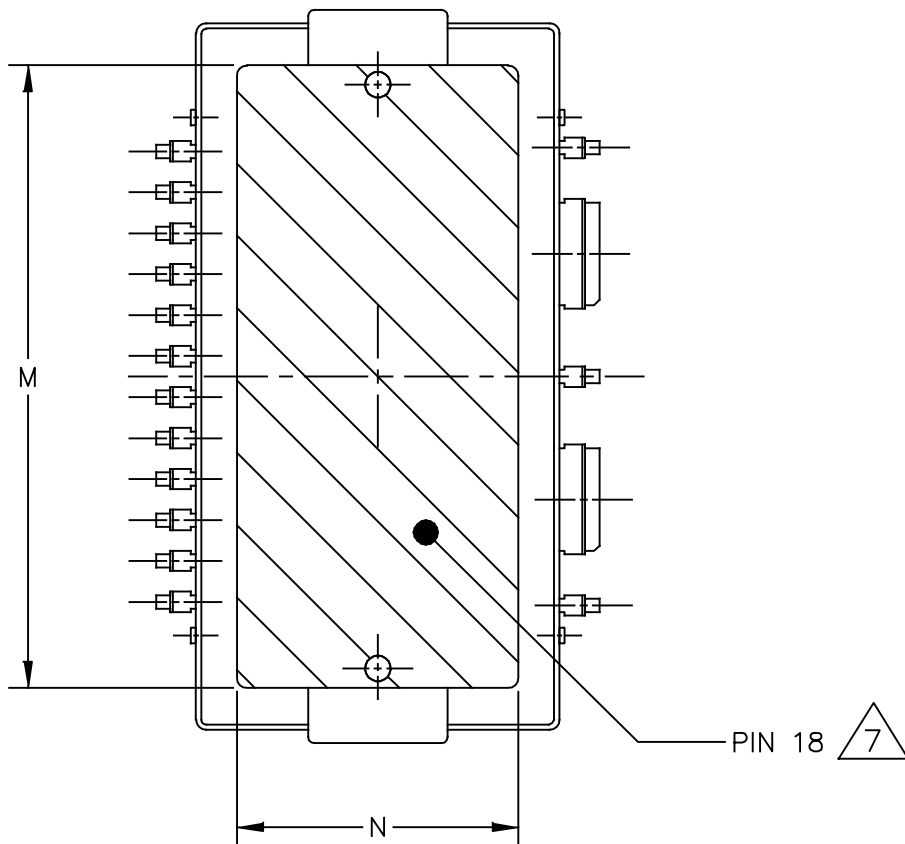
DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.551	.559	14.00	14.20	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
F	.025 BSC		0.64 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE		
TITLE:  TO-270WB-17			DOCUMENT NO: 98ASA00583D		REV: B	
			STANDARD: NON-JEDEC			
			SOT1730-1		21 JAN 2016	

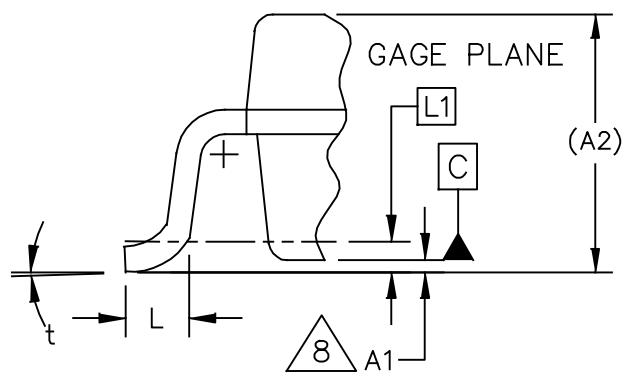


© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE:  TO-270WBG-17	DOCUMENT NO: 98ASA00729D	REV: B
	STANDARD: NON-JEDEC	
	SOT1730-2	12 JAN 2016





VIEW W-W



DETAIL "Y"

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE:  TO-270WBG-17	DOCUMENT NO: 98ASA00729D		REV: B
	STANDARD: NON-JEDEC		
	SOT1730-2	12 JAN 2016	

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS D AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS bb AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb AND b1 DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. DIMENSIONS M AND N REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF THE HEAT SLUG.
8. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM C. THE POSITIVE VALUE IMPLIES THAT THE BOTTOM OF THE PACKAGE IS HIGHER THAN THE BOTTOM OF THE LEAD.
9. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.099	.105	2.51	2.67	bb	.097	.103	2.46	2.62
A1	.001	.004	0.03	0.10	b1	.010	.016	0.25	0.41
A2	(.105)		(2.67)		b2	----	.019	----	0.48
D	.688	.692	17.48	17.58	c1	.007	.011	0.18	0.28
D1	.712	.720	18.08	18.29	e	.020 BSC		0.51 BSC	
E	.429	.437	10.90	11.10	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.223 BSC		5.66 BSC	
E2	.346	.350	8.79	8.89	e3	.120 BSC		3.05 BSC	
E3	.132	.140	3.35	3.56	e4	.253 INFO ONLY		6.43 INFO ONLY	
L	.018	.024	0.46	0.61	t	2'	8'	2'	8'
L1	.010 BSC		0.25 BSC		aaa	.004		0.10	
M	.600	----	15.24	----	bbb	.008		0.20	
N	.270	----	6.86	----					

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE:  TO-270WBG-17		DOCUMENT NO: 98ASA00729D      REV: B	
		STANDARD: NON-JEDEC	
		SOT1730-2	12 JAN 2016

## PRODUCT DOCUMENTATION

Refer to the following resources to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2017	<ul style="list-style-type: none"><li>• Initial release of data sheet</li></ul>

## ***How to Reach Us:***

**Home Page:**  
nxp.com

**Web Support:**  
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

NXP, the NXP logo, and Airfast are trademarks of NXP B.V. All other product or service names are the property of their respective owners.

© 2017 NXP B.V.

