IP and Session Initiation Protocol

IP Multimedia Subsystems

Overview

It's all about convergence in the network, systems and services. Services need to be accessible 24/7, whether they are wireless or wireline. An IP Multimedia Subsystem (IMS), as defined by 3GPP, provides an enabling architecture that is access independent. Based on IP and Session Initiation Protocol (SIP), IMS provides a highly versatile core that integrates session management, mobility and service quality all on a single platform.

IMS solutions will enable many types of access devices such as mobile phones, video phones, PDAs or laptops to access services through any type of network like cellular, broadband, Wi-Fi®, WiMax and PSTN. Below are examples of services enabled by IMS:

- **Video and Audio Conferencing—Multimedia Conferencing**
  Participants can be added and deleted as required.
- **Collaboration Groups**
  Individuals can share text, graphics, video and voice based on the capabilities of each user's access device.
- **Instant Messaging**
  Multimedia IM is the latest thing—plus text instant messages can be sent to any end device.
- **Push-to-Talk and Push-to-X**
  This "walkie-talkie" like service uses VoIP half-duplex communications for efficiency and speed. Over a cellular network, it's called push-to-talk over cellular (PoC). Also can include other types of communications beyond voice.
- **Dual-Mode Wi-Fi and Cellular Handsets**
  These new handsets enable the user to use VoIP over Wi-Fi (with a wireline connection to the Internet from the site) when the user is at home, at a business site or Wi-Fi hotspot, and cellular phone service when traveling.
- **Requests for Content**
  Consumers can request content from video applications like IPTV and video-on-demand (VoD) from a Web site to be delivered to any wireline or wireless device.

Design Challenges

The major design challenges for designing and implementing converged solutions are multimedia content, Quality of Service (QoS), programmability and scalability. Each challenge is unique and has its own special requirements, standards or concerns.

Multimedia Content

All systems need to support a wide variety of different types of media content such as VoIP, video and data. The system also needs the ability to adapt the content to suit the specific capabilities of the access device.

Quality of Service

Users may prefer certain trade-offs and subscribe to various levels of service. Operators want to offer differentiated services. Operators would like to define either global or user-specific service policies. For example, operators may want to make all emergency calls free or impose a lower tariff on data traffic at certain hours or to certain places.

Programmability

As the evolution of new standards in the voice and video industry continues, customers need to design using programmable solutions. This will provide the flexibility to easily modify or add new software modules to meet the industry's changing standards without the need for any hardware modifications.

Scalability

As the demand for IMS increases, operators need the ability to scale the number of users that can be supported in their system. To accommodate such needs, customers need to design modular architectures that can scale in number of channels and performance without impacting the power or size budgets.

Freescale Solutions

AdvancedTCA® based system solutions

- PowerQUICC™ and host processor boards (MPC8548, MPC8641, MPC83xx)
- DSP AMC boards (MSC8122, MSC8144)

Key Advantages of Freescale IMS Solutions:

Supports Convergence

- Addresses voice, video and data processing
- Supports extensive next-generation and legacy peripherals
- Supports multiprotocol migration for triple-play and IMS networks

Cost Effectiveness

- Achieves a new level of performance density for high-capacity infrastructure applications
- Offers industry's largest embedded memory to help increase channel densities and reduce total system cost, board space and power dissipation
- Highest performance at lowest power per channel

Compatibility

- Maintains binary compatibility for easy upgrade from today's SC140-based software
- Offers user-friendly high-level C code, control and DSP code

Devices:

MSC8144 DSP

- Four fully-programmable StarCore™ SC3400 DSP cores, each running at up to 1 GHz for a 4 GHz-equivalent performance
- 16 KB instruction cache and 32 KB data cache
- Memory Management Unit (MMU) for memory protection and address translation
- Debug and profiling unit
- Interrupt controller and timers
- 10.5 MB embedded memory—the industry's largest—in a single package
- 128 KB shared L2 cache
- Architecture highly optimized for voice, fax, video and data compression processing with industry-leading channel densities
- QUICC Engine™ communications technology—dual internal RISC-based packet-processing engine supporting multiple networking protocols for reliable data transport over packet networks while off-loading the processing from the DSP cores
- Supports next-generation and legacy interfaces:
  - 1x/4x Serial RapidIO®
  - Packet
    - Dual Ethernet controllers supporting RGMII, SGMII, MII, RMII, SMII
    - UTOPIA L2 50 MHz 8-/18-bit slave, supporting AAL1, AAL2, AAL5 ATM adaptation layers in firmware
  - TDM
    - 2048 DS-0 channels in eight independent ports
  - Host/Master
    - PCI—PCI 2.2 controller, master/agent, 32-bit at 66 MHz
  - External Memory Interface:
    - 16-/32-bit DDRI/DDRII at 400 MHz data rate, 32 channels DMA
  - Debug, Boot, Configuration:
    - I²C, UART, EonCE/JTAG
  - 29 mm x 29 mm FCPBGA package, 1 mm pitch

MSC8122 DSP

- Four 300/400/500 MHz StarCore SC140 DSP extended cores
- 16 ALUs on a chip deliver up to 4800/6400/8000 MMACS
- Performance equivalent to a 1.2/1.6/2.0 GHz SC140 Core
- 1436 KB of internal SRAM
- External bus configurable as:
  - 32-bit data system bus/64-bit direct slave interface (DSI)
  - 64-bit data system bus/32-bit DSI
  - Ethernet (MII/RMII)/32-bit system bus/32-bit DSI
- Four independent time-division multiplex (TDM) interfaces
  - 256 channels total for connectivity to T1/E1, MVIP, and H.110 interfaces
  - Up to 62.5 Mbps per TDM interface
- Flexible memory controller accesses various external memories, including SDRAMs, SRAMs, SSRAMs, EPROMs and flash
- Internal DMA controller that supports 16 time-multiplexed unidirectional channels, enabling data transfers of to and from the SC140 core M1 memory, the M2 memory, and the serial interfaces
- Ethernet interface designed to comply with IEEE® Std 802.3™, 802.3u™, 802.3x™ and 802.3ac™:
  - Gives direct access to internal memories via the DMA controller
  - Supports the 10/100 Mbps and 10 Mbps media-independent interfaces (MIIs), 10/100 Mbps reduced media-independent interface (RMII), and 10/100 Mbps serial media-independent interface (SMII)
- 20 mm x 20 mm flip chip ball grid array (FCBGA) package, available with lead-free or lead-bearing spheres

MPC8548 Host Processor

Based on the scalable e500 system-on-chip (SoC) platform and a processor core built on Power Architecture™ technology, the MPC8548/E PowerQUICC III processor delivers performance and features:

- Integrated L1/L2 cache
  - L1 cache—512 KB (8-way set associative); 512 KB/256 KB/128 KB/64 KB can be used as SRAM
- Integrated DDR memory controller with full ECC support, supporting:
  - 200 MHz clock rate (400 MHz data rate), 64-bit, 2.5V/2.6V I/O, DDR SDRAM
  - 333 MHz clock rate (up to 667 MHz data rate) DDR2 SDRAM
- MMU
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4 encryption algorithms
- Multiple PCI interface support
  - 64-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
  - 64-bit PCI-X bus controller (up to 133 MHz, 3.3V I/O)
- Four on-chip triple-speed Ethernet controllers (GMACs) supporting 10 and 100 Mbps, and 1 Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, RTBI and TBI physical interfaces
  - TCP/IP checksum acceleration
  - Advanced QoS features
- Serial RapidIO and PCI Express™ high-speed interconnect interfaces, supporting
  - Single x8 PCI Express, or
  - Single x4 PCI Express and single 4x Serial RapidIO
- Integrated four-channel DMA controller
- Dual I²C interfaces and Dual Universal Asynchronous Receiver/Transmitter (DUART) support
- General-purpose parallel I/O (GPIO)
- IEEE 1149.1 JTAG test access port
- 1.1V core voltage with 3.3V and 2.5V I/O
- 783-pin FC-BGA package

Software:

- Video: MPEG-4, H.263, H.264, H.324 MDSP (roadmap)
- ETSI/3GPP1 Vocoders: GSM-FR, GSM-HR, GSM-AMR/EFR, 3GPP AMR-WB
- TIA/3GPP2 Vocoders: IS127 EVRC, IS893 SMW
- ITU G.7xx Vocoders: G.711, G.711 App. 1 and 2 (PLC and VAD/CNG), G.722, G.723.1, G.726, G.726A, G.728, G.729B, G.729AB, G.729E
- Modem Pumps: V.23 Caller ID, V.34, V.90, V.92 V.42 MNP4 (error correction)
- Compression: V.44, V.42 bis, MNP5
- Negotiation: V.8, V.8 bis
- HDLC
- Relay: V.150.1 (MoIP)
- Fax Pumps: V.17, V.27ter, V.29
- Relay: T.30 (FoIP), T.38
- Echo cancellation G.165, G.168 (64 ms), G.168 2004 (128 ms, windowed), noise reduction, acoustic level control, Acoustic EC (roadmap)
- Telephony support DTMF detection, universal tone generation, special tone event detect, VAD/CNG, PLC, RTP packetization
- Security: AES
- Device Drivers: DMA driver, SRIO driver, TDM driver, Ethernet driver, PCI

Ecosystem or Tools:

Freescale CodeWarrior® Tools

- Integrated development environment
- ANSI 'C', 'C++' optimizing compilers
- Source level debugger
- SmartDSP OS—multi-core, royalty-free operating system
- Multi-core, royalty-free operating system
- Integrated device drivers (BSP)
- Integrated cycle and functional accurate simulators

Enea® OSEck RTOS

- OSEck real-time kernel
- Preemptive multitasking
- Multi-core DSP support
- OSEck soft kernel environment
- OSEck link handler
- OSEck illuminator
- Board support package (BSP)

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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