AN5238

FS6500 and FS4500 safe system basis chip hardware design and product guidelines

Rev. 10 — 27 August 2024 **Application note**

Document information

Information	Content
Keywords	FS6500, FS4500, ASIL B, ASIL D, CAN FD, LIN
Abstract	This application note provides design guidelines for integrating the FS6500 and FS4500 system basis chip (SBC) family of devices into automotive and industrial electronic systems.

1 Introduction

This application note provides design guidelines for integrating the FS6500 and FS4500 system basis chip (SBC) family of devices into automotive and industrial electronic systems. It shows how to optimize PCB layouts and gives recommendations regarding external components.

To minimize the EMC impact from embedded DC/DC converters, pay attention to PCB component routing when designing with the FS6500 and FS4500.

2 Overview

The FS6500 and FS4500 are multi-output power supply integrated circuits dedicated to the automotive market. They simplify system implementation by providing ISO 26262 system solutions, documentation and an optimized MCU interface enabling customers to minimize the cost and complexity of their designs. The FS6500 and FS4500 integrated EMC and ESD protections also facilitate less complex system designs with increased functional reliability.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow integrating precision analog, power functions, and dense CMOS logic together on a single cost-effective die.

This application note applies to all FS6500 and FS4500 part numbers in both versions ASIL D and ASIL B. LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. Other exceptions are specifically indicated. Compared to ASILD, ASIL B parts feature a simple Watchdog and do not provide LBIST or FCCU monitoring.

2.1 Typical block diagram

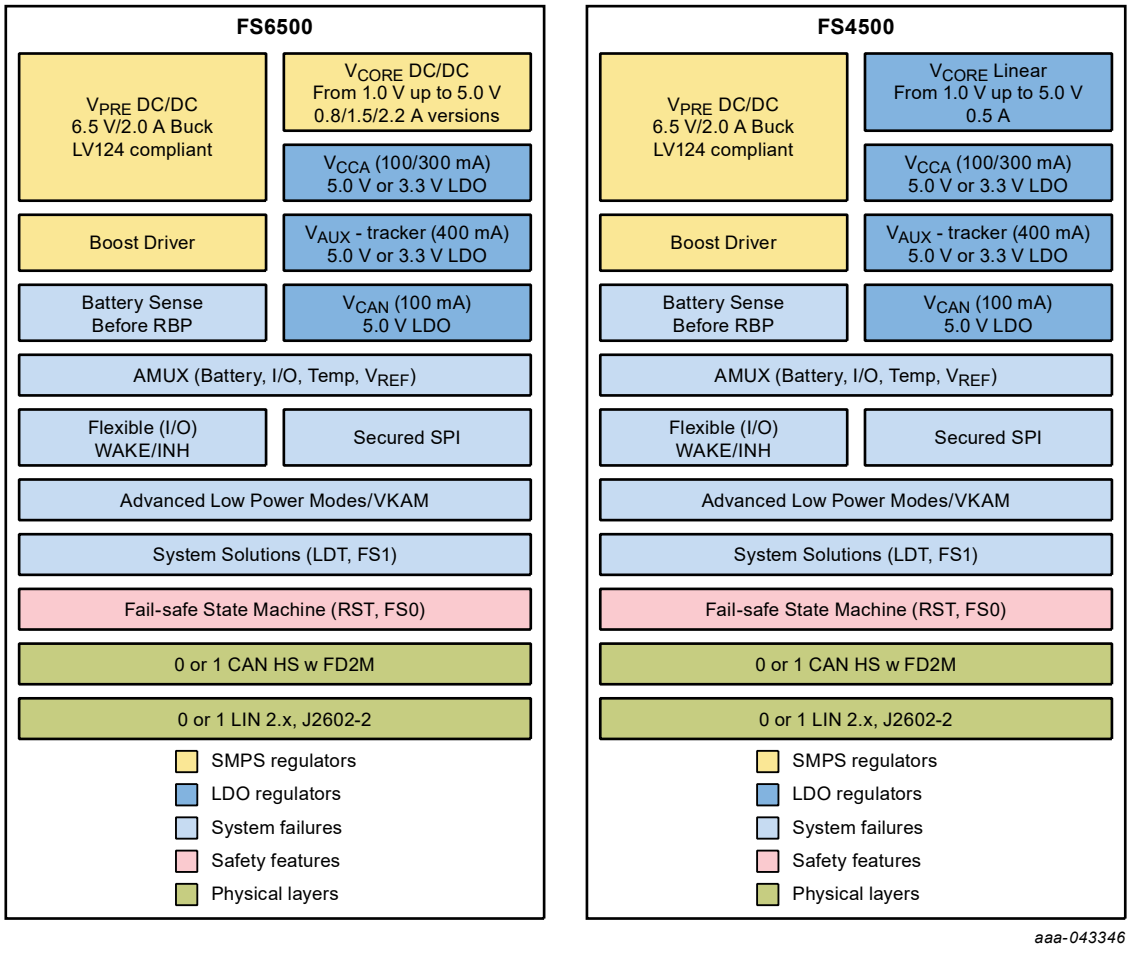


Figure 1. FS6500 and FS4500 block diagrams

2.1.1 Key features

- Flexible DC/DC buck pre-regulator with optional boost to fit with LV124
- Ultra low-voltage operation down to 2.7 V
- Scalable family of products supporting a wide range of MCU and power segmentation architectures
- Pin to pin compatible, backward compatible with MC33907/8 at the iso function
- SMPS core supply, from 1.0 V to 5.0 V, delivering up to 2.2 A on FS6500 series
- Linear core supply, from 1.0 V to 5.0 V, delivering up to 0.5 A on FS4500 series
- Analog multiplexer and battery sensing
- Long duration timer available in normal and low-power modes (1.0 s resolution)
- Low-power mode 32 µA
- Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT
- Secured SPI interface
- Robust CANFD (2.0 Mbit/s) and LIN physical layers with superior EMI/ESD performance
- Independent fail-safe state machine monitoring safety critical parameters and supporting functional safety standards
- Fail-silent safety strategy allowing fail-safe state without reset assertion
- Two fail-safe outputs with configurable timings between FS0B and FS1B
- Fit for ASIL D and ASIL B safety requirements

2.1.2 Typical applications

- Electrical power steering, engine/battery management
- Active suspension, gear box, transmission
- EV, HEV, inverter, ADAS
- Automation (PLC, robotics), medical (infusion pump, stairs)
- Building control (lift), transportation (military, mobile machine)

2.1.3 Part number selector guide

2.1.3.1 Part number breakdown for ASIL D parts

MC35FS c 5 x y z AE/R2 (Automotive) – Grade 0

Table 1. Part number breakdown – ASIL D parts

Code	Option	Variable	Description
c	4 series	V_{CORE} Type	Linear
	6 series		DCDC
x	0	V_{CORE} Current	0.5 A or 0.8 A
	1		1.5 A
y	0	Functions	None
	1		FS1B
	2		LDT
	3		FS1B and LDT
z	N	Physical Interface	None
	C		CAN FD

Table 1. Part number breakdown – ASIL D parts*...continued*

Code	Option	Variable	Description
Note: Refer to the data sheet for the exact list of part numbers available.			

MC33FS c 5 x y z AE/R2 (Automotive) – Grade 1

Table 2. Part number breakdown – ASIL D parts

Code	Option	Variable	Description
c	4 series	V_{CORE} Type	Linear
	6 series		DCDC
x	0	V_{CORE} Current	0.5 A for FS45 0.8 A for FS65
	1		1.5 A
	2		2.2 A
y	0	Functions	None
	1		FS1B
	2		LDT
	3		FS1B and LDT
	4		LDT and VKAM ON by default
z	N	Physical Interface	None
	C		CAN
	L		CAN and LIN
Note: Refer to the data sheet for the exact list of part numbers available.			

2.1.3.2 Part number breakdown for ASIL B parts

MC35FS c 5 x y z AE/R2 (Automotive) – Grade 0

Table 3. Part number breakdown – ASIL B parts

Code	Option	Variable	Description
c	4 series	V_{CORE} Type	Linear
	6 series		DCDC
x	0	V_{CORE} Current	0.5 A or 0.8 A
	1		1.5 A
y	5	Functions	None
	6		FS1B
	7		LDT
	8		FS1B and LDT
z	N	Physical Interface	None
	C		CAN FD
Note: Refer to the data sheet for the exact list of part numbers available.			

MC33FS c 5 x y z AE/R2 (Automotive) – Grade 1

Table 4. Part number breakdown – ASIL B parts

Code	Option	Variable	Description
c	4 series	V_{CORE} Type	Linear
	6 series		DCDC
x	0	V_{CORE} Current	0.5 A or 0.8 A
	1		1.5 A
	2		2.2 A
y	5	Functions	None
	6		FS1B
	7		LDT
	8		FS1B and LDT
z	N	Physical Interface	None
	C		CAN FD
	K		LIN only
	L		CAN FD and LIN
Note: Refer to the data sheet for the exact list of part numbers available.			

2.2 Voltage regulators

2.2.1 V_{PRE} voltage pre-regulator (SMPS)

V_{PRE} is a flexible switched-mode power supply working in PWM at a fixed 440 kHz frequency. V_{PRE} is a current mode controlled SMPS, with a fully integrated compensation network. V_{PRE} can be configured in two topologies:

non-inverting buck-boost or standard buck configuration. The output voltage is regulated at 6.5 V with 2.0 A current capability. V_{PRE} keeps power dissipation down and eliminates the need for bulky heat sinks compared to linear regulators for a wide input supply range from 2.7 V to 36 V.

2.2.2 FS6500 V_{CORE} voltage regulator (SMPS)

FS6500 V_{CORE} is a step-down switched-mode converter working in PWM at a fixed 2.4 MHz frequency dedicated to supplying the MCU core. V_{CORE} is a voltage mode controlled SMPS, with an external compensation network. The output voltage can be configured in a 1.0 V to 5.0 V range, with an external resistor bridge (a maximum of 1.0 % accuracy resistors are recommended) connected between V_{CORE} and the FB_CORE pin. The V_{CORE} output voltage accuracy is ±2.0 % (excluding external resistor accuracy) with a 0.8 A current capability for the FS650x family, 1.5 A for the FS651x family and 2.2 A for the FS652x family.

2.2.3 FS4500 V_{CORE} voltage regulator (linear)

FS4500 V_{CORE} is a linear voltage regulator dedicated to supplying the MCU core. The output voltage can be configured in a 1.0 V to 5.0 V range, with an external resistor bridge (a maximum of 1.0 % accuracy resistors are recommended) connected between V_{CORE} and the FB_CORE pin. The V_{CORE} output voltage accuracy is ±2.0 % (excluding external resistor accuracy) with a 0.5 A current capability for the FS450x family.

2.2.4 V_{CCA} voltage regulator (LDO)

V_{CCA} is a linear voltage regulator mainly dedicated to supplying the MCU I/Os, especially the ADC reference voltage. The output voltage is selectable at 5.0 V or 3.3 V, thanks to a resistor value connected to the SELECT pin. The V_{CCA} output voltage accuracy is ±1.0% with an output current capability of 100 mA. An external PNP transistor can be used to boost the current capability up to 300 mA with a ±3.0% output voltage accuracy.

2.2.5 V_{AUX} voltage regulator (LDO)

V_{AUX} is an auxiliary voltage regulator mainly dedicated to suppling additional devices in the ECU, additional MCU I/Os, or sensors outside the ECU. The external PNP is mandatory. V_{AUX} is protected against short to battery for up to 40 V. The output voltage is selectable at 5.0 V or 3.3 V, due to the resistor value connected to the SELECT pin. V_{AUX} output voltage accuracy is ±3.0 % with an output current capability of 400 mA. V_{AUX} can be configured as a tracker of V_{CCA} with a ±15 mV accuracy, when V_{AUX} is supplying a sensor and V_{CCA} the reference of the ADC, converting the sensor data to do ratio metric conversions.

2.2.6 CAN_5V voltage regulator

CAN_5V is a linear voltage regulator dedicated to the embedded CAN FD interface. If the internal CAN transceiver is not used in the application, the CAN_5V regulator can be used to supply an external standalone CAN or FLEX-RAY transceiver.

2.3 Built-in CAN FD transceiver

The built-in CAN FD interface meets the ISO11898-2 and -5 standards with flexible data standard at 2.0 Mbit/s. Local and bus failure diagnostics, protection, and fail-safe operation modes are provided. The CAN FD exhibits wake-up capability with a very low-current consumption. Refer to the data sheet to know which part number has CAN FD active.

2.4 Built-in LIN transceiver

The built-in LIN interface is compatible with the LIN protocol specification 2.0, 2.1, 2.2, and SAEJ2602-2. Local and bus failure diagnostics, protection, and fail-safe operation modes are provided. The LIN exhibits wake-

up capability with a very low-current consumption. Refer to the data sheet to know which part number has LIN active.

2.5 Analog multiplexer

The analog multiplexer allows multiplexing of the following voltages to be output from the FS6500 and FS4500 and connected to one of the MCU ADC channels. The MCU can use the information for monitoring purposes (refer to the data sheet for more details).

- 2.5 V internal reference voltage with a ±1.0 % accuracy
- Battery sense
- Analog inputs IO_0 and IO_5
- Die temperature T(°C) = (V_{AMUX} - V_{AMUX_TP}) / $V_{AMUX\_TP\_CO}$ + 165

A serial resistor can be added to filter the MUX_out pin before the MCU ADC input. This resistor is not mandatory, and depends on the application need and PCB layout performances. If a resistor is added, the MUX_out time constant is longer.

2.6 Configurable I/Os

The FS6500 and FS4500 includes five multi-purpose I/Os.

IO_0 and IO_4 are global pins and can be connected outside the ECU. They are load dump proof and robust against ISO 7637-2:2011 pulses with a serial resistor and a capacitor to limit the current and the negative voltage during the high transient pulse on the line.

IO_2/3 are local pins and must be connected inside the ECU.

IO_5 is shared with V_{KAM} output regulator and consequently rated at 20 V maximum. A zener diode in addition to a serial resistor is required if this IO is connected outside the ECU to be robust against load dump and ISO 7637-2:2011 pulses.

2.7 Safety outputs

The FS6500 and FS4500 has two safety outputs FS0B and FS1B. The FS0B pin is intended to take remedial action (disable actuators) after any critical fault detection within the system fault interval time (FTTI). The FS1B pin follows the activation of FS0B with a configurable delay or for a configurable duration. Both safety outputs are active low. Refer to the safety manual for more details on the safety implementation.

2.8 Fail-safe machine

To fulfill the safety-critical applications, a dedicated fail-safe machine (FSM) is provided. The FSM is composed of three main sub-blocks:

- Voltage supervisors
- Fail-safe output driver (FSO)
- Built-in self test (BIST)

The FSM is independent from the rest of the circuitry to avoid common cause failure. The FSM has its own voltage regulators (analog and digital), dedicated bandgap, and oscillator. This block is physically independent from the rest of the circuitry by doing dedicated layout placement and trench isolation.

2.9 Watchdog

According to the data sheet chapter 6.5.2.1, WD_ANSWER = NOT(WD_LFSR x 4 +6 – 4) /4. In order to correctly calculate the WD_ANSWER, based on the WD_LFSR, the MCU shall use unsigned integer operation on minimum 16 bits register. Note: this applies only to ASIL D. For ASIL B, a simple watchdog is implemented.

2.10 Low-power mode OFF

Before going to LPOFF, it is recommended to read the IO_INPUT register and verify IO_0 state. With default IO_0 wake-up configuration (rising edge or high level), IO_0 must be at a low level before sending the LPOFF SPI command. Otherwise, the device goes to LPOFF and immediately wakes up by the IO_0 high level state.

In low-power mode OFF (LPOFF), all the voltage regulators are turned off, except VKAM, if VKAM was ON before going to LPOFF. The MCU connected to V_{CORE} is not supplied. The FS6500 and FS4500 configuration monitors external events to wake-up and leave the LPOFF mode. Wake-up events can be generated via the CAN FD interface, LIN interface, I/O inputs, or long duration timer. A wake-up event triggers the regulators to turn on.

After wake-up from LPOFF, it is recommended to read the fault error counter and decrement it to an appropriate value by several consecutive good watchdog refreshes before a reset request by the SPI. The number of watchdogs needed (N) depends on the fault error counter value (FLT_ERR_2:0) and the WD refresh counter (WD_RFR_2:0) setup during INIT phase. N = FLT_ERR_2:0 x (WD_RFR_2:0 + 1) to decrement the counter to "0".

2.11 MCU programming

2.11.1 At customer assembly line

After PCB assembly, the first time the MCU is powered, the flash memory of the MCU is empty and must be programmed. To facilitate the programming, it is recommended to use the debug mode of the device applying the correct voltage at DEBUG pin as explained in Section 6.8. FS6500 and FS4500 Debug pin, page 34.
In debug mode, the CAN transceiver is in normal mode by default, ready to transmit and receive data, and the watchdog timeout is disabled by default, preventing to refresh good watchdog periodically. When the programming is complete, send the device to LPOFF_Auto_WU to restart the MCU from a power on reset and execute the software.

2.11.2 In-vehicle programming

For in-vehicle programming at the garage, if the debug mode cannot be used, the watchdog refresh can be disabled during INIT_FS state of the fail-safe logic to allow programming without taking care of the watchdog refresh. INIT_FS can be entered by a reset request with RSTB_REQ bit in SF_OUTPUT_REQUEST register. It is also recommended to disable the FCCU monitoring to avoid unexpected FCCU error detection during the programming by setting IO_23_FS bit at ‘0’ in INIT_FSSM register. The watchdog disable is effective when the INIT_FS is closed and requires at least one good watchdog refresh within the 256 ms of the INIT_FS timeout.

When the programming is complete, reset the MCU by a reset request with RSTB_REQ bit in SF_OUTPUT_REQUEST register to execute the new software and enable the watchdog again or send the device to LPOFF_Auto_WU to restart the MCU from a power on reset and execute the new software.

2.12 Simplified internal power tree

Figure 2 describes a simplified internal power tree to help understand basic concept between main part of the device and fail-safe part of the device.

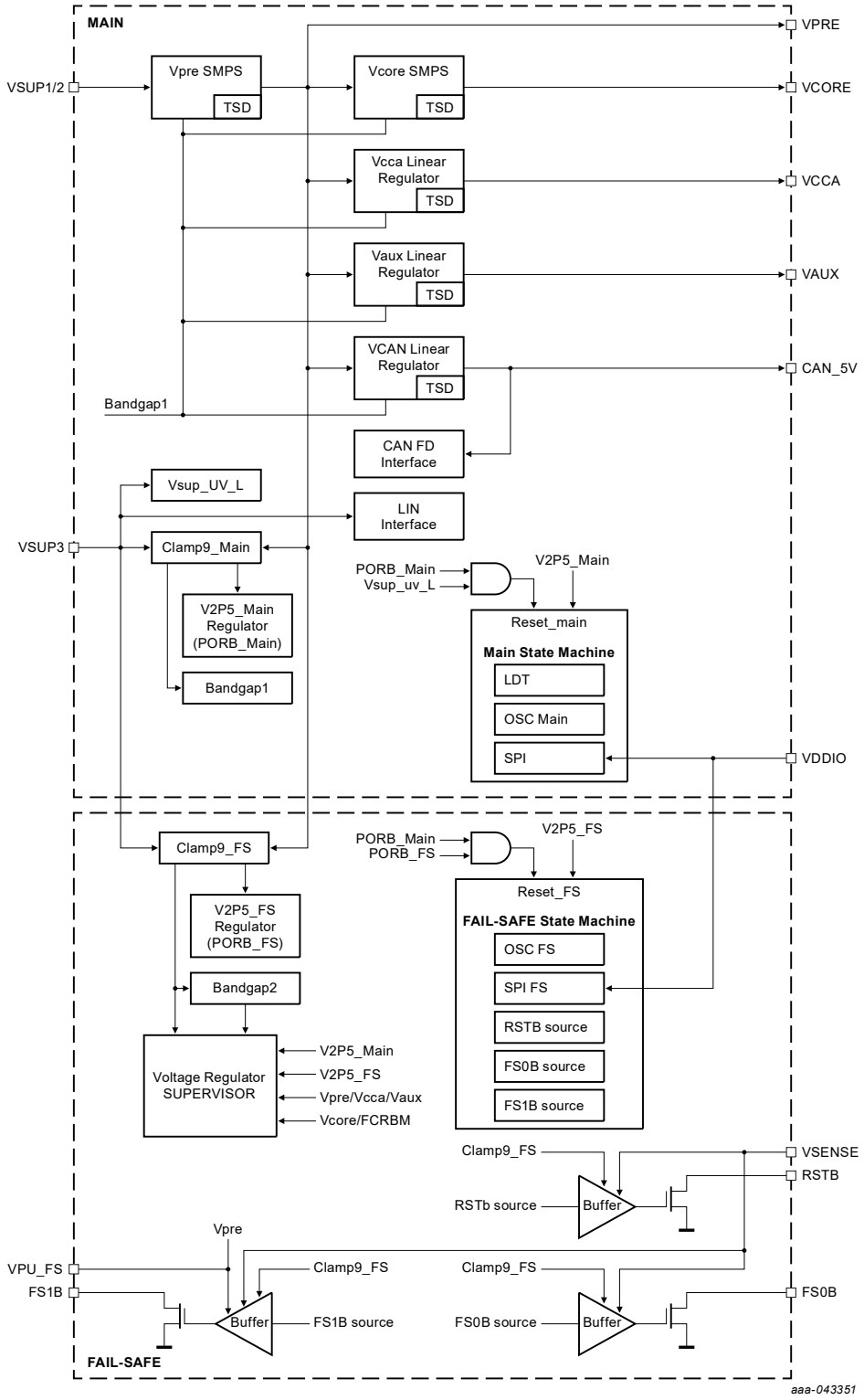


Figure 2. Simplified internal power tree

3 Known device behaviors

Table 5. Known behavior summary and workaround

Event	Behavior	AN Section	Workaround
LPOFF current spikes	Two current spikes could be observed after several minutes in LPOFF mode	Section 3.1	NA
LPOFF current excursion	Temporary excursion in the LPOFF quiescent current	Section 3.2	Mask INTB interrupt generation to remove this excursion.
FS1b time delay	tDELAY or tDUR time is not respected in specific configuration	Section 3.3	NA
No wake up by CAN	Part numbers without FS1B will not wake up by can if FS1B_CAN_IMPACT=1	Section 3.4	Configure FS1B_CAN_IMPACT=0 in INIT_FAULT register for part numbers without FS1B.
Unexpected OV/UV after wake up from LPOFF.	In case of wake up from LPOFF with a residual voltage on VPRE<3.4 V, VPRE_OV, VCORE_FB_OV, VCCA_OV, VAUX_OV, VSNS_UV flags can unexpectedly reported	Section 3.5	Read Diagnostic registers twice after wake up from LPOFF to filter unexpected flags.
Unexpected CAN_5V Ilim flag	If CAN TXD traffic is present when CAN_MODE bit is configured from sleep to normal mode, ILIM_CAN bit can be unexpectedly reported	Section 3.6	Configure CAN_MODE in normal mode before starting a transmission on CAN TXD.
FS1B backup delay automatically triggered	FS1B backup delay is triggered When VSUP is removed or when device goes to LPOFF mode	Section 3.7	Removing Cpd and Rpd in Vpu_fs Pin.
Unexpected FS1B release	FS1B glitch happens ~12 s after device power-up , results in FS1B being released gradually when FS1B is pulled up to VDDIO and FS1B_DLY_REQ=1 (S1 open), even when there is no FS1B release command	Section 3.8	Pull up FS1B to VPU_FS or set FS1B_DLY_REQ=0 before FS1B release when FS1B is pulled up to VDDIO.
CANH_BATT,CANH_GND, CANL_BATT,CANL_GND didn't report as expected	When CAN BUS is shorted to GND/battery, CANH_BATT,CANH_GND,CANL_BATT happen, diagnose bits did not report as expected.	Section 3.9	
ISO 7637-2 Pulse 2a (+112 V max) test fail when Pi filter inductor >2.2 µH	When Pi filter inductor $>$ 2.2 µH, it is possible that Vcore_UV, Vcca_UV, Vaux_UV reported when ISO 7637-2 pulse 2 a was injected.	Section 3.10	Select Pi filter inductor value ≤ 2.2 µH.
VAUX short to VBAT at start-up	When powering-up, if VAUX is shorted to VBAT, the RSTB pin is kept low until the short-circuit is removed, preventing application to run.	Section 3.11	Use dual common anode switching diode as protection
VAUX 3.3 V tracker regulating at 5 V during LBIST after wake-up	V_{AUX} starts up at 5.0 V after wake-up from LPOFF/DFS during LBIST execution (~12 ms) before regulating to 3.3 V when V_{AUX} = V_{CCA} = 3.3 V and VAUX tracker mode is enabled.	Section 3.12	Disable VAUX tracker mode or use an external tracker LDO if 3.3 V tracker function is a must.
VAUX 3.3 V tracker oscillation at light load	V_{AUX} oscillates between 3.3 V and 5 V after LBIST execution preventing RSTB release at light load.	Section 3.13	Disable VAUX tracker mode or use an external tracker LDO if 3.3 V tracker function is a must.
Fault error counter behavior when ABIST1 fails	Fault error counter value will be stuck at '2' and will not be incremented when RSTB or FS0B is asserted LOW when ABIST1 fails.	Section 3.14	Send 'LPOFF_AUTO_WU' SPI commands when ABIST1 failure is detected.

3.1 LPOFF current spikes

The current consumption on V_{SUP} in LPOFF mode is specified in the data sheet at 60 µA maximum at T_A = 80 °C. However, two current spikes could be observed after several minutes.

Measurements taken with KITFS6523CAEEVM at T_A = 80 °C in Figure 3 indicates :

- first spike at 90 µA after 17 minutes during 18 seconds
- second spike at 350 µA after 21 minutes during 30 seconds

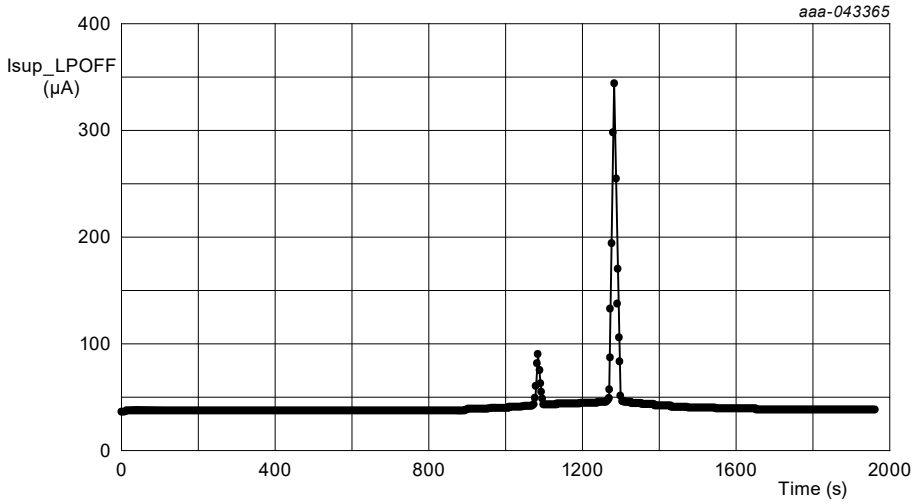


Figure 3. I_{SUP} LPOFF current versus time at T_A = 80 °C

The origin of these current spikes in LPOFF mode are due to VPRE bootstrap capacitor discharge. When the device goes in LPOFF, the bootstrap capacitor is discharged through leakages. It can take a long time to discharge at room temperature and it is accelerated by hot temperature. This time depends also on device manufacturing process and PCB parasitic. The current spike levels and timings measured on KITFS6523CAEEVM are for information only. It might differ at customer application.

During capacitor discharge some elements in the bootstrap circuitry are activated, consuming current from V_{SUP} and finally discharging the capacitor. It is a single event. When the bootstrap capacitor is fully discharge after these two current spikes, no more variation of the LPOFF quiescent current is visible.

3.2 LPOFF current excursion

A temporary excursion in the LPOFF quiescent current can be observed in the specific conditions described in the following list:

- ISUP_LPOFF current = 32 µA (typ.) when the device enters in LPOFF with VSUP < 7.7 V or VSUP > 8.3 V. When the device is in LPOFF, then ISUP_LPOFF current does not change with VSUP voltage.
- ISUP_LPOFF current = 1.7 mA (typ.) when the device enters in LPOFF with VSUP between 7.7 V and 8.3 V. When the device is in LPOFF, if VSUP moves < 7.7 V or > 8.3 V, then ISUP_LPOFF current goes back to 32 µA and does not change anymore with VSUP voltage.
- To trigger the ISUP_LPOFF excursion behavior, it is mandatory to enter in LPOFF with VSUP between 7.7 V and 8.3 V and to stay in this VSUP range.

This behavior is not temperature dependent and is visible on all the parts. This LPOFF current excursion can be removed if the INTB interrupt generation is masked with INT_INH_ALL bit in INIT_INT register.

3.3 FS1b time delay

The activation of FS1B follows the activation of FS0B with a configurable delay (tDELAY) or a configurable duration (tDUR).

In specific configurations FS1b will be activated after a specific time mentioned in the following table.

Table 6. FS1b Activation time

FS1b configuration	INIT_SF_ IMPACT register	Deep FailSafe	INIT_FS closing condition after RSTb assertion	FS1b
tDELAY config	RSTB and FS0b asserted low	disable	Good WD	Asserted after tDELAY config
			time out (256 ms)	Asserted after 4.7 s
			wrong WD sent after 37 ms	Asserted after 4.7 s
		enable	Time out or wrong WD	Asserted after 4.7 s deep failsafe when fault_err_ count=max value
tDUR config	RSTB and FS0b asserted low	disable	Good WD	Released after tDUR config
			time out (256ms)	Released after 4.7 s
			wrong WD after 37 ms	Released after 4.7 s
		enable	Time out or wrong WD	Never released deep failsafe when fault_err_count = max value

3.4 No wake up by CAN

Part numbers without FS1B will not wake up by CAN if FS1B_CAN_IMPACT=1. It is recommended to configure FS1B_CAN_IMPACT=0 in INIT_FAULT register to keep the CAN wake up capability.

3.5 Unexpected OV/UV when returning from low power off mode

In case of wake up from LPOFF with a residual voltage on VPRE (Vpre < 3.4 V), VPRE_OV,VCORE_FB_OV,VAUX_OV,VCCA_OV and VSNS_UV flags can unexpectedly be set to 1.

It is recommended to read Diagnostic registers twice after wake up from LPOFF to filter unexpected flags. In case of true failure, the flags will remain visible at the second reading.

3.6 Unexpected CAN_5V Ilim flag

If CAN TXD traffic is present when CAN_MODE bit is configured from sleep to normal mode, ILIM_CAN bit in DIAG_VSUP_VCAN can be unexpectedly reported.

Configure the CAN_MODE bit before starting a transmission on CAN TXD.

3.7 FS1B backup delay automatically triggered

This behavior happens when FS1B is configured in delay mode and pulled up to Vpu_fs. When Vsup is removed or when the device goes to LPOFF Mode, all fail safe registers are reset to their default values. FS1B_DLY_REQ bit in SF_OUTPUT_REQUEST register will be set to 1: Request FS1B assertion with Tdelay controlled by the backup delay (open S1). As a result, FS1B backup delay is triggered if Rpd and Cpd are connected to the Vpu_fs pin.

If FS1B is high when Vsup is removed or when device goes to LPOFF Mode, FS1B is asserted low with a delay after FS0B is activated. The delay time is defined by Rpd and Cpd in Vpu_fs pin. If FS1B is low when Vsup is removed or when device goes to LPOFF Mode, FS1B goes high as soon as Vsup < Vsup_UV_L (Buck-Boost Mode), Vsup < Vsup_UV_L_B (Buck Mode) or FS65 enters LPOFF mode. Then, FS1B return to low when Vpu_fs voltage drops to 3.2 V (typ). The duration of FS1B high is defined by Rpd and Cpd value in Vpu_fs pin.

The workaround is to remove Cpd and Rpd from the Vpu_fs pin if the triggered FS1B backup delay function is not expected when Vsup is removed or when device goes to LPOFF Mode in the application.

3.8 Unexpected FS1B release

This behavior happens when FS1B is pulled up to VDDIO and FS1B_DLY_REQ=1 (S1 open). An FS1B glitch happens ~12 s after the device powers up, resulting in FS1B being released gradually, even if there is no FS1B release command.

To prevent this behavior, pull FS1B up to Vpu_fs. Pulling up FS1B to Vpu_fs avoids the common cause failure when both FS0B and FS1B are pulled up to VDDIO. If the application requires that FS1B be pulled up to VDDIO, the FS1B_DLY_REQ bit in the SF_OUTPUT_REQUEST register must be set to 0 (Close S1) before the FS1B glitch happens.

3.9 CANH_BATT, CANH_GND, CANL_BATT, CANL_GND didn’t report as expected

CANL_GND/CANH_BATT did not report in some cases when a CAN BUS short to GND/battery occurs, because the voltage in the CANL/CANH pin did not reach the CANL_GND/CANH_BATT detection threshold. First, CANL short to GND is detected when CANL< 0.5 V, 500 ns after TXD is activated low, and five consecutive times have elapsed. 0.5 V is not the detection threshold. Different parts have different thresholds, but the max threshold < 0.5 V. CANH short to battery is detected when CANH > 5.2 V, 500 ns after TXD is activated low, and five consecutive times have elapsed. 5.2 V is not the detection threshold. Different parts have different thresholds, but the min threshold > 5.2 V. In another side, the injected position CANL short to GND/ CANH short to battery impacts the diagnostic bits report due to a voltage drop between the injected point and the CANL/CANH pins.

CANL_BATT/CANH_GND did not report in some cases when a CAN BUS short to battery/GND occurs, because ICANL or ICANH did not reach the CANL_BATT/CANH_GND detection threshold. First, CANL short to battery and CANH short to GND are detected when ICANL or ICANH > 75 mA (typ), 500 ns after TXD is activated low, and five consecutive times have elapsed. 75 mA is the typical threshold. Different parts have different thresholds, varying from 40 mA to 100 mA. In another side, there is usually a common choke in the CAN BUS to filter noise. This component prevents ICANL or ICANH from reaching the diagnostic threshold when a CAN BUS short to battery/GND happens.

3.10 ISO 7637-2 Pulse 2a (+112 V max) test fails when Pi filter inductor > 2.2 µH

The FS45/FS65 may report a Vcore_UV, Vaux_UV, Vcca_UV when injectingISO 7637-2 Pulse 2a(+112 V max) with Pi filter inductors with values greater than recommended (> 2.2 µH). Pi filters with higher values cause voltage gaps between Vsup1/2 and Vsup3 when the battery voltage oscillates. The FS45/FS65 data sheet says that “All VSUPS (VSUP1/2/3) must be connected to the same supply”. A 1 µH Pi filter inductor is recommended in the FS65 application schematic and the inductor value must not exceed 2.2 µH. To improve EMC performance for the whole board, add another inductor with a higher inductance (for a change) before the FS65.

3.11 VAUX short to VBAT at start-up

When the FS65-FS45 is powering-up while VAUX output is shorted to the battery voltage (VBAT), the RSTB pin is kept low, preventing the application from running. The only way to release RSTB, is to eliminate the short circuit. However, if the short circuit occurs after the FS65-FS45 is already awake and configured, the device reaction depends on the INIT_VAUX_OVUV_Impact register settings. Also, if VAUX is shorted to ground, this event will not occur since VAUX_FS_UV_1:0 default setting is “VAUX_UV does have an impact on FS0B only”.

When the product goes in LPOFF, its current configuration is lost, which means the default configuration will be taken into account when waking up again. In the default configuration, VAUX is configured as “safety critical” so

an OV (e.g. short to battery) triggers a RESET and keeps the safety pins asserted. After 8.0 s, the FS65-FS45 goes into DFS (Deep Fail-Safe) if enabled, or LPOFF.

Figure 4 shows a workaround for RSTB being held low because the VAUX output is shorted to battery voltage during power-up. This workaround uses a dual common anode switching diode as protection.

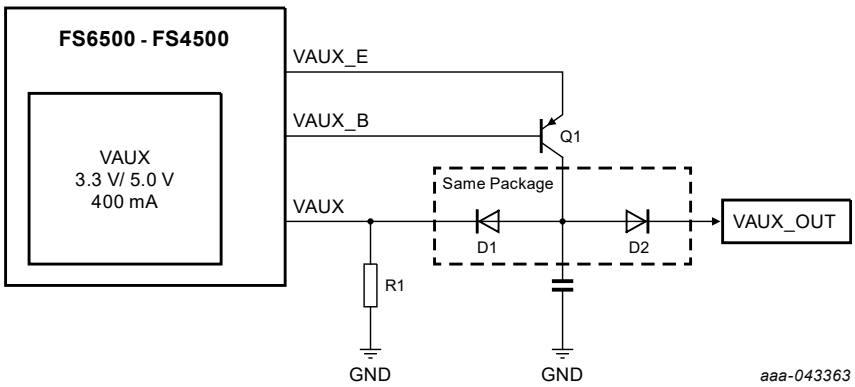


Figure 4. VAUX short to VBAT protection workaround

The same forward voltage for both diodes is achieved by keeping the dual common anode switching diodes in the same package with the same thermal coupling for both diodes (optimum would be on the same die) and by using the R1 pull-down resistor to balance the VAUX load current between the diodes.

This workaround is well fitted for light load currents on VAUX (e.g. ILOAD < ~50 mA). For higher current levels, R1 would have to dissipate too much power and VAUX accuracy would be impacted.

3.12 VAUX 3.3 V tracker regulating at 5 V during LBIST after wake-up

When the device wakes up from LPOFF or DFS mode, V_{AUX} delivers 5.0 V during LBIST execution (~12 ms) before regulating to 3.3 V when V_{AUX} = V_{CCA} = 3.3 V and VAUX tracker mode is enabled. See Figure 5.

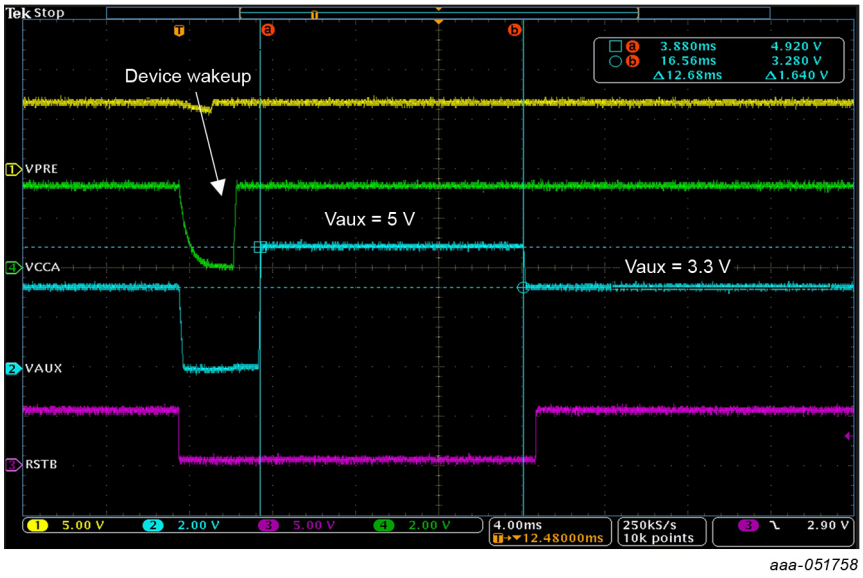


Figure 5. V_{AUX} 3.3 V tracker regulating at 5 V

The root cause is that the VAUX 3.3 V configuration is masked by the digital block if VAUX_TRK_EN = 1 when the device wakes up from LPOFF mode. Since the VAUX feedback resistor divider default configuration is

5.0 V, V_{AUX} starts up and remains at 5 V until the tracker mode is engaged when ABIST1 starts (after LBIST execution). After LBIST execution, V_{AUX} starts to track the V_{CCA} output voltage and regulates at 3.3 V.

The workaround is to disable VAUX tracker mode when V_{AUX} and V_{CCA} are configured at 3.3 V. V_{AUX} will regulate at 3.3 V after wake-up from LPOFF/DFS mode. If V_{AUX} 3.3 V tracker mode is a must, the customer is advised to use an external tracker LDO; the tracker LDO can be supplied by V_{PRE} with reference from V_{CCA} for tracking (see Figure 6).

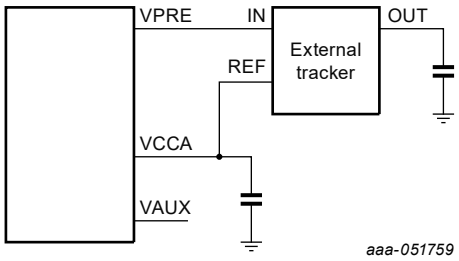


Figure 6. External tracker supplied by V_{PRE}

3.13 VAUX 3.3 V tracker oscillation at light load

When there is a light load at the VAUX output, V_{AUX} will oscillate between 3.3 V and 5 V after the transition from 5 V to 3.3 V, preventing pin RSTB being released.

The root cause is that the V_{AUX} transition time from 5 V to 3.3 V is greater than the V_{AUX} overvoltage filtering time (V_{AUX_OV}) when there is a light load on VAUX. As a result, V_{AUX} UV and OV events are triggered cyclically and V_{AUX} oscillates between 3.3 V and 5 V (see Figure 7).

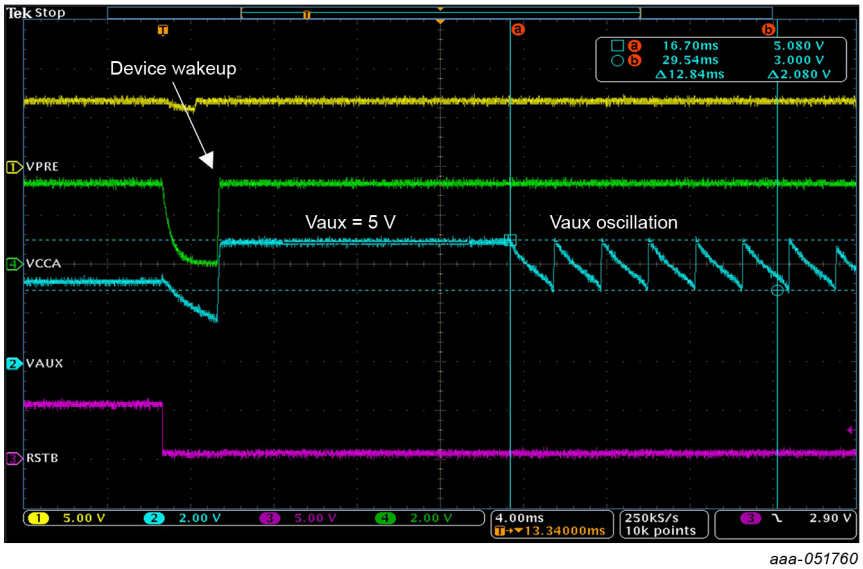


Figure 7. V_{AUX} oscillates between 3.3 V and 5 V when the load on VAUX is low

The workaround is the same as suggested for VAUX 3.3 V tracker regulating at 5 V in Section 3.12. Disable VAUX tracker mode or add an external tracker LDO.

3.14 Fault error counter behavior when ABIST1 fails

The fault error counter value is '1' by default after device POR or wake-up from LPOFF mode. However, the fault error counter value will be stuck at '2' and will not increase when RSTB or FS0B is asserted if ABIST1 has failed.

The workaround is to send an 'LPOFF_AUTO_WU = 1' command via SPI if an ABIST1 failure is reported after device power-up. Fail-safe digital will be reset, ABIST1 will be executed again and ABIST1 will pass if faults are removed.

4 Application schematic and unused pins configuration

4.1 Application schematic

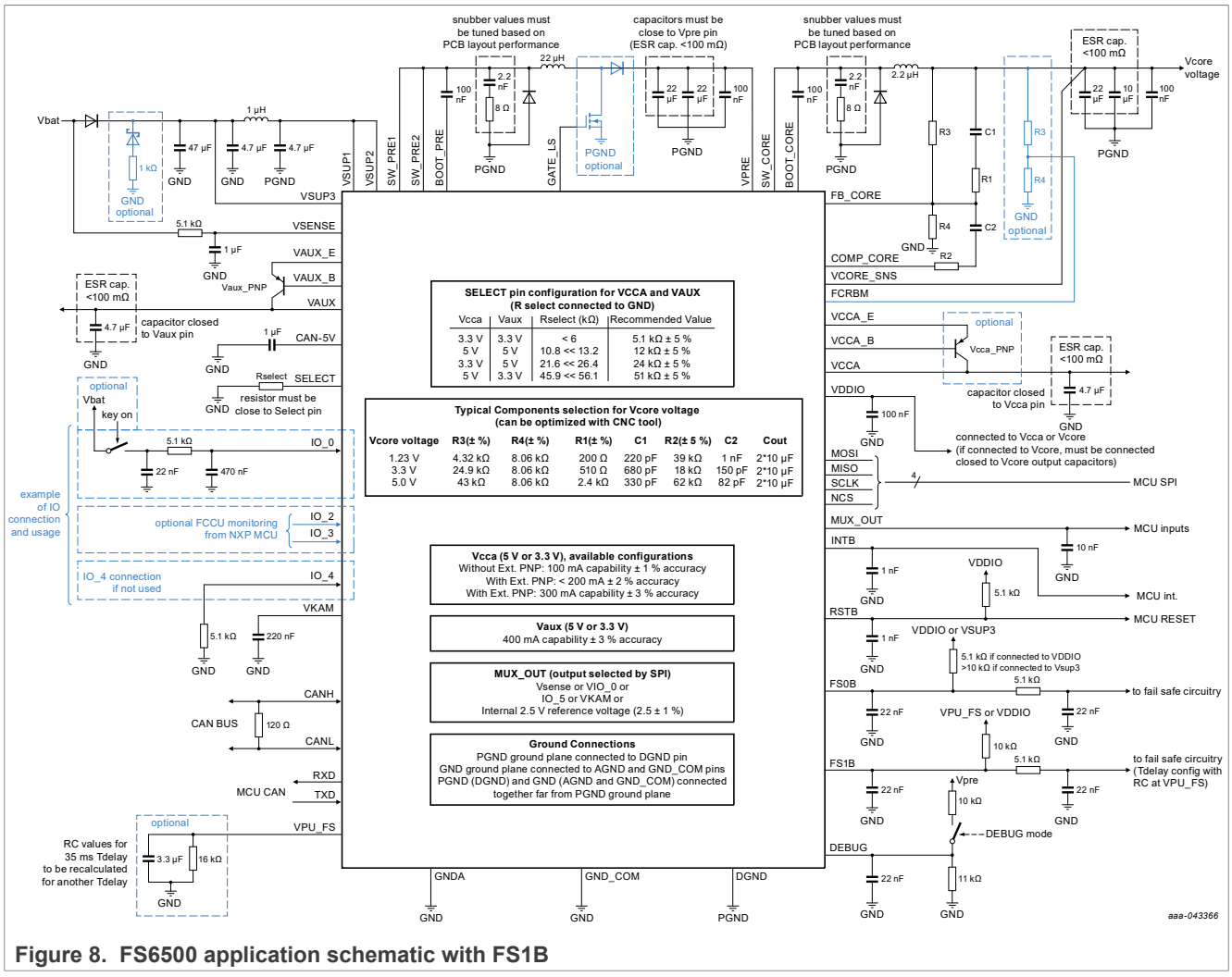


Figure 8. FS6500 application schematic with FS1B

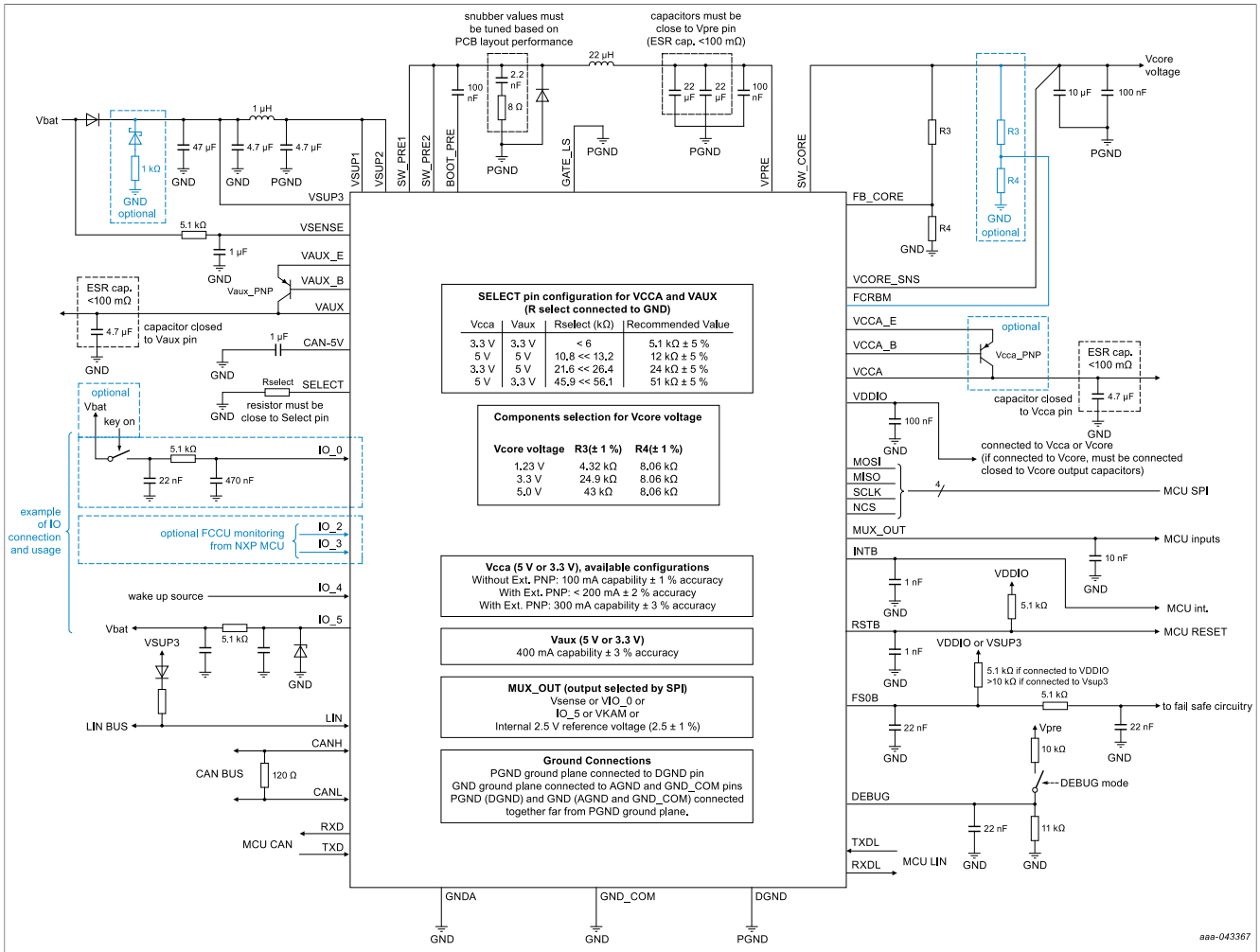


Figure 9. FS4500 application schematic with LIN

4.2 Connection of unused pins

Connection of unused pins

Pins	Name	Type	Connection if not used
1	VSUP1	A_IN	Connection mandatory
2	VSUP2	A_IN	Connection mandatory
3	VSESNSE	A_IN	Connection mandatory
4	VSUP3	A_IN	Connection mandatory
5	LIN	A_IN/OUT	Open
	or FS1B	D_OUT	Open - 4.0 MΩ internal pull-down to GND
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
6	GND_COM	GROUND	Connection mandatory
7	CAN_5V	A_OUT	Connection mandatory

Pins	Name	Type	Connection if not used
8	CANH	A_IN/OUT	Open
9	CANL	A_IN/OUT	Open
10	IO_4	D_IN A_OUT	External 5.1 kΩ pull-down to GND
11	IO_5/VKAM	A_IN D_IN A_OUT	External pull down to GND
	VKAM can be enabled or disabled by default at power-up. The differentiation is made by part numbers.		
12	IO_0	A_IN D_IN	External pull down to GND (DEEP fail-safe should be disabled - SELECT pin connected to VPRE)
13	FCRBM	A_IN	Connection mandatory (to the middle point of the redundant resistor bridge or to FB_CORE directly)
14	FS0B	D_OUT	Open - 4.0 MΩ internal pull-down to GND
15	DEBUG	D_IN	Connection mandatory (to GND in application run mode)
16	AGND	GROUND	Connection mandatory
17	MUX_OUT	A_OUT	Open
18 19	IO_2:3	D_IN	External pull down to GND/Open
20	TXD	D_IN	Open - 33 kΩ internal pull up to VDDIO
21	RXD	D_OUT	Open - push pull structure
22	TXDL	D_IN	Open - 33 kΩ internal pull up to VDDIO
	or VPU_FS	A_OUT	Open
	LIN and FS1B functions are exclusive. The differentiation is made by part numbers. When LIN is available, FS1B is not, and vice versa. If neither LIN, nor FS1B functions are used, this pin must be left open.		
23	RXDL	D_OUT	Open - push pull structure
24	RSTB	D_OUT	Connection mandatory
25	MISO	D_OUT	Connection mandatory
26	MOSI	D_IN	Connection mandatory
27	SCLK	D_IN	Connection mandatory
28	NCS	D_IN	Connection mandatory
29	INTB	D_OUT	Open - 10 kΩ internal pull up to VDDIO
30	VDDIO	A_IN	Connection mandatory
31	SELECT	D_IN	Connection mandatory
32	FB_CORE	A_IN	Connection mandatory
33	COMP_CORE	A_OUT	Connection mandatory
34	VCORE_SNS	A_IN	Connection mandatory

Pins	Name	Type	Connection if not used
35	SW_CORE	A_OUT	Connection mandatory
	or VCORE	A_OUT	Connection mandatory
36	BOOT_CORE	A_IN/OUT	Connection mandatory
37	VPRE	A_IN	Connection mandatory
38	VAUX	A_OUT	Open
39	VAUX_B	A_OUT	Open
40	VAUX_E	A_OUT	Open
41	VCCA_E	A_OUT	Connection mandatory
42	VCCA_B	A_OUT	Open
43	VCCA	A_OUT	Connection mandatory
44	GATE_LS	A_OUT	Connection mandatory
45	DGND	GROUND	Connection mandatory
46	BOOT_PRE	A_IN/OUT	Connection mandatory
47	SW_PRE2	A_OUT	Connection mandatory
48	SW_PRE1	A_OUT	Connection mandatory

5 Optional configurations

According to customer application needs, optional configurations for the FS6500 and FS4500 are described in the following sections.

5.1 Pre-regulator, buck or buck-boost configuration

Two topologies are available on the FS6500 and FS4500 for the V_{PRE} pre-regulator. The FS6500 and FS4500 can be configured in buck only or buck-boost converter mode according to the GATE_LS pin connection. The detection is done automatically during the startup sequence, from power on reset or after each wake-up from LPOFF.

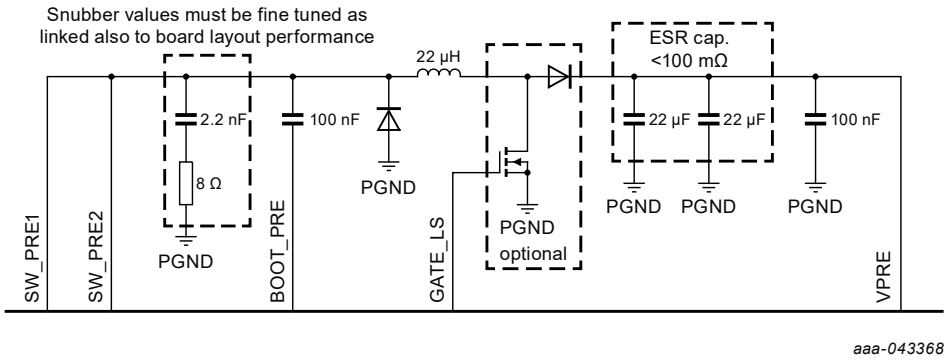


Figure 10. Buck-boost configuration

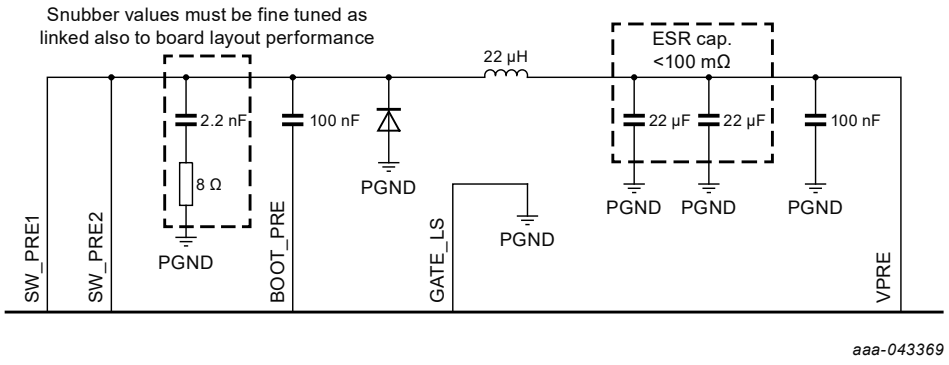


Figure 11. Buck configuration

In buck-only configuration, the external low-side MOS and the diode are removed, and the Gate_LS pin must be connected to ground (PGND or GND).

5.2 V_{CCA}, current capability

To increase the current capability from 100 mA to 300 mA on the V_{CCA} linear regulator, an external PNP transistor must be connected. Using an external PNP increases the current capability and reduces the accuracy from ±1.0 % at 100 mA to ±3.0 % at 300 mA.

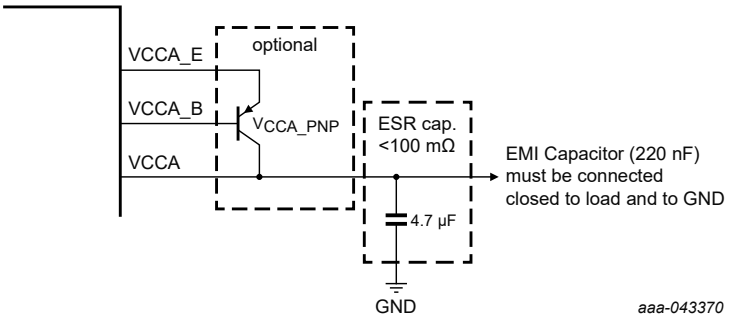


Figure 12. V_{CCA} current capability 300 mA, ±3.0 % accuracy

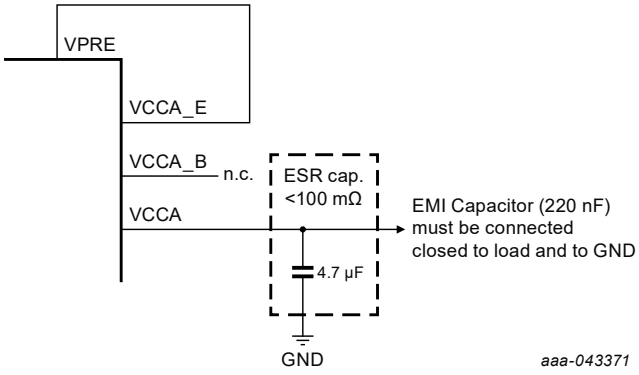


Figure 13. V_{CCA} current capability 100 mA, ±1.0 % accuracy

When no external PNP is connected to V_{CCA}, the VCCA_E pin must be connected to the VPRE pin.

5.3 V_{AUX}

Depending on application needs, the auxiliary regulator can be used. Figure 10 shows the correct connections of V_{AUX} with the mandatory external PNP.

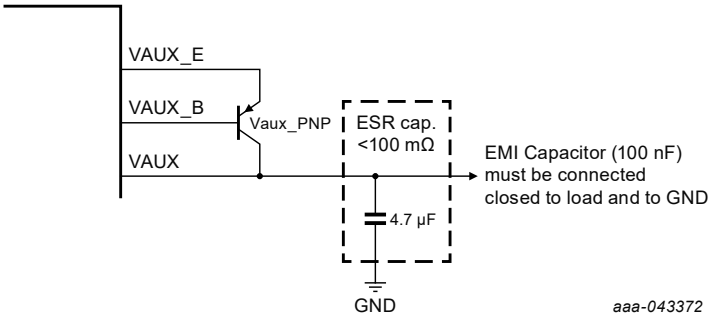


Figure 14. V_{AUX} current capability 400 mA, ±3.0 % accuracy

When V_{AUX} is not used, VAUX_E, VAUX_B and Vaux pins must be left open. In this situation, VAUX_UV flag is set and cannot be cleared. This is an expected behavior since VAUX is not starting in this situation. As a consequence, VOTHERS_G bit is also set and cannot be cleared since VOTHERS_G = ILIM_CCA or TWARN_CCA or TSD_CCA or ILIM_CCA_OFF or VCCA_UV or VCCA_OV or ILIM_AUX or TSD_AUX or ILIM_AUX_OFF or VAUX_OV or VAUX_UV or ILIM_CAN or VCAN_UV or VCAN_OV or TSD_CAN.

5.4 Feedback Core Resistor Bridge Monitoring (FCRBM)

When the application targets the ISO 26262 ASIL D or ASIL B safety level, it is recommended to monitor the V_{CORE} output voltage through FCRBM. In that case, a second resistor bridge is needed, which is a duplication of the R3/R4 external resistor bridge used to create V_{CORE} from FB_CORE. Refer to the safety manual for more information. If the second resistor bridge (R3b/R4b) is not mounted, FCRBM must be connected directly to FB_CORE to satisfy FB_CORE = FCRBM in all conditions.

5.5 IO_0 ignition connection

In automotive applications, it is recommended to connect IO_0 to the ignition to be able to recover from deep fail-safe state by a key OFF, key ON action. IO_0 is a global pin and can be connected outside the ECU. It is load dump proof and robust against ISO 7637-2:2011 pulses with a serial resistor R_IO[0] and a capacitor Cout1_IO[0] to limit the current and the negative voltage during the high transient pulse on the line. It is robust against ESD GUN test up to ±8.0 kV, with a filtering capacitor Cout2_IO[0].

Cout1_IO[0] must be placed close to the device pin and Cout2_IO[0] must be placed close to the module connector. Recommended values are R_IO[0] = 5.1 kΩ, Cout1_IO[0] = 470 nF, and Cout2_IO[0] = 22 nF.

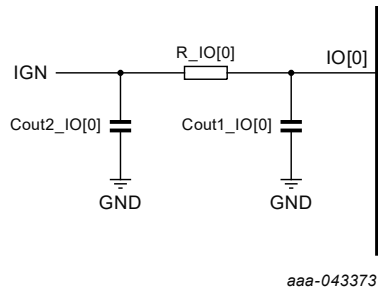


Figure 15. IO_0 connection to IGN

5.6 IO_2 and IO_3, FCCU monitoring for ASIL D only

IO_2 and IO_3 can be configured as safety inputs to allow monitoring of the NXP microcontroller FCCU output pins FCCU_E[0] and FCCU_E[1]. IO_2 should be connected to FCCU_EF[0] and IO_3 to FCCU_E[1]. A 5.1 kΩ pull-up resistor must be connected to IO_3/FCCU_E[1] and a 10 kΩ pull-down resistor to IO_2/FCCU_E[0]. Bi-stable protocol only from MCU is supported. If not used, IO_2 and IO_3 can be left open or pulled down to GND. Refer to the safety manual for more information.

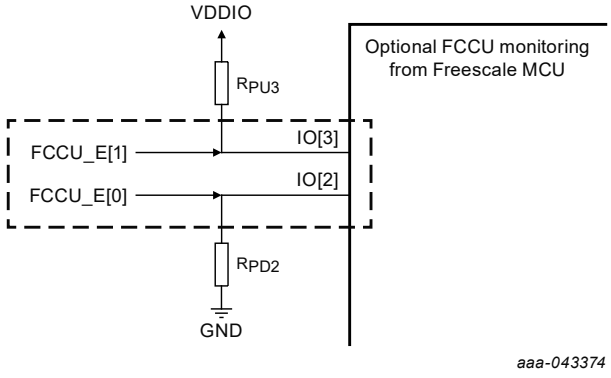


Figure 16. IO_2 and IO_3 configured as safety inputs

5.7 IO_5 connected outside the ECU

If IO_5 is connected outside the ECU, a zener diode ZD[5], in addition to a serial resistor R_IO[5] and a capacitor Cout1_IO[5], is required to limit the current and the negative voltage during the high transient pulse on the line. It is robust against an ESD GUN test up to ±8.0 kV, with the filtering capacitor Cout2_IO[5]. Cout1_IO[0] must be placed close to the device pin and Cout2_IO[0] must be placed close to the module connector.

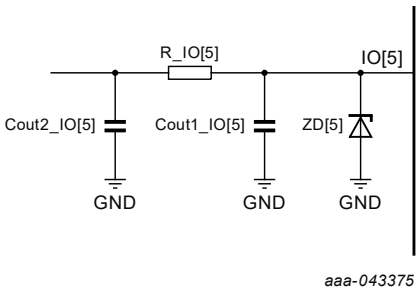


Figure 17. IO_5 connected outside the ECU

Table 7. IO_5 component list

Component	Value	Reference/manufacturer proposal	Ground connection
Cout1_IO[5]	470 nF		
Cout2_IO[5]	22 nF		GND
ZD[5]		BZT52H-C20/NXP MMSZ5250BT1G/ON Semiconductor	GND
R_IO[5]	5.1 kΩ		

5.8 VKAM

VKAM is a keep alive memory supply, available in LPOFF to supply the static RAM of the MCU (usually named VSTBY at MCU side), but it can also be used for other use cases where VKAM would fit. It provides a 3.3 V supply with 3.0 mA maximum current capability and requires an external capacitor between 100 nF and 1.0 µF to work properly. A 220 nF output capacitor is recommended. VKAM is ON by default in part numbers FS65x4.VKAM is OFF by default in other part numbers, and can be turned ON by the SPI. VKAM current consumption depends on the VKAM current load.This dependence is shown in Figure 14 to illustrate the data sheet parametric performances.

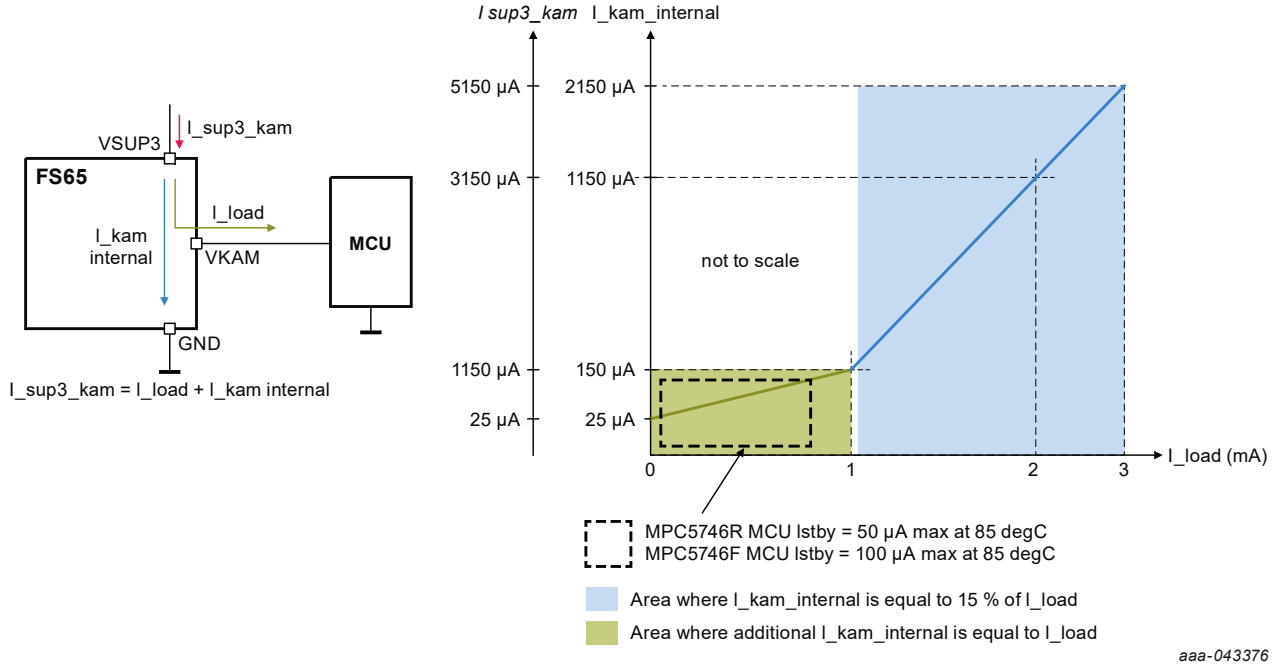


Figure 18. VKAM current consumption depends on VKAM load current

5.9 CAN ESD protection

CAN ESD protection option 2 is recommended to pass J2962-2 certification for the American market.

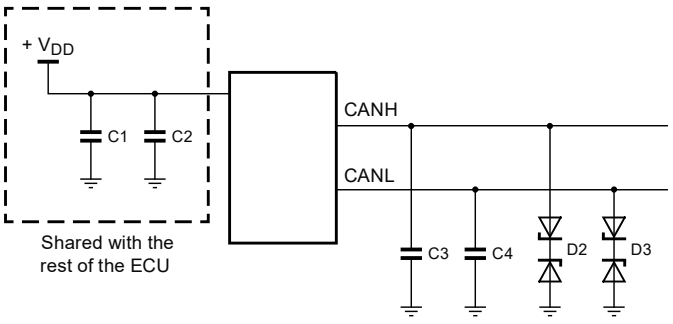


Figure 19. CAN ESD protection - J2962-2 option 2

Table 8. CAN ESD protection component list

Option No.	Component name	Label	Value
2	Capacitor	C3, C4	82 pF, 100 V ±5 % (1)
	Zener	D2, D3	NXP PESD1CAN, (in same SOT23 package)

Note
1. Over the entire voltage and temperature operating range

6 FS6500 and FS4500 external components

This section is based on Figure 4 and Figure 5, and details how to select the external components. It also proposes some references and tolerances needed to ensure optimal performance of the system. All the recommended components are based on NXP use case validations.

6.1 FS6500 and FS4500 power supply

Power to the FS6500 and FS4500 is provided by the VSUP1, VSUP2, and VSUP3 supply pins. An external reverse battery protection diode must be connected between the VBAT external battery input and the capacitor input filter.

A PI filter is implemented to avoid current switching noises coming from DC/DC converters to be propagated to V_{BAT} and V_{SUP3} supplies. For that reason, VSUP3 must be connected before the PI filter to deliver a clean supply to the FS6500 and FS4500, de-correlated from the VSUP1 and VSUP2 dedicated to the VPRE SMPS pre-regulator.

The C_{BAT} capacitor between the VBAT and VSUP pins must be greater than 47 µF, to limit the slew rate on VSUP pins, in case of high transients. The resistor connected to VSENSE is mandatory to limit the current at the pin, in case of high transients (positive and negative).

If the application has to sustain ISO pulses on VBAT in LPOFF mode, the connection of a an external zener diode (D_{IP}) and a serial resistor to ground (R_{IP}) is needed to discharge the C_{BAT} capacitor.

If the application has to pass J2962 certification for American automotive market, a ferrite bead (FB) on the V_{BAT} line is recommended to pass the radiated emission test. The FS6500 and FS4500 power connection is shown in Figure 16.

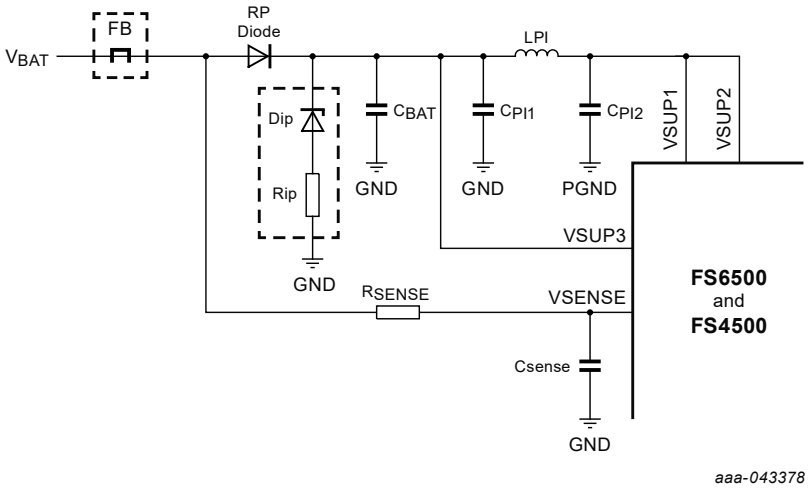


Figure 20. Power supply connection

The PI filter has a resonance frequency at

$$f\_res = \frac{1}{2\pi \times \sqrt{LPI \cdot CPI}}$$

with a filtering slope at –40 dB per decade.

The V_{PRE} pre-regulator is the main contributor to the noise reported to V_{BAT}. The resonance frequency of the PI filter must be f_res < V_{PRE} switching frequency (f_res < F_{SWPRE} < 440 kHz). LPI = 1.0 µH and CPI = 4.7 µF,

giving a resonance frequency f_res = 73 kHz. The resonance frequency of the PI filter can be adjusted at the application level to improve EMC performances.

Table 9. Power supply component list

Component	Value	Reference/manufacturer proposal	Ground connection
FB		MPZ1608S101ATAH0/TDK	
RP Diode		PMEG10030ELP/NXP (I_F = 3 A, V_R = 100 V) PMEG10020ELR/NXP (I_F = 2A, V_R = 100 V) SBRS81100T3G/On Semiconductor (I_F = 2A, V_R = 100 V)	
Dip	Zener 30 V	BZX384C/NXP	
R_{IP}	1.0 kΩ		GND
C_{BAT}	47 µF	EMVH500ADA470MJA0G/NIPPON CHEMI-CON CORPORATION	GND
CPI1	4.7 µF	GCM32ER71H475K/Murata	GND
LPI	1 µH	B82472G6102M000/TDK-EPCOS	
CPI2	4.7 µF	GCM32ER71H475K/Murata	PGND
R_{SENSE}	5.1 KΩ		
C_{SENSE}	1.0 µF	CGA5L3X7R1H105K/Murata	GND

6.2 FS6500 and FS4500 V_{PRE} pre-regulator

The V_{PRE} pre-regulator delivers a 6.5 V typical output voltage.

- In buck only configuration, the Gate_LS pin must be tied to PGND or GND.
- In buck-boost configuration, an external logic level MOSFET (N-type) must be connected to the Gate_LS pin and an additional diode is needed, as shown in Figure 6.

The two C_{OUT_VPRE} capacitors in parallel can be replaced by one 47 µF capacitor, but with always ESR < 100 mΩ. The V_{PRE} pre-regulator connections are shown in Figure 17.

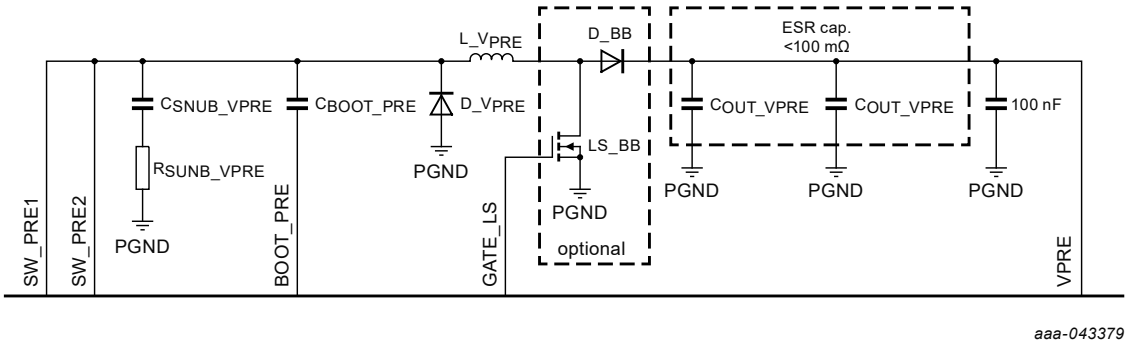


Figure 21. V_{PRE} connections

6.2.1 V_{PRE} main characteristics

- V_{SUPMAX} = 36 V
- V_{SUPMIN} = 2.7 V
- V_{PRE} = 6.5 V
- $V_{PRE\_MAXRATING}$ = 8.0 V

- I_{PREMAX} = 2.0 A
- I_{PREMIN} = 0.3 A (in boost mode when V_{SUP} < 4.0 V)
- F_{SWPRE} = 440 kHz

6.2.2 L_V_{PRE} calculation

- Inductor current ripple: I_{RIP} = K x I_{PREMAX} = 0.6 A with K = 0.3 (30% of I_{PRE})
- Buck configuration:

$$LVpre = \frac{(Vpre \times (Vsupmax - Vpre))}{K \times Vsupmax \times Ipremax \times Fswpre}$$

- Boost configuration:

$$LVpre = \frac{(Vsupmin^2 \times (Vpre - Vsupmin))}{K \times Vpre^2 \times Ipremin \times Fswpre}$$

- From calculation, L_V_{PRE} = 20.6 µH in buck mode and L_V_{PRE} = 16.6 µH in boost mode
- From normalized value, recommended L_V_{PRE} = 22 µH
- The current discharge slope in the inductor is:

$$\frac{-Vpre}{LVpre}$$

with V_{PRE} = 6.5 V and L_V_{PRE} = 22 µH, I_{SLOPE} = –300 mA/µs.

- V_{PRE} is a current mode controlled SMPS with a –500 mA/µs internal slope compensation to avoid sub-harmonic oscillations when the duty cycle is > 50%. A minimum L_V_{PRE} must be chosen to maintain the current discharge slope in the inductor lower than the internal slope compensation.

6.2.3 L_V_{PRE} selection

- Must be shielded inductor
- Inductor value: 22 µH

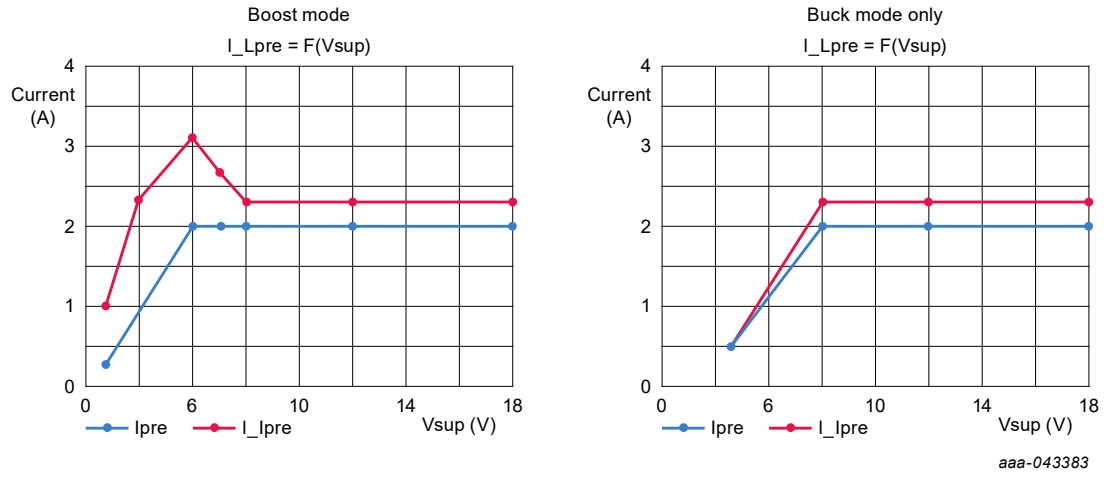


Figure 22. Peak current in the inductor

- Buck mode only:
  - rated current: $I_R > I_{PREMAX} > 2.0$ A
  - saturation current: $I_{SAT} > I_R + (I_{RIP}/2) > 2.3$ A
- Buck/boost mode (80 % efficiency considered in boost mode):
  - rated current: $I_R > I_{SUP} > 2.7$ A
  - saturation current: $I_{SAT} > I_{SUP} + (I_{RIP}/2) > 3.1$ A
- Serial resistance: DCR < 100 mΩ

6.2.4 D_V_{PRE} selection

- Schottky diode is recommended
  - lower forward voltage drop (V_F) reduces power dissipation
  - lower parasitic capacitor improves EMC performance
- Reverse voltage: $V_R \geq V_{SUPMAX} \geq 36$ V
- Average rectified forward current: $I_F > I_{PREMAX} + (I_{RIP}/2) > 2.3$ A
- Power dissipation: $P_D = V_F \times I_F$

6.2.5 LS_BB selection

- Must be logic level N-type MOSFET
- Low $R_{DS(on)}$ reduces conduction losses
- Drain source voltage: $V_{DS} > V_{PRE\_MAXRATING} + V_{F(D\_BB)} > \sim 9.0$ V
- Drain current: $I_{DS} > I_{PREMAX} + (I_{RIP}/2) > 2.3$ A
- Gate source capacitance:

$$Cgs = \frac{(Iboost \times Trise)}{Vpre}$$

With I_{BOOST} = 300 mA and t_{RISE} = 30 ns, C_{GS} = 1.5 nF.

6.2.6 D_BB selection

- Schottky diode is recommended
  - lower forward voltage drop (V_F) reduces power dissipation
  - lower parasitic capacitor improves EMC performance
- Reverse voltage: $V_R \geq V_{PRE\_MAXRATING} \geq 8.0$ V
- Average rectified forward current: $I_F > I_{PREMAX} + (I_{RIP}/2) > 2.3$ A
- Power dissipation: $P_D = V_F \times I_F$

6.2.7 Output capacitors

- Minimum 40 µF ceramic capacitor(s) with low ESR << 100 mΩ is recommended
- The ESR of the output capacitor is one of the main contributor to the output voltage ripple. The ripple generated by the ESR is proportional to its value (ESR * I_{RIP}). A high ripple can disturb the regulation loop.
- Low ESR capacitors reduce the ripple, avoid instability and lower EMI.

6.2.8 Snubber

In asynchronous SMPS, a freewheeling diode is used to discharge the inductor (during recirculation phase). When this diode is turned OFF (corresponding to when the MOS is turned ON), some oscillations happen due to the leakage inductance and output capacitance of the diode plus the PCB layout parasitic. A RC snubber in parallel to the diode dampens these oscillations and lower EMI. The snubber improves EMI but impact efficiency lowering the turn ON and OFF switching times. Its implementation is a compromise between EMI performance and Efficiency. The damping effect of a well designed snubber is shown in Figure 19.

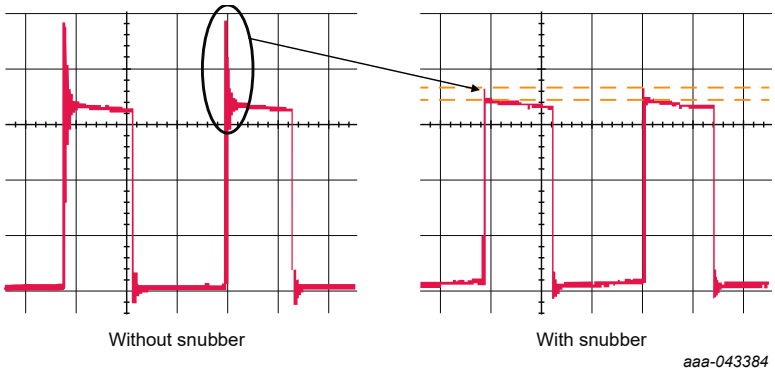


Figure 23. Snubber effect

- is the oscillation frequency where L_P and C_P are the parasitic inductor/capacitor mainly depending on the diode and the PCB layout.

$$Fring = \frac{1}{2\pi \times \sqrt{Lp \times Cp}}$$

- A good starting point to design the snubber is to take:
  - C_P = diode output capacitance from diode data sheet
  - $C_{SNUB} = 5 \times C_P$
  - Calculate L_P from Fring measured by oscilloscope
  -

$$Rsnub = 1 / 2 \times \sqrt{(Lp) / (Cp)}$$

- Try the snubber calculated values or try the values provided for V_{PRE} and V_{CORE} in this application note and adjust them experimentally to compensate the PCB layout parasitic.

6.2.9 V_{PRE} RC snubber

- RC snubber in parallel to the freewheeling diode D_V_{PRE} is recommended to dampen the voltage ringing at the SW_PRE pin and reduce high frequency emissions.
- C_{SNUB_VPRE} and R_{SNUB_VPRE} values must be tuned according to board and layout performance to take into account parasitic inductance/capacitance.
- The current pike in R_{SNUB_VPRE} at each V_{PRE} cycle is important. R_{SNUB_VPRE} resistor must be at least a 1/4 W resistor type for V_{SUPMAX} = 18 V. $P(R_{SNUB\_VPRE}) = 1/2 * C_{SNUB\_VPRE} * (V_P^2 + V_N^2) * F_{SW}$ where V_P and V_N are the voltage levels (positive and negative) measured at the resistor R_{SNUB_VPRE} (see Figure 20).
- From Figure 20, $P(R_{SNUB\_VPRE}) = 1/2 * 4.7\ nF * (14.7^2 + 3.6^2) * 440\ kHz = 0.237\ W$.

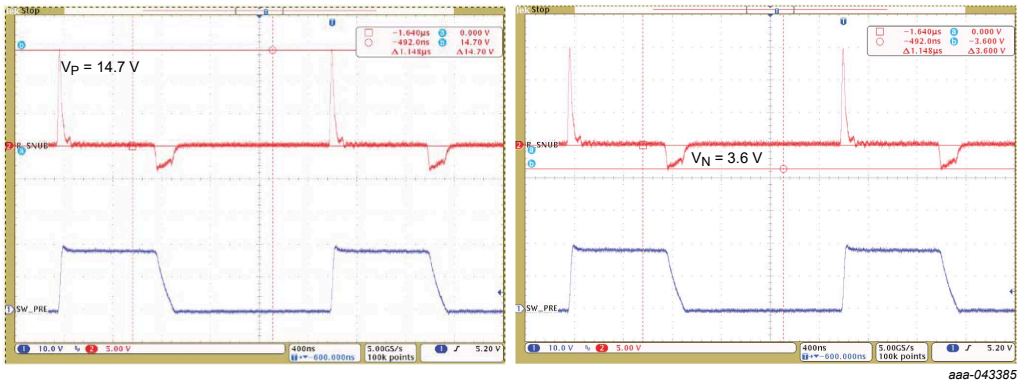


Figure 24. V_{PRE} R_{SNUB} V_P and V_N measurement at V_{SUP} = 18 V

6.2.10 Continuous mode

- V_{PRE} must work in continuous mode (current in the inductor always > 0) to provide a good load transient response and good EMC performance. V_{PRE} is continuous when I_{PRE} > 180 mA (for a 22 µH inductor).
- $I_{PRE} = I_{CCA} + I_{AUX} + I_{CAN} + (I_{CORE} * V_{CORE} / V_{PRE} / V_{CORE\_EFF})$ where V_{CORE_EFF} is V_{CORE} efficiency (~85 % at 3.3 V and ~70 % at 1.2 V)

6.2.11 Component list proposal

Table 10. V_{PRE} supply component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{SNUB_VPRE}	2.2 nF	Snubber component values to be adjusted at PCB level	
R_{SNUB_VPRE}	8.0 Ω		PGND
C_{BOOT_PRE}	100 nF	CGA2B3X7R1H104K050BB/TDK	
D_V_{PRE}		- PMEG4020EP/NXP (I_F = 2.0 A, V_R = 40 V) - PMEG4030EP/NXP (I_F = 3.0 A, V_R = 40 V) - SS24T3G/On Semiconductor (I_F = 2.0 A, V_R = 40 V) - MBRS340T3/ON Semiconductor (I_F = 3.0 A, V_R = 40 V)	PGND

Table 10. V_{PRE} supply component list...*continued*

Component	Value	Reference/manufacturer proposal	Ground connection
L_V_{PRE}	22 µH	- B82464G4223M/TDK-EPCOS (I_R = 2.25 A, I_{SAT} = 2.5 A) - MSS1278-223MLB/COILCRAFT (I_R = 4.0 A, I_{SAT} = 6.0 A)	
LS_BB		- BUK9M24-60E/NXP - BUK9832-55A/NXP	PGND
D_BB		- PMEG4020EP/NXP (I_F = 2.0 A, V_R = 40 V) - PMEG4030EP/NXP (I_F = 3.0 A, V_R = 40 V) - SS24T3G/On Semiconductor (I_F = 2.0 A, V_R = 40 V) - MBRS340T3/ON Semiconductor (I_F = 3.0 A, V_R = 40 V)	
C_{OUT_VPRE}	10 µF 22 µF	Ceramic capacitor ESR < 100 mΩ - 4x CGA6M3X7R1C106K/TDK - 2x GCM32ER71C226ME19/MURATA	PGND

6.3 FS6500 V_{CORE} supply regulator

The FS6500 V_{CORE} buck converter regulator is configurable with a 1.0 V to 5.0 V range and adjustable around these voltages with an external resistor bridge (R3 and R4). An external compensation network made of R1, C1, R2, and C2, is connected between VCORE_SNS, FB_CORE, and COMP_CORE, to ensure a good stability of the closed loop. The FS6500 V_{CORE} supply connections are shown in Figure 21.

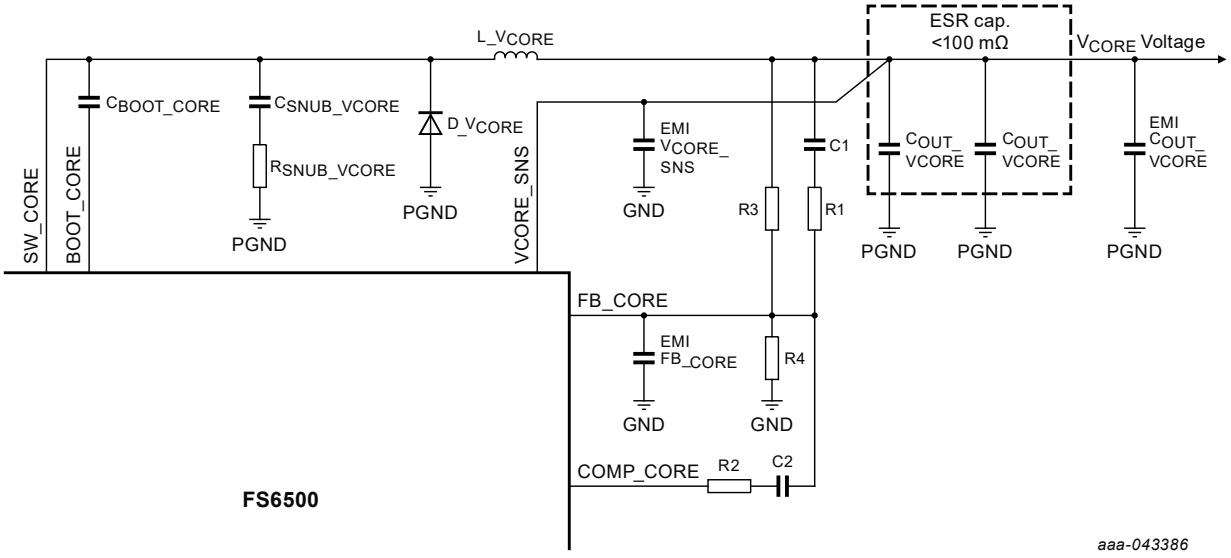


Figure 25. FS6500 V_{CORE} connections

6.3.1 V_{CORE} main characteristics

- V_{PREMAX} = 7.0 V
- $V_{PRE\_MAXRATING}$ = 8.0 V
- V_{CORE} = 1.0 V to 5.0 V
- $I_{COREMAX}$ = 2.2 A for FS652x, 1.5 A for FS651x, 0.8 A for FS650x
- F_{SWCORE} = 2.4 MHz

6.3.2 L_V_{CORE} calculation

- Max I_{CORE} recommendation: 0.8 A max for V_{CORE} = 5.0 V, 1.5 A max for V_{CORE} = 3.3 V, 2.2 A max for V_{CORE} = 1.2 V
- Inductor current ripple: I_{RIP} = K x I_{CORE} with K = 2 x ($I_{CORE\_LIM\_MIN}$ - I_{CORE_MAX}) / I_{CORE_MAX}
- Buck configuration:

$$LVcore = \frac{(Vcore \times (Vpremax - Vcore))}{K \times Vpremax \times Icore \times Fswcore}$$

- Min. L_V_{CORE} calculation for different use cases:

V_{CORE}	I_{CORE_MAX}	L_V_{CORE} calculated	L_V_{CORE} normalized
5.0 V	0.8 A	1.55 µH	2.2 µH
3.3 V	0.8 A	1.90 µH	
	1.5 A	1.25 µH	
1.2 V	0.8 A	1.1 µH	1.5 µH
	1.5 A	0.75 µH	
	2.2 A	0.75 µH	

6.3.3 L_V_{CORE} selection

- Must be shielded inductor
- Inductor value: 2.2 µH or 1.5 µH depending on V_{CORE} setting
- 2.2 µH inductor value was used to validate all V_{CORE} settings at NXP
- Rated current: $I_R > I_{COREMAX}$
- Saturation current: $I_{SAT} > I_R + (I_{RIP}/2)$
- Serial resistance: DCR < 50 mΩ

6.3.4 D_V_{CORE} selection

- Schottky diode is recommended
  - lower forward voltage drop (V_F) reduces power dissipation
  - lower parasitic capacitor improves EMC performance
- Reverse voltage: $V_R \geq V_{PRE\_MAXRATING} \geq 8.0$ V
- Average rectified forward current: $I_F > I_{COREMAX} + (I_{RIP}/2)$
- Power dissipation: $P_D = V_F \times I_F$

6.3.5 Output capacitors

- From 20 µF to 40 µF ceramic capacitor(s) with low ESR << 100 mΩ is recommended for the FS6500 series
- Capacitor value can be optimized with CNC tool (see Section 15 "References")
- The ESR of the output capacitor is one of the main contributors to the output voltage ripple. The ripple generated by the ESR is proportional to its value (ESR * I_{RIP}). A high ripple can disturb the regulation loop.
- Low ESR capacitor reduces the ripple, avoids instability, and lowers EMI

6.3.6 V_{CORE} RC snubber

- An RC snubber in parallel to the freewheeling diode D_V_{CORE} is recommended to dampen the voltage ringing at SW_CORE pin and reduce high frequency emissions
- C_{SNUB_VCORE} and R_{SNUB_VCORE} values must be tuned according to board and layout performance to take parasitic inductance/capacitance into account
- The current pike in R_{SNUB_VCORE} at each V_{CORE} cycle is important. The R_{SNUB_VCORE} resistor type must be at least 1/4 W. $P(R_{SNUB\_VCORE}) = 1/2 * C_{SNUB\_VCORE} * (V_P^2 + V_N^2) * F_{SW}$ where V_P and V_N are the voltage levels (positive and negative) measured at the resistor R_{SNUB_VCORE} (see Figure 26)
- From Figure 26, $P(R_{SNUB\_VCORE}) = 1/2 * 4.7\ nF * (5.4^2 + 3.12^2) * 2.4\ MHz = 0.219\ W$

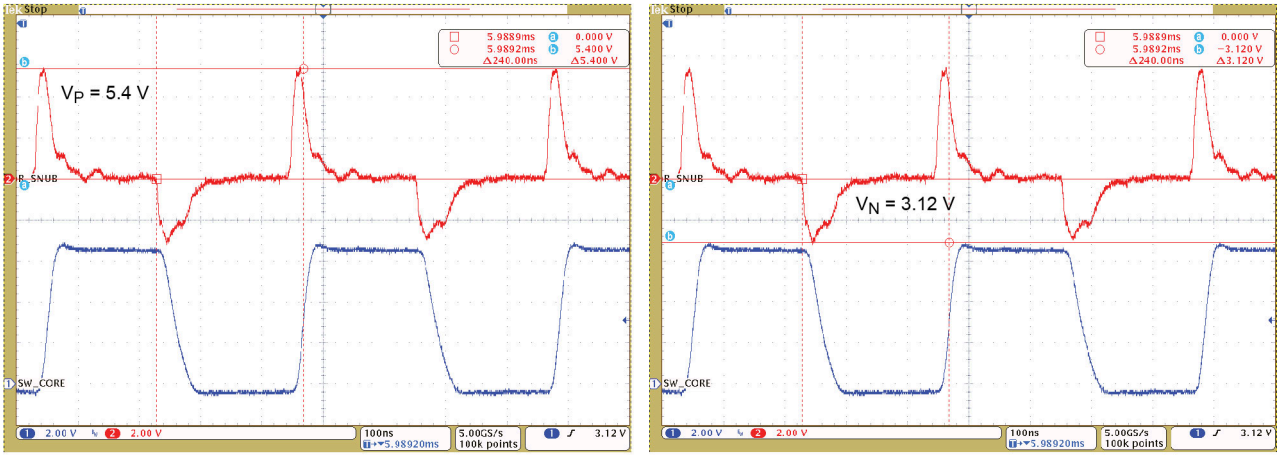


Figure 26. V_{CORE} R_{SNUB} V_P and V_N measurement

6.3.7 Continuous mode

- V_{CORE} must work in continuous mode (current in the inductor always > 0) to provide a good load transient response and good EMC performances. For a 2.2 µH inductor:
  - For V_{CORE} = 5.0 V configuration, V_{CORE} is in continuous when I_{CORE} > 110 mA
  - For V_{CORE} = 3.3 V configuration, V_{CORE} is in continuous when I_{CORE} > 160 mA
  - For V_{CORE} = 1.2 V configuration, V_{CORE} is in continuous when I_{CORE} > 120 mA

6.3.8 Compensation network

V_{CORE} is a voltage mode buck converter with two poles and needs a compensation network, which creates a large phase boost. Such amplifier circuit is called *type 3 amplifier compensation*. It gives a very good transient response to the circuit. The compensation network connection is shown in Figure 27, and the 'AN4661: Designing the V_{CORE} compensation network' covers this subject in detail. In addition, a simulation tool is available to optimize IC performance for specific use cases.

The compensation network R1, C1, R2, and C2, is external to be flexible. It can be tuned to attach the FS6500 to different MCUs. Only C3, which is a very small capacitor value, is internal. A simulation tool (CNC), based on Matlab model, can be provided on demand to support optimized compensation network design. Typical component values are provided in the data sheet and in the Figure 4 application schematic.

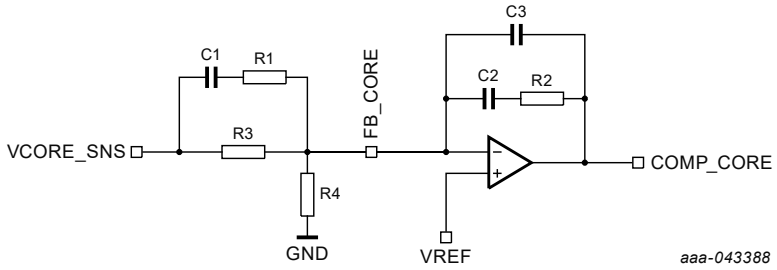


Figure 27. V_{CORE} compensation network

6.3.9 Component list proposal

Table 11. V_{CORE} supply component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{SNUB_VCORE}	2.2 nF	Snubber component values to be adjusted at PCB level	
R_{SNUB_VCORE}	8.0 Ω		PGND
C_{BOOT_CORE}	100 nF	CGA2B3X7R1H104K050BB/TDK	
D_V_{CORE}		- PMEG3020EH/NXP (I_F = 2.0 A, V_R = 30 V) - PMEG3030BEP/NXP (I_F = 3.0 A, V_R = 30 V) - SS22T3G/ON Semiconductor (I_F = 2.0 A, V_R = 20 V)	PGND
L_V_{CORE}	2.2 µH	B82472G6222M000/TDK-EPCOS (I_R = 3.0 A, I_{SAT} = 2.8 A)	
	1.5 µH	B82472G6152M000/TDK-EPCOS (I_R = 3.4 A, I_{SAT} = 3.0 A)	
R4	8.06 kΩ ±1 %		GND
R3	43 kΩ ±1 %	V_{CORE} = 5.0 V, C_{OUT} = 20 µF I_{CORE} = 10 mA to 0.8 A, dI_{CORE}/dt ≤ 2.0 A/µs	
R1, C1	2.4 kΩ, 330 pF		
R2, C2	62 kΩ, 82 pF		
R3	24.9 kΩ ±1 %	V_{CORE} = 3.3 V, C_{OUT} = 40 µF I_{CORE} = 10 mA to 1.5 A, dI_{CORE}/dt ≤ 2.0 A/µs	
R1, C1	510 Ω, 680 pF		
R2, C2	18 kΩ, 150 pF		
R3	4.32 kΩ ±1 %	V_{CORE} = 1.23 V, C_{OUT} = 40 µF I_{CORE} = 10 mA to 2.2 A, dI_{CORE}/dt ≤ 2.0 A/µs	
R1, C1	200 Ω, 220 pF		
R2, C2	39 kΩ, 1.0 nF		
C_{OUT_VCORE}	10 µF 22 µF	Ceramic capacitor ESR < 100 mΩ - 2x to 4x CGA6M3X7R1C106K/TDK - 1x to 2x GCM32ER71C226ME19/MURATA	PGND
EMI C_{OUT_VCORE}	100 nF	EMI capacitor values to be adjusted at PCB level	PGND
EMI V_{CORE_SNS}	330 pF		GND
EMI FB_C_{ORE}	22 pF		GND

6.4 FS4500 V_{CORE} supply regulator

The FS4500 V_{CORE} linear regulator is configurable with a 1.0 V to 5.0 V range and adjustable around these voltages with an external resistor bridge (R3 and R4). BOOT_CORE and COMP_CORE pins used for FS6500 V_{CORE} buck converter regulator must be left open for FS4500 V_{CORE} linear regulator. The FS4500 V_{CORE} supply connections are shown in Figure 28.

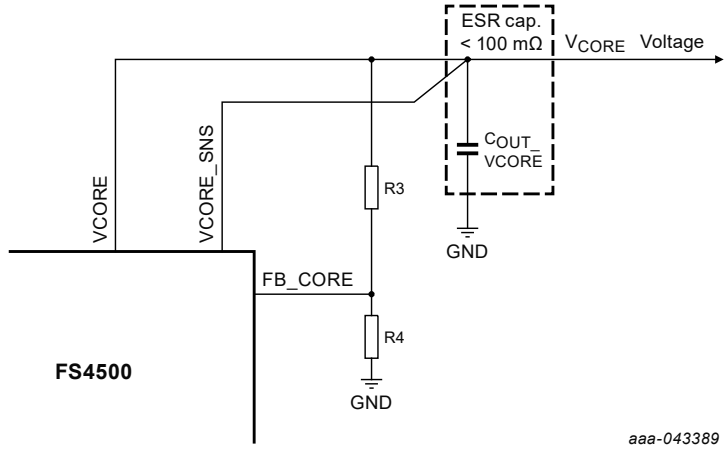


Figure 28. FS4500 V_{CORE} connections

Table 12. Linear regulator component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{OUT_VCORE}	10 µF 22 µF	Ceramic capacitor ESR < 100 mΩ - 2x CGA6M3X7R1C106K/TDK - 1x GCM32ER71C226ME19/MURATA	GND

6.5 FS6500 and FS4500 linear regulators, V_{CCA} and V_{AUX}

The V_{CCA} and V_{AUX} regulators can deliver 3.3 V or 5.0 V independently, according to the resistor value connected on the SELECT pin. The detection of this resistor value is done during the start-up sequence and the regulators output voltage automatically settles to their selected voltage value.

When V_{CCA} and V_{AUX} regulators are configured to 3.3 V, a minimum delta of 50 mV between ($V_{CCA\_OV\_33}$ min – V_{CCA} max), ($V_{AUX\_OV\_33}$ min – V_{AUX} max), (V_{CCA} min – $V_{CCA\_UV\_33}$ max), (V_{AUX} min – $V_{AUX\_UV\_33}$ max) is guaranteed on all production parts by the Automatic Test Equipment program.

6.5.1 V_{CCA} with external PNP and V_{AUX} used

An external PNP can be connected to VCCA to increase its current capability from 100 mA (configuration with internal PMOS) to 300 mA (configuration with external PNP). The VCCA with external PNP and VAUX connections are shown in Figure 29.

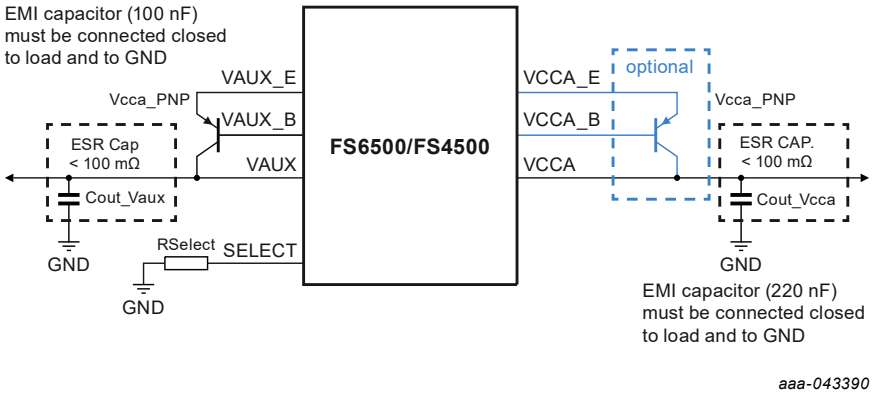


Figure 29. Linear regulator connection

6.5.2 PNP selection

- V_{CCA} PNP
  - Collector-emitter voltage: VCE ≥ $V_{PRE\_MAXRATING}$ ≥ 8.0 V
  - Collector-base voltage: VCB ≥ $V_{PRE\_MAXRATING}$ ≥ 8.0 V
  - Collector current: IC ≥ I_{CCA_LIM} ≥ 675 mA
  - Current gain: 150 < HFE < 450
  - Power dissipation: Pd = (V_{PRE} – V_{CCA}) * I_{CCA} = 1.0 W for V_{CCA} = 3.3 V/300 mA
- V_{AUX} PNP
  - Collector-emitter voltage: VCE ≥ V_{SUPMAX} ≥ 40 V
  - Collector-base voltage: VCB ≥ V_{SUPMAX} ≥ 40 V
  - Collector current: IC ≥ I_{AUX_LIM} ≥ 800 mA
  - Current gain: 100< HFE < 450
  - Power dissipation: P_D = (V_{PRE} – V_{AUX}) * I_{AUX} = 1.0 W for V_{AUX} = 3.3 V/300 mA

6.5.3 Reduce Vaux_PNP power dissipation

When V_{AUX} is used at 3.3 V and high current, the power dissipation in the external PNP can be reduced by adding a resistance in serial with the PNP collector, as shown in Figure 30. R_{AUX} reduces the drop in V_{AUX_PNP} and its power dissipation.

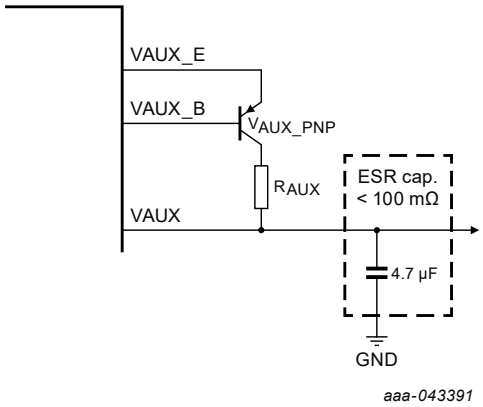


Figure 30. Reduce V_{AUX_PNP} power dissipation

V_{AUX_PNP} voltage drop must be > 1.5 V so R_{AUX} voltage drop must be less than V_{PRE} – V_{AUX} – 1.5 V < 1.7 V. R_{AUX} must be < 4.0 Ω.

R_{AUX} value depends on I_{AUX} and P_{DIS_RAUX} to be balanced with $P_{DIS\_VAUX\_PNP}$.

- Without R_{AUX}:
  - $P_{DIS\_VAUX\_PNP} = (V_{PRE} – V_{AUX}) \times I_{AUX} = (6.5\ V – 3.3\ V) \times 0.4\ A = 1.3\ W$
- With $R_{AUX} = 3.0\ \Omega$:
  - $P_{DIS\_MAx} = (V_{PRE} – V_{AUX} – (R_{AUX} \times I_{AUX})) \times I_{AUX} = (6.5\ V – 3.3\ V – (3 \times 0.4)) \times 0.4\ A = 0.8\ W$
  - $P_{DIS\_RAUX} = R_{AUX} \times I_{AUX}^2 = 0.5\ W$

6.5.4 Component list proposal

Table 13. Linear regulator component list

Component	Value	Reference/manufacturer proposal	Ground connection
V_{AUX_PNP}		- PHPT60603PY/NXP - PBSS5350Z/NXP - NJT4030P/ON Semiconductor	
C_{OUT_VAUX}	4.7 µF ±10 %	Ceramic capacitor ESR < 100 mΩ GCM31CC71H475KA03L/Murata	GND
V_{CCA_PNP}		- PHPT60603PY/NXP - PBSS5350Z/NXP - NJT4030P/ON Semiconductor	
C_{OUT_VCCA}	4.7 µF ±10 %	Ceramic capacitor ESR < 100 mΩ GCM31CC71H475KA03L/Murata	GND
Component	**Value**	**V_{AUX}/V_{CCA} voltage configuration**	
R_{SELECT}	5.1 kΩ ±5.0 %	$V_{CCA} = 3.3\ V$, $V_{AUX} = 3.3\ V$	GND
R_{SELECT}	12 kΩ ±5.0 %	$V_{CCA} = 5.0\ V$, $V_{AUX} = 5.0\ V$	GND
R_{SELECT}	24 kΩ ±5.0 %	$V_{CCA} = 3.3\ V$, $V_{AUX} = 5.0\ V$	GND
R_{SELECT}	51 kΩ ±5.0 %	$V_{CCA} = 5\ V$, $V_{AUX} = 3.3\ V$	GND

6.5.5 V_{CCA} without external PNP and V_{AUX} not used

If V_{AUX} is not used in the application, the VAUX_B, VAUX_E and VAUX pins must be left open. If V_{CCA} is used without the external PNP, the VCCA_E pin must be connected to the VPRE pin. VCCA_B pin must be left open. The V_{CCA} without external PNP and V_{AUX} not used connections are shown in Figure 31.

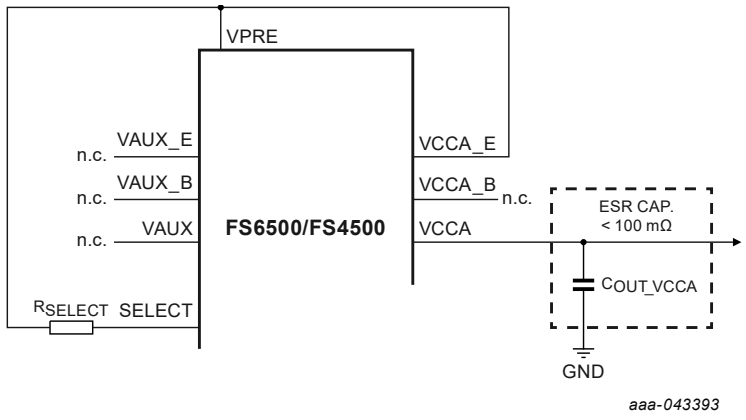


Figure 31. DFS disabled, VAUX not used and VCCA w/o PNP

Table 14. R_{SELECT} component list

Component	Value	V_{CCA} voltage configuration	Ground connection
R_{SELECT}	5.1 kΩ or 24.9 kΩ ±5.0 %	V_{CCA} = 3.3 V	GND
R_{SELECT}	12.1 kΩ or 51.1 kΩ ±5.0 %	V_{CCA} = 5.0 V	GND

6.6 CAN_5V

CAN_5V is a regulator dedicated to the internal physical layer. An external capacitor is needed for filtering purposes, as shown in Figure 32

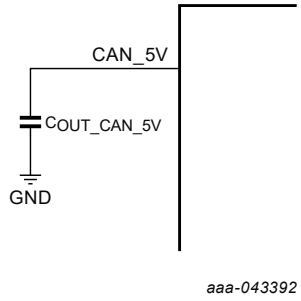


Figure 32. CAN_5V connection

Table 15. CAN_5V component list

Component	Value	Reference/manufacturer proposal	Ground connection
C_{OUT_VCAN}	1.0 µF	CGA4J2X7R1C105K / TDK	GND

6.7 Reset and fail-safe outputs - RSTB, FS0B, and FS1B

The RTSB pin must be connected to the MCU reset pin. Depending on INIT configuration, the FS6500 and FS4500 asserts RSTB low if a fault is reported. C_{OUT_RSTB} must be placed close to the device pin.

The FS0B pin is the first safety output pin. Depending on INIT configuration, the FS6500 and FS4500 asserts FS0B low if a fault is reported, disconnecting the critical functions in the application. The FS1B pin is the second safety output pin. The FS6500 and FS4500 asserts FS1B low when FS0B is asserted with a configurable delay, for a configurable duration.

FS0B and FS1B are global pins and can be connected outside the ECU. They are load dump proof and robust against ISO 7637-2:2011 pulses with a serial resistor to limit the current during the high transient pulse on the line. They are robust against ESD GUN test up to ±8.0 kV with a filtering capacitor. C_{OUT1_FSXB} must be placed close to the device pin and C_{OUT2_FSXB} must be placed close to the module connector. RSTB, FS0B, and FS1B connections are shown in Figure 33.

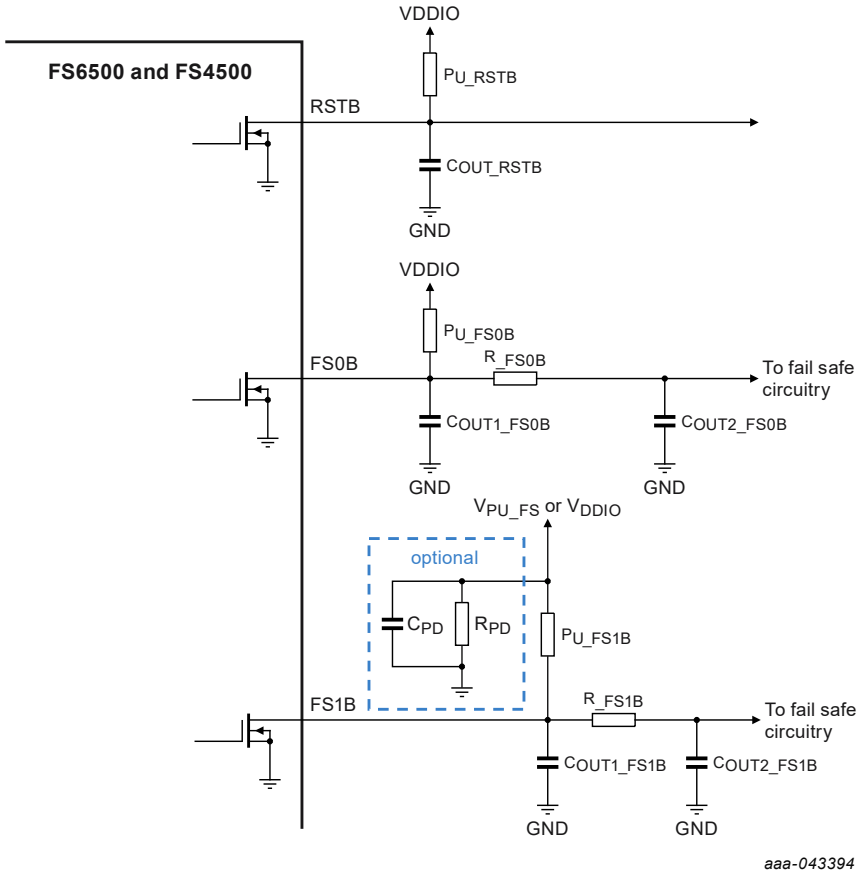


Figure 33. Reset and fail-safe output connections

In LPOFF mode, RSTB, FS0B and FS1B are asserted low. For safety applications, it is recommended to connect the FS1B pull up to VPU_FS. When the backup delay is implemented, which is recommended for ASIL D applications, the external R_{PD}/C_{PD} components are required with a mandatory connection to VPU_FS. Refer to the data sheet and the safety manual for more information on the configuration and reaction of these outputs.

Table 16. Reset and fail-safe outputs component list

Component	Value	Ground connection
C_{OUT_RSTB}	1.0 nF	GND
P_{U_RSTB}	5.1 kΩ	
C_{OUTx_FSxB}	10 nF to 22 nF	GND
P_{U_FS0B}	5.1 kΩ	
P_{U_FS1B}	10 kΩ	
R_{FS0B} and R_{FS1B}	5.1 kΩ	

The FS1B pin can be pulled up to VDDIO or VPU_FS as depicted in Figure 33. It is highly recommended to use VPU_FS as a pull-up of FS1B pin. First, to ensure the FS1B delay is guaranteed in all system failure cases, FS1B must pull up to VPU_FS. Second, using VPU_FS as a pull-up of FS1B pin avoids common cause failure when FS0B is pulled up to VDDIO.

VPU_FS internal switch(S1) to VPRE must be closed when power up or wake-up during INIT_FS mode, regardless of whether FS1B is pulled up to VPU_FS or VDDIO. If FS1B is pull-up to VPU_FS, a resistor and a

capacitor are placed in parallel between VPU_FS and Ground as backup delay. If FS1B is pull-up to VDDIO, VPU_FS can be open.

6.8 FS6500 and FS4500 debug pin

The connections shown in Figure 34 can be used to enter into debug mode on the FS6500 and FS4500. Debug mode allows the user to debug software with the MCU. The deep fail-safe and the WD timeout are disabled. The CAN and the LIN physical layers are in normal mode by default. The DEBUG pin is scanned by the main and the fail-safe state machines after power on reset and after wake-up from LPOFF during the SELECT pin configuration state.

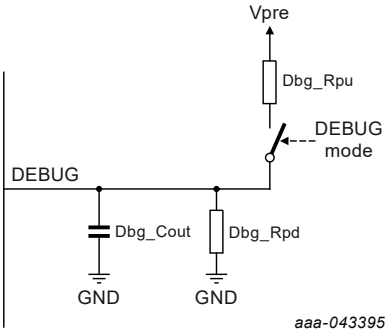


Figure 34. Debug mode entry connection

Table 17. Debug mode component list

Component	Value	Ground connection
D_{BG_COUT}	10 nF to 22 nF	GND
D_{BG_RPD}	11 kΩ	GND
D_{BG_RPU}	10 kΩ	

7 FS6500 and FS4500 vs. MC33907/8 pinout compatibility

FS6500 and FS4500 pinout is backward compatible with the MC33907/8 at the ISO function, facilitating the hardware migration from the MC33907/8 to the FS6500 and FS4500. The FS6500 and FS4500 long duration timer (LDT) does not require any external pins. Table 18 summarizes the pinout differences.

Table 18. Pinout compatibility

Pin	MC33907/8		FS6500 and FS4500		
	Function	Max. rating	Function	Max. rating	Comment
5	LIN	–0.3 V to 40 V	LIN	–0.3 V to 40 V	LIN and FS1B functions are exclusive
	NC		FS1B	–0.3 V to 40 V	
11	IO_5	–0.3 V to 40 V	IO_5	–0.3 V to 20 V	IO_5 cannot be used as DIGITAL_OUT, but can be used as an analog input like IO_0
			VKAM	–0.3 V to 8.0 V	Output
13	IO_1	–0.3 V to 40 V	FCRBM	–0.3 V to 8.0 V	Fixed for redundant V_{CORE} voltage monitoring, former IO_1 FB_CORE monitoring
22	TXDL	–0.3 V to V_{DDIO} +0.3	TXDL	–0.3 V to 8.0 V	LIN and VPU_FS functions are exclusive
			VPU_FS	–0.3 V to 8.0 V	
33	COMP_CORE	–0.3 V to 2.5 V	COMP_CORE	–0.3 V to 2.5 V	Must be left open for FS4500
36	BOOT_CORE	0 V to 15 V	BOOT_CORE	0 V to 15 V	Must be left open for FS4500

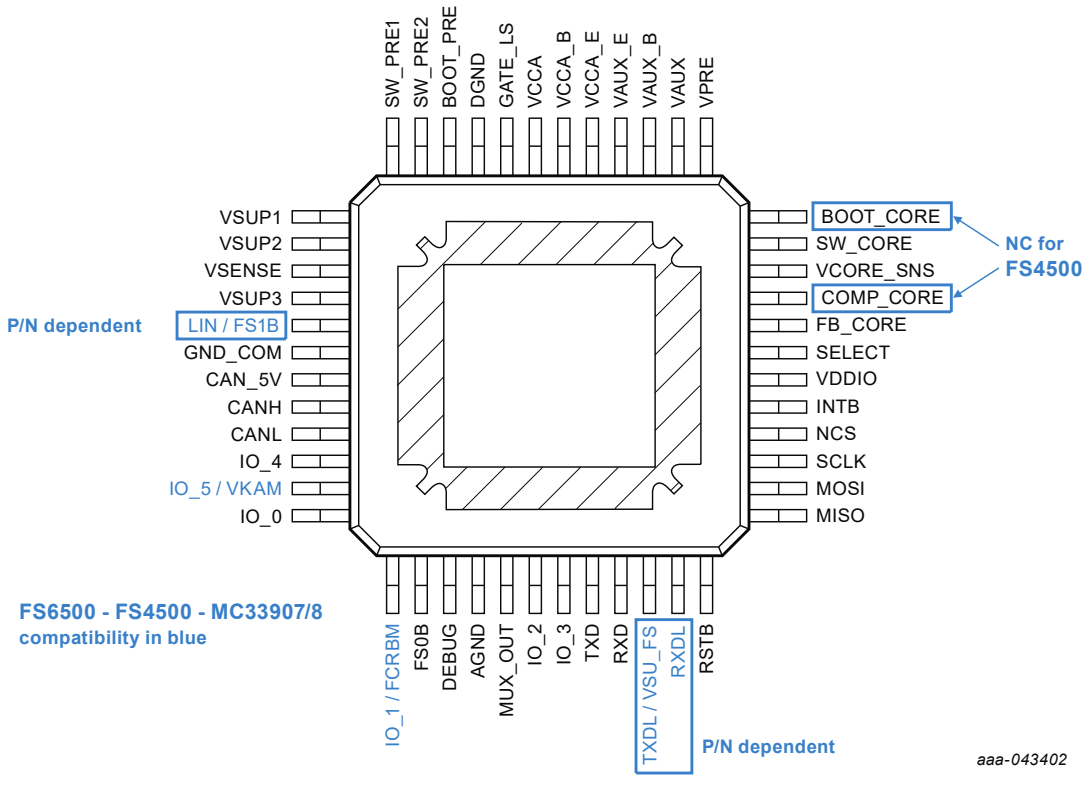


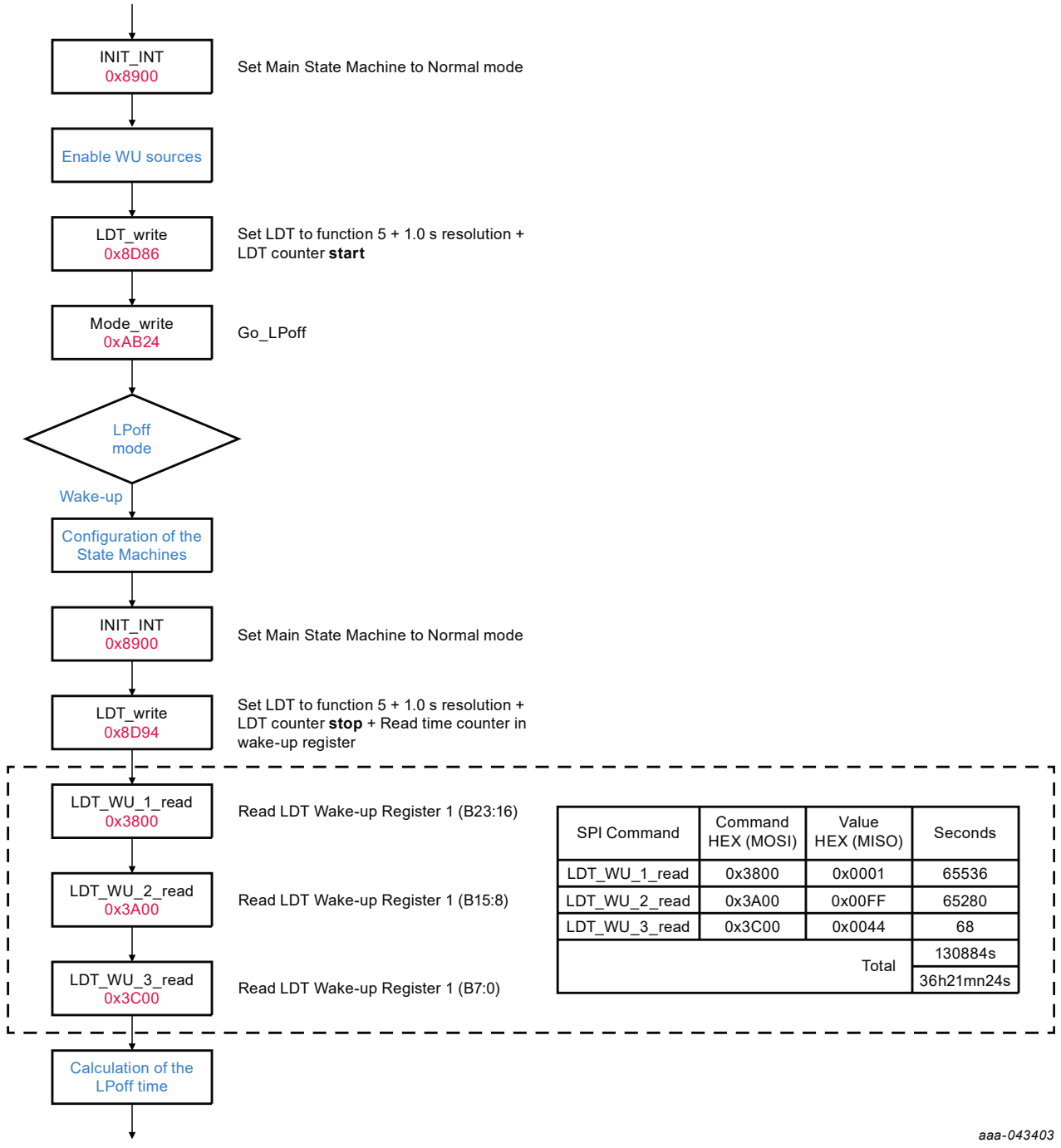
Figure 35. FS6500 and FS4500 pinout comparison with the MC33907/8

8 FS6500 and FS4500 long duration timer (LDT)

8.1 LDT function 5 principle

Depending on the part number, the FS6500 and FS4500 can provide a long duration timer to count timings in normal and/or LPOFF modes with a 1.0 s time base. Refer to the data sheet for more details on each LDT function. An example of how to handle the LDT function 5 is illustrated in Section 8.1 "LDT function 5 principle". To configure starting or stopping the LDT, the main state machine must be in normal mode.

Function 5: In LPOFF, count and do not wake-up unless the counter overflow occurs, or if the device wakes up by another source (I/Os, CAN, LIN). The time in LPOFF (usually ignition OFF time), can be read after stopping the LDT from the LDT_Wake_Up registers.



SPI Command	Command HEX (MOSI)	Value HEX (MISO)	Seconds
LDT_WU_1_read	0x3800	0x0001	65536
LDT_WU_2_read	0x3A00	0x00FF	65280
LDT_WU_3_read	0x3C00	0x0044	68
		Total	130884s
			36h21mn24s

Figure 36. LDT function 5 principle

8.2 LDT diagnostic

The objective is to verify the correct operation of the LDT and wake-up by LDT in case it is used as a safety function.

8.2.1 Principle

1. In normal mode, the LDT operation can be verified like the oscillator, the registers, the 16 and 24 bit counter(s) via INTB pulse, and internal register read back.
2. To test the wake-up function, enter into LPOFF mode and wake-up by LDT as the primary wake-up source. The IO_5 falling edge is used as a secondary wake-up source, in case the LDT wake-up does not work. An IO_5 high to low transition is created from IO_4 or V_{PRE} with a diode, and is testable via internal logic or the analog MUX.
3. Verify the correct LDT wake-up source before definitely sending the system into LPOFF with the guarantee to wake-up by LDT.

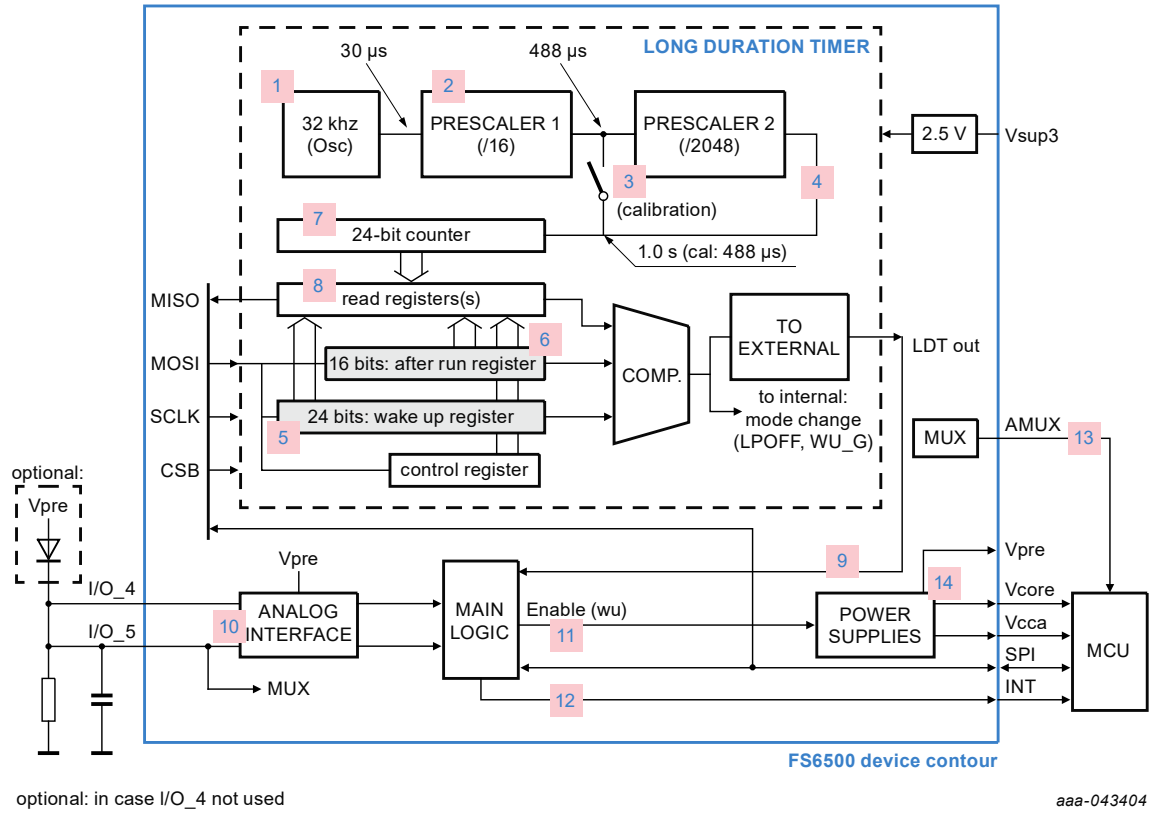


Figure 37. LDT diagnostic proposal

8.2.2 Detailed operation

- In normal mode:
  - Activate LDT. Select function F1 (INTB pulse)
  - Select calibration mode, it allows verification of (1), (2), (3), (7), (6), (9), and (12). Counter (7) counts with 488 µs time base, many bits of register (6) can be verified
  - Select non-calibration mode, it allows verification of (1), (2), (4), (7), (6), (9), and (12). Counter (7) counts with 1.0 s time base, few bits of register (6) can be verified
  - Set IO_4 high, verify the level on I0_5 via IO_5 bit from the IO_INPUT register and/or analog MUX. It allows the verification of (10) via usage of (13)
  - Configure LDT wake-up in calibration mode, with function 4, wake-up time 100 ms (example)

  - External R/C is calculated to ensure the falling edge at IO_5 after 100 ms (ex 200 ms), to allow secondary wake-up, in case LDT wake-up fails
- Enter into LPOFF mode, via function 4:
  - (11) is the connection from main logic to enable the power supply after LDT or IO wake-up
  - (11) is not tested during a LPOFF to a normal mode transition. In case of a failure at (11), the device enters into LPOFF and does not wake-up
  - (14) denote power supplies, and is operational
- Enter into LPOFF mode, via function 3:
  - It allows verification of (11), transition from normal to LPOFF and LPOFF to normal

8.2.3 LDT clock accuracy

Long duration timer is based on an internal 32768 Hz oscillator with ±5.0 % accuracy out of the NXP production line from –40 °C to 125 °C (as specified in the data sheet). This accuracy depends on process variations, temperature range and aging drift.

Statistical analysis shows the ±5.0 % oscillator accuracy is split between ±3.0 % process variation and ±2.0 % temperature and aging variation from –20 °C to 85 °C. The process variation can be removed with a part-to-part calibration at the customer production line test at room temperature. After calibration, the long duration timer oscillator accuracy could achieve ±2.0 % from –20 °C to 85 °C temperature range and 15 years life cycle.

9 MCU mapping with FS6500 and FS4500

The FS6500 and FS4500 family is covering a wide range of NXP and non NXP MCU core voltage and current capability through multiple part numbers as defined in Table 1.

Section 9 "MCU mapping with FS6500 and FS4500" summarizes the possible MCU mapping with FS6500 and FS4500 family. This summary might not be exhaustive with latest MCU and non NXP MCU. Contact your NXP representative if you want to use the FS6500 and FS4500 with another MCU not listed in Section 9 "MCU mapping with FS6500 and FS4500" in order to verify the compatibility.

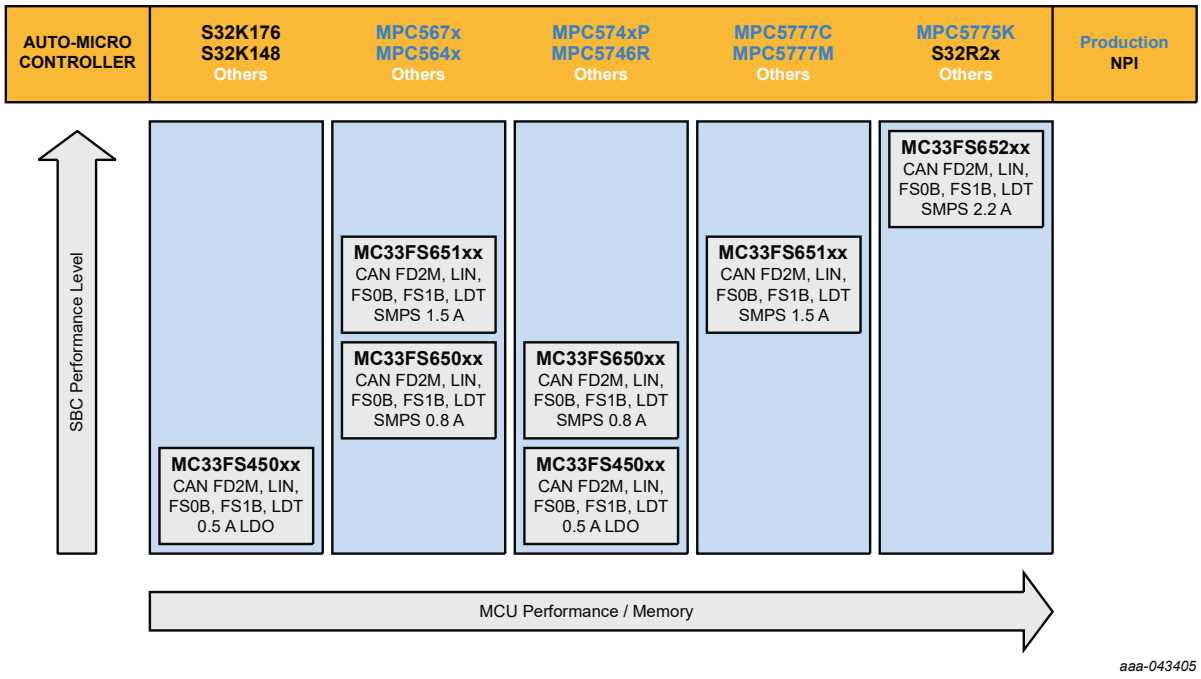


Figure 38. MCU mapping with FS6500 and FS4500

10 FS6500 and FS4500 extended use cases

10.1 V_{SENSE} accuracy

V_{SENSE} voltage, image of the battery voltage, can be monitored through the MUX_OUT pin with 5.0 % accuracy out of the NXP production line (as specified in the data sheet). As described in Figure 39, this accuracy depends on the V_{SENSE} resistor bridge and the MUX_OUT amplifier offset, both varying with temperature, voltage, and process.

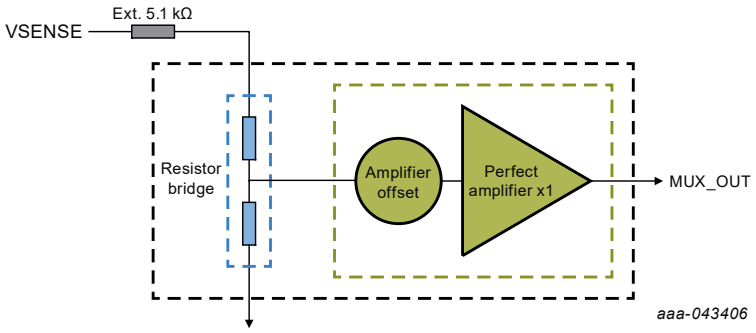


Figure 39. Simplified V_{SENSE} to MUX_OUT block diagram

Statistical analysis shows the main contributor to the accuracy is the process variation that can be removed with a part-to-part calibration at the customer production line test. The calibration can be done at room temperature, and static V_{SENSE} between 9.0 V and 19 V (ideally 12 V or 14 V). After calibration, the V_{SENSE} monitoring accuracy can achieve ±1%, for both V_{DDIO} = 3.3 V and 5.0 V, in wide range resistor bridge configuration (without taking into account the V_{SENSE} supply accuracy used for the calibration).

10.2 FS6500 attach to an Infineon Aurix MCU

The FS6500 can be attached to the Aurix MCU from Infineon. Figure 40 is a power tree proposal to show a possible connection between these two devices. This is not the only one, and can be adjusted, depending on the application need. Refer to the safety manual for safety connections and MCU error monitoring.

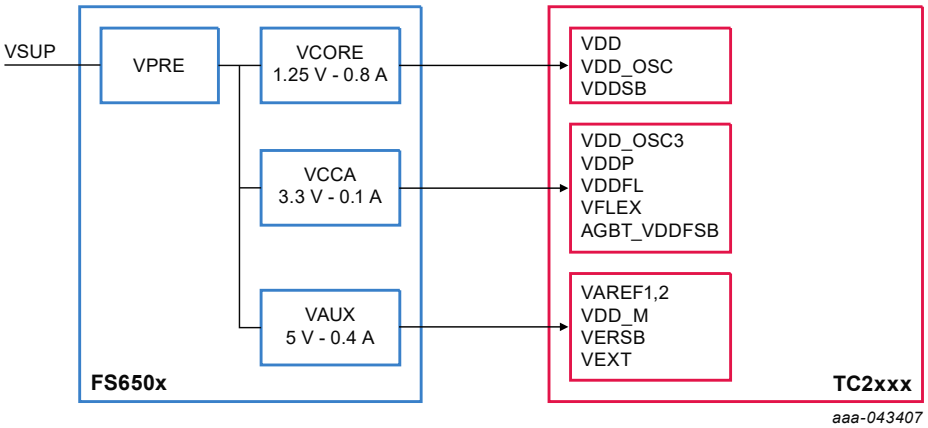


Figure 40. Power tree proposal

10.3 FS6500 and FS4500 For 24 V application

The FS6500 and FS4500 can fit for 24 V DC input voltage up to 36 V maximum operating voltage. The maximum rating voltage is 40 V and an additional input protection is required to sustain a 60 V load dump in 24 V transportation applications.

10.3.1 With a load dump protection

Figure 41 is a companionship proposal for the FS6500 and FS4500 to sustain 60 V load dump. The MAX6495 limits the input voltage at V_{OV} (set here at 37.7 V) to not exceed the 40 V maximum rating of the FS6500 and FS4500, and keeps the application running during the load dump condition.

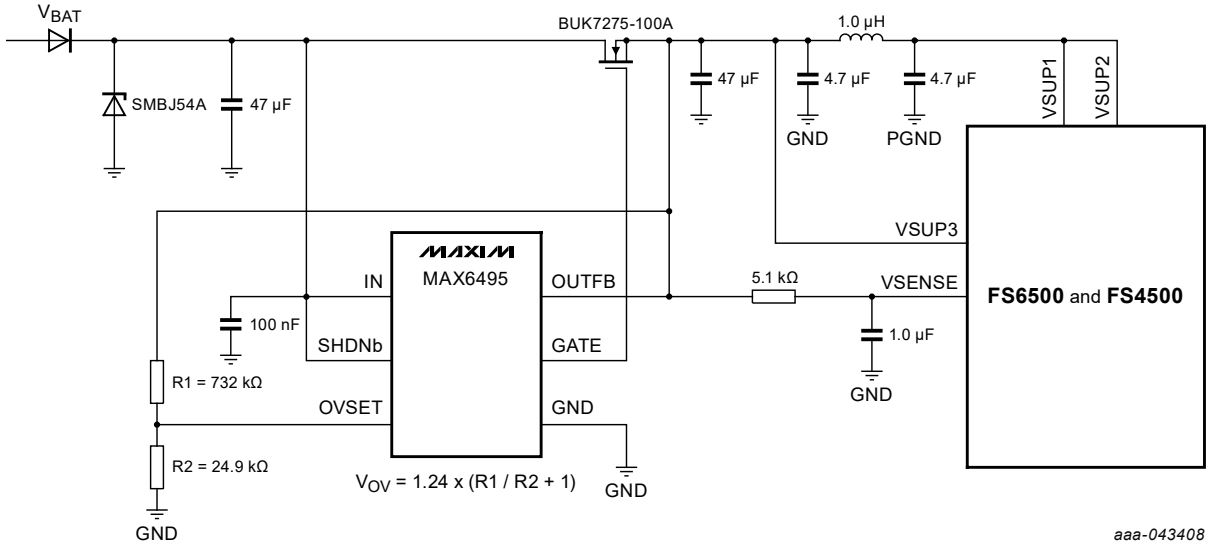


Figure 41. Battery connection proposal to sustain 60 V load dump

Table 19. MAX6495 external component list

Component	Reference/manufacturer proposal	Ground connection
ZD1	- SMBJ54A/Fairchild - PTVS54VP1UP/NXP	GND
M1	- BUK7275-100A/NXP - BUK7Y65-100E/NXP	

10.3.2 With a 60 V pre-regulator

Figure 42 is a companionship proposal for the FS6500 and FS4500 to sustain 60 V load dump. The LM5118 accepts a wide input voltage range from 3.0 V to 75 V and delivers a constant regulated output voltage > 8.0 V to the input supply pins of the FS6500 and FS4500. This configuration prevents exceeding the maximum rating of the FS6500 and FS4500, keeps the application running during the load dump condition, and provides a protected V_{SUP} supply usable for other application purpose.

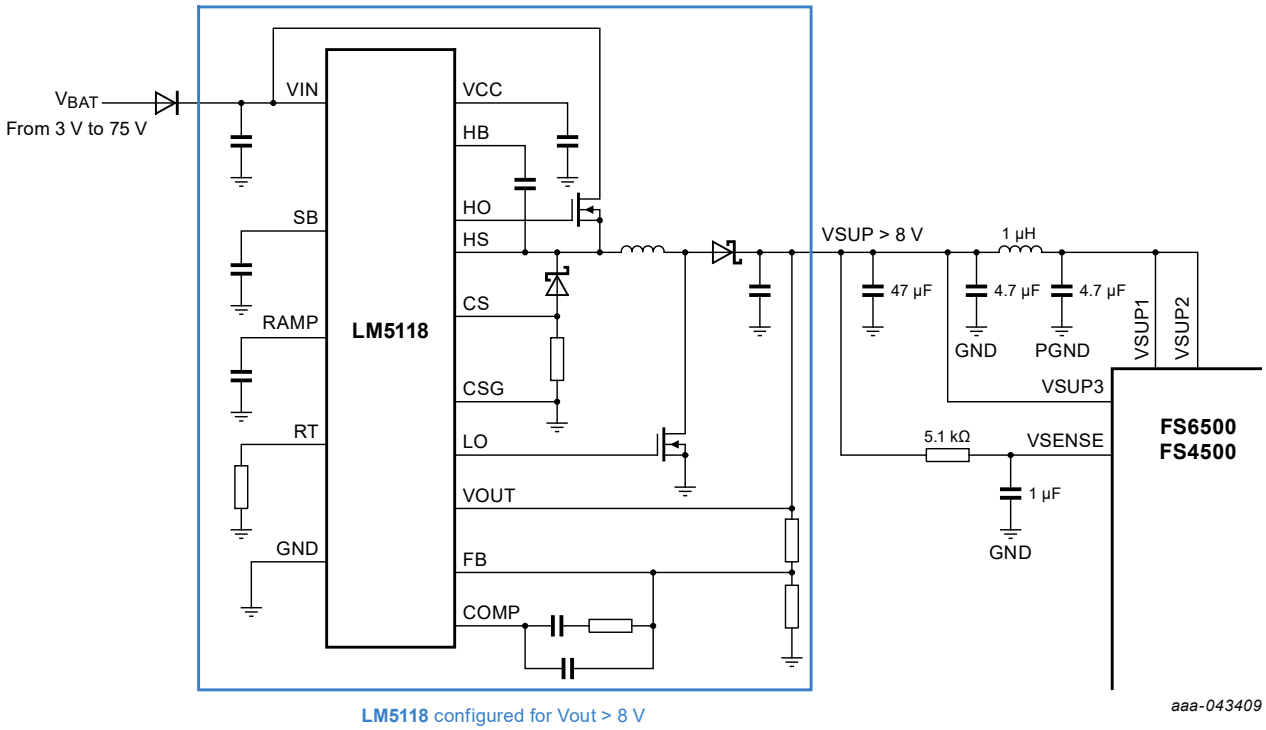


Figure 42. Battery connection proposal with a 60 V pre-regulator

Set the LM5118 output voltage:

- > $V_{SUP\_UV\_7}$ (> 8.0 V) in order to make sure that VPRE always works in buck mode only
- < V_{SUP_IPFF} (< 21 V) in order to make sure that VPRE frequency does not change to 220 kHz due to input feed forward condition

11 PCB layout recommendations

To minimize the effects of switching noise on the embedded DC/DC converters, special attention must be paid to the layout of the power components when designing a printed circuit board (PCB) using the FS6500 and FS4500. Component locations and ground connections on the PCB are important to consider when successfully optimizing overall performance with regards to high transient current loops, as shown in Figure 43.

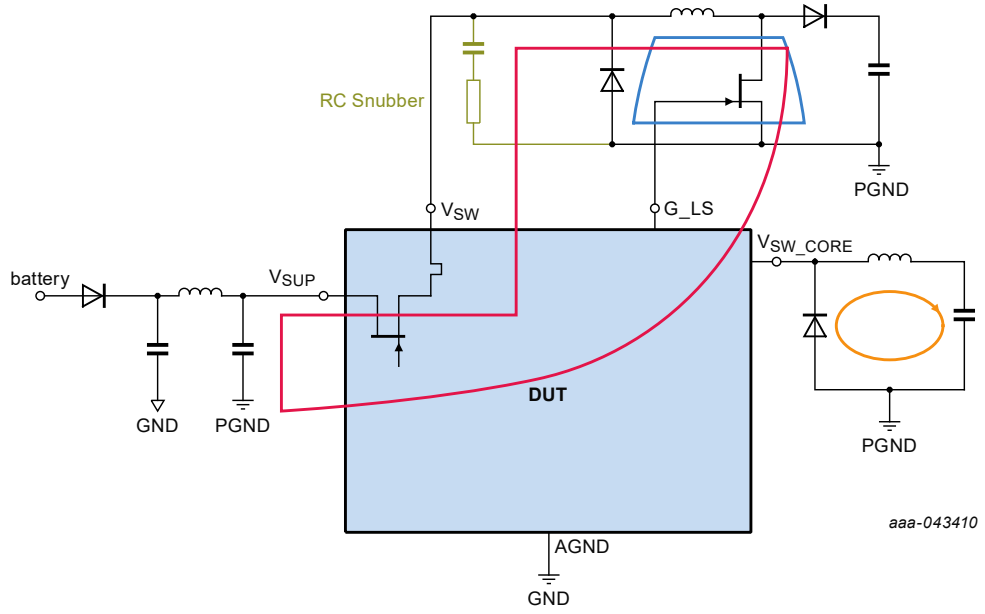


Figure 43. FS6500 current loops with a V_{CORE} buck converter

11.1 Ground connections

Three grounds are available on the FS6500 and FS4500:

- AGND (analog ground),
- GND_COM (physical layer ground), and
- DGND (logic ground).

On the PCB, two grounds must be clearly separated:

- Local PGND for power components involved in the high transient current loops
- GND for other components connected to ground

The star connection between PGND and GND must be done as far as possible from the local PGND ground on the PCB. The exposed pad is not electrically connected to ground, but this connection to the ground plane serves the power dissipation. The MCU digital ground should be connected to PGND to avoid any perturbation to GND. Each of the FS6500 and FS4500's external component connections to adequate ground are listed in Section 6 "FS6500 and FS4500 external components". Connections from FS6500 and FS4500 grounds and PCB grounds are shown in Figure 44.

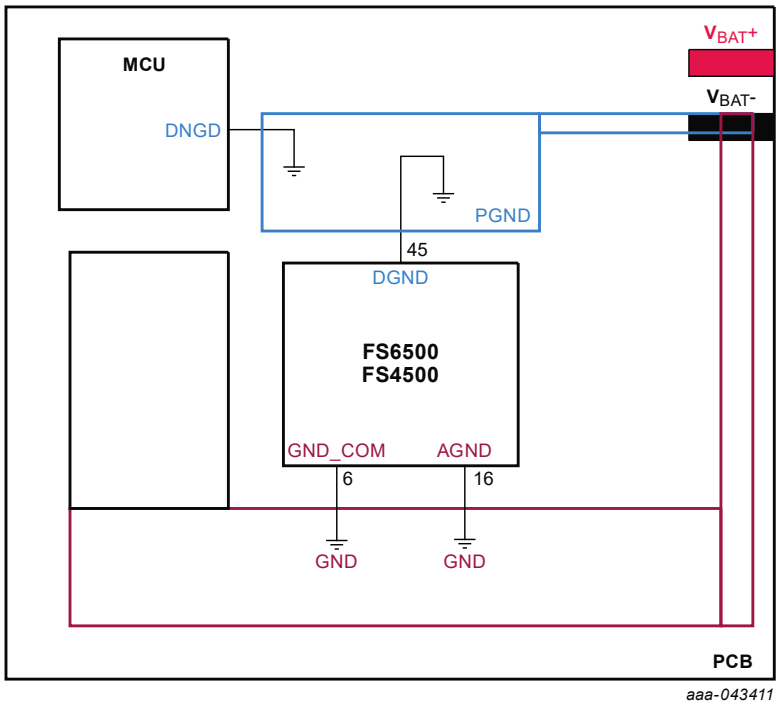


Figure 44. Ground connections between FS6500 or FS4500 and PCB ground

11.2 Routing external components

It is important to minimize the current loop on the PCB as much as possible. One way to do this is to place the power stage components involved in the high transient current loop as close as possible to the device. Avoid placing any power stage components close to other components that need to drive low-current levels. Such components could easily be perturbed by switching noise.

11.2.1 The V_{PRE} pre-regulator

Based on Figure 21, the PGND line of D_V_{PRE} is connected close to the PGND line near the $C_{OUT\_VPRE}(n)$ capacitors. $C_{OUT\_VPRE}(n)$ is kept close to the VPRE pin. The snubber (C_{SNUB_VPRE}, R_{SNUB_VPRE}) is kept close to D_V_{PRE}.

11.2.2 The V_{CORE} supply regulator

Based on Figure 25, the PGND line of D_V_{CORE} is connected close to the PGND line of the $C_{OUT\_VCORE}(n)$ capacitors. The snubber (C_{SNUB_VCORE}, R_{SNUB_VCORE}) is kept close to D_V_{CORE}. V_{CORE} output must be connected close to MCU core supply input to avoid DC voltage drop in the PCB track.

11.2.3 V_{AUX}, V_{CCA} linear regulators

Based on Figure 29, C_{OUT_VAUX} is kept close to the VAUX pin. C_{OUT_VCCA} is kept close to the VCCA pin.

11.2.4 VCAN

Based on Figure 32, keep $C_{OUT\_CAN\_5V}$ close to the CAN_5V pin.

11.2.5 R_{SELECT}

Based on Figure 29, R_{SELECT} must be placed close to the SELECT pin. Avoid placing power stage components close to the RSELECT pin to not disturb the current in the resistor during startup. This resistor is used for V_{CCA} and V_{AUX} voltage configuration.

11.2.6 Best practice

- If a high-current loop is going through multiple PCB layers, multiple vias are recommended to limit the parasitic (R and L) in the high-current path.
- Avoid a AGND plane/signal below SMPS power components
- Avoid low level signals below SMPS power components
- Connect components with high-impedance signals close to device pin to avoid noise injection

11.2.7 Placement example

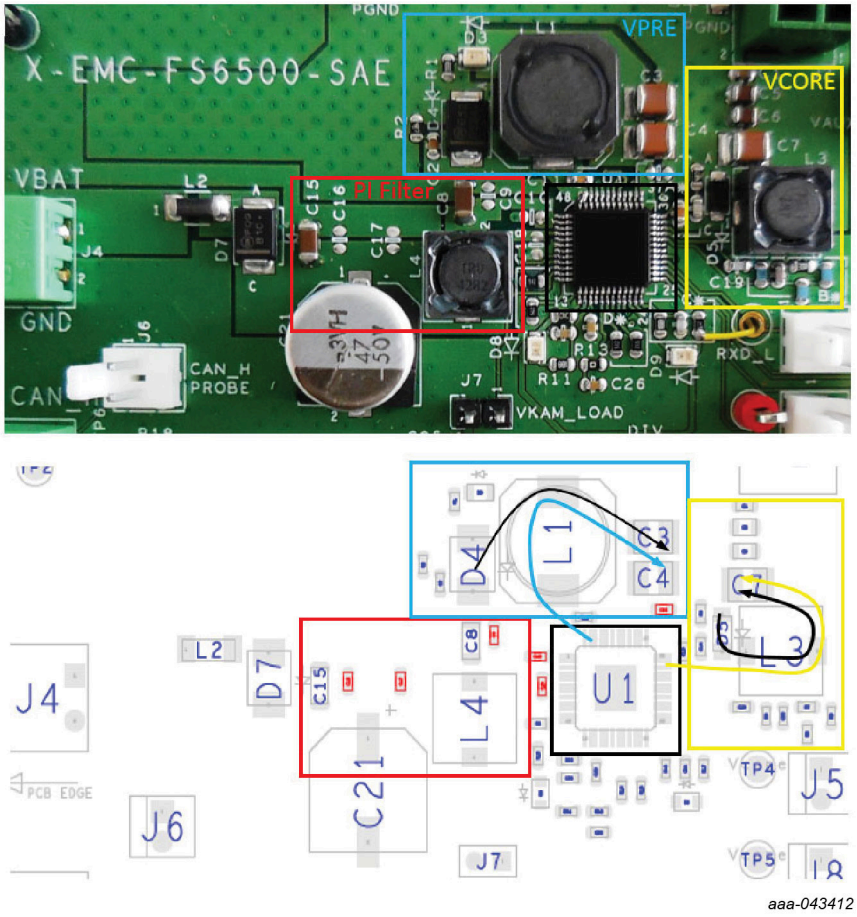


Figure 45. Placement example

- D7 is the reverse battery diode
- C21 is the V_{SUP} input capacitor which must be > 47 µF
- Place the input capacitor of the PI filter close to VSUP3 pin and the output capacitor close to VSUP1/2 pin
- V_{PRE} and V_{CORE} are located close together to facilitate the PGND local ground (SMPS ground)
- VPRE_SW and VCORE_SW output switching pins connected to inductors input pin number 1
- Place V_{CORE} compensation network components close to the device pin

- In Blue and Yellow, V_{PRE} and V_{CORE} current loops during inductor charging phase
- In Black, current loops during inductor discharging phase

11.2.8 Ground connection example

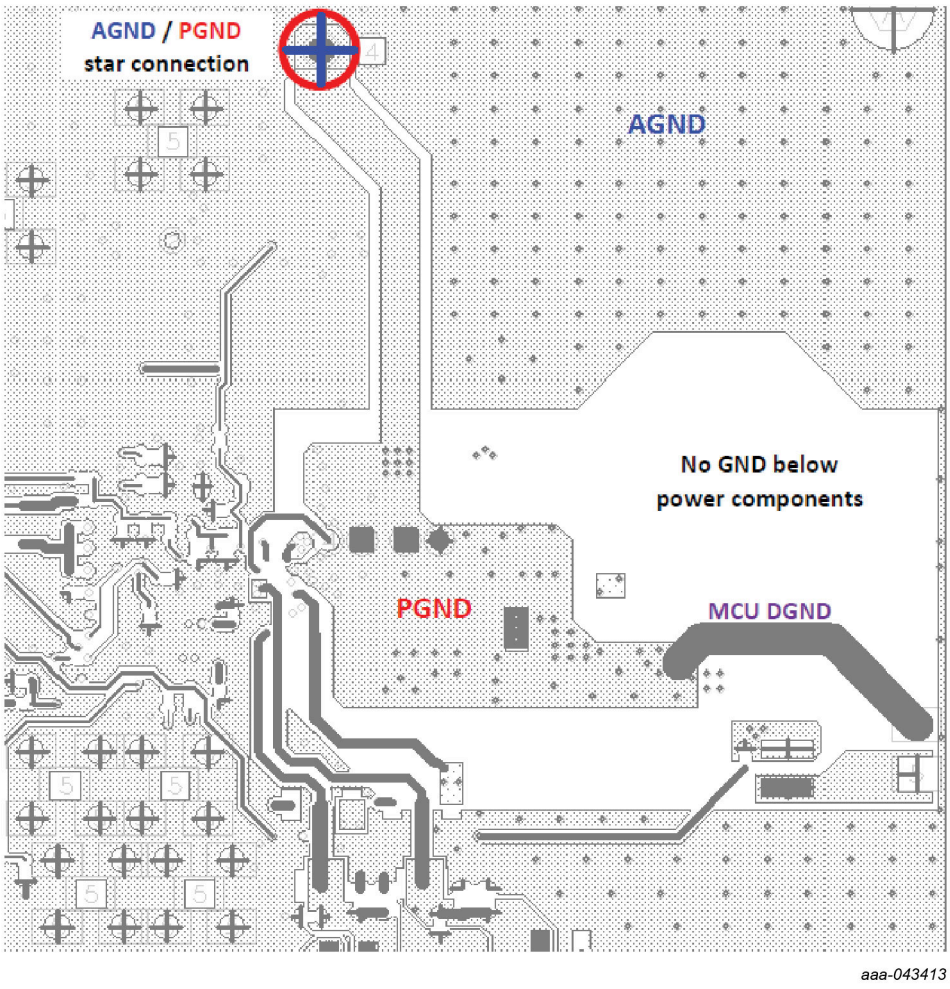


Figure 46. Ground connection example

- PGND is the SMPS (V_{PRE} and V_{CORE} for FS6500) power local ground
- AGND is the ground plane
- Star connection between PGND and AGND far from the local PGND (recommended at the input of the power connector)
- No AGND plane below the V_{PRE}/V_{CORE} SMPS power components
- MCU DGND connected to PGND

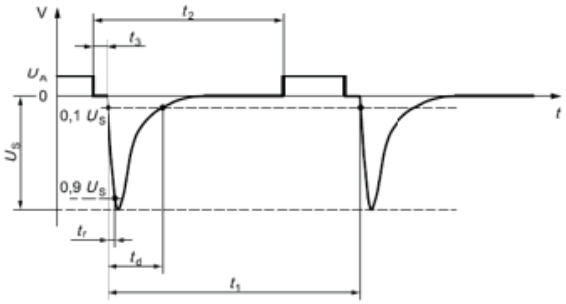
12 ISO pulses

12.1 Reference documents

- ISO 7637-2: 2011, Road vehicles – Electrical disturbances from conduction and coupling
  Part2: Electrical transient conduction along supply lines only
- ISO 16750-2: 2010, Road vehicles – Environmental conditions and testing for electrical and electronic equipment
  Part2: Electrical loads

12.2 Test pulses description

Test Pulse 1:

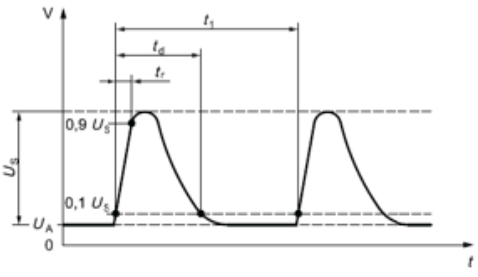


Parameters	Nominal 12 V system	Nominal 24 V system
U_s	−75 V to −150 V	−300 V to −600 V
R_i	10 Ω	50 Ω
t_d	2 ms	1 ms
t_r	$(1\ ^{0}_{-0,5})$ µs	$(3\ ^{0}_{-1,5})$ µs
t_1[a]	⩾0,5 s	
t_2	200 ms	
t_3[b]	<100 µs	

[a] t_1 shall be chosen such that it is the minimum time for the DUT to be correctly initialized before the application of the next pulse and shall be ⩾0,5 s.

[b] t_3 is the smallest possible time necessary between the disconnection of the supply source and the application of the pulse.

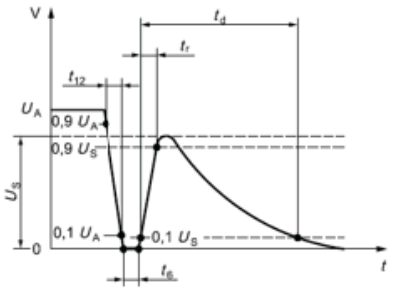
Test Pulse 2a:



Parameters	Nominal 12 V and 24 V system
U_s	+37 V to +112 V
R_i	2 Ω
t_d	0,05 ms
t_r	$(1\ ^{0}_{-0,5})$ µs
t_1[a]	0,2 s to 5 s

[a] The repetition time t_1 can be short depending on the switching. The use of a short repetition time reduces the test time.

Test Pulse 2b:

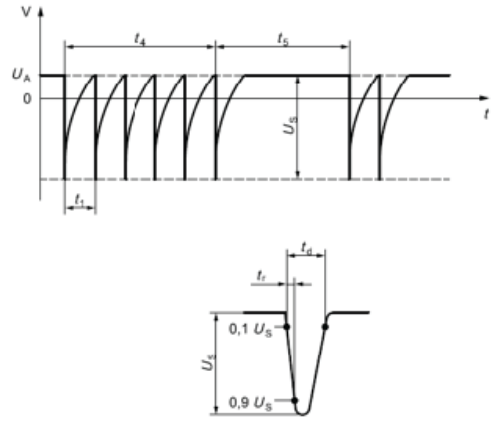


Parameters	Nominal 12 V system	Nominal 24 V system
U_s	10 V	20 V
R_i	0 Ω to 0,05 Ω	
t_d	0,2 s to 2 s	
t_{12}	1 ms ± 0,5 ms	
t_r	1 ms ± 0,5 ms	
t_6	1 ms ± 0,5 ms	
Repetition time: 0.5s		

aaa-043414

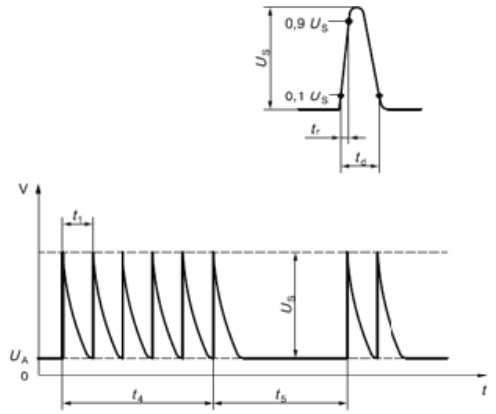
Figure 47. ISO test pulses description (1 of 3)

Test pulse 3a:



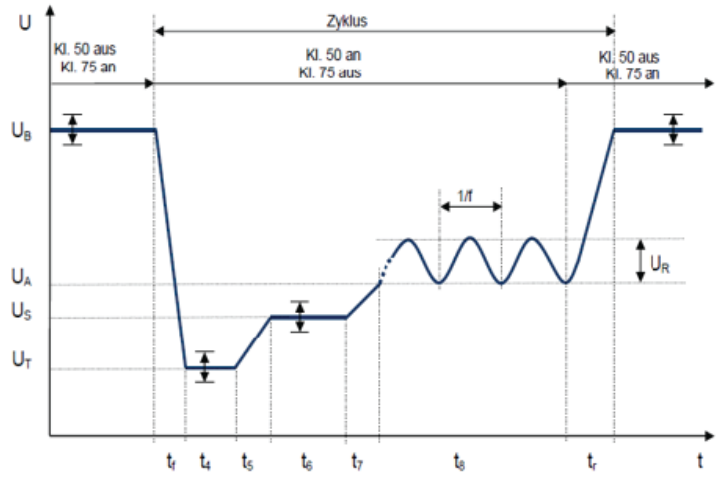
Parameters	Nominal 12 V system	Nominal 24 V system
U_s	–112 V to –220 V	–150 V to –300 V
R_i	50 Ω	
t_d	150 ns ± 45 ns	
t_r	5 ns ± 1,5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

Test pulse 3b:



Parameters	Nominal 12 V system	Nominal 24 V system
U_s	+75 V to +150 V	+150 V to +300 V
R_i	50 Ω	
t_d	150 ns ± 45 ns	
t_r	5 ns ± 1,5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

Test pulse 4 (cranking):

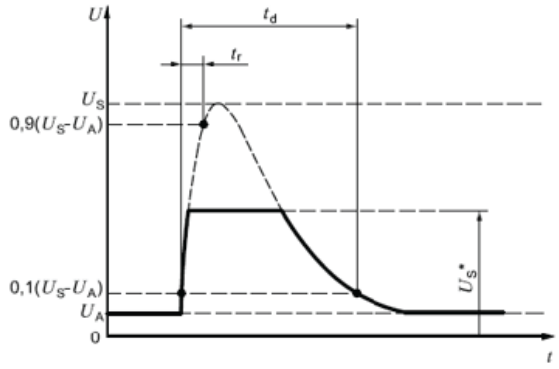


Parameter	Vpre Buck only	Vpre Buck-Boost
U_B	11,0V	11,0V
U_T	4,5V	3,2V $^{+0,2V}$
U_S	4,5V	5,0V
U_A	6,5V	6,0V
U_R	2V	2V
t_f	≤ 1ms	≤ 1ms
t_4	0ms	19ms
t_5	0ms	≤ 1ms
t_6	19ms	329ms
t_7	50ms	50ms
t_8	10s	10s
t_r	100ms	100ms
f	2Hz	2Hz
R_i	0,01Ω	0,01Ω
Pause between cycles	2s	2s
Number of cyles	10	10

aaa-043415

Figure 48. ISO test pulses description (2 of 3)

Test pulse 5b (load dump with centralized load dump suppression):



Parameter	Type of system		Minimum test requirements
	U_N = 12 V	U_N = 24 V	
U_S [a] V	$79 \leqslant U_S \leqslant 101$	$151 \leqslant U_S \leqslant 202$ V	5 pulses at intervals of 1 min
U_S* V	35	65	
R_i [a] Ω	$0,5 \leqslant R_i \leqslant 4$	$1 \leqslant R_i \leqslant 8$	
t_d ms	$40 \leqslant t_d \leqslant 400$	$100 \leqslant t_d \leqslant 350$	
t_r ms	$10\left(\frac{0}{-5}\right)$	$10\left(\frac{0}{-5}\right)$	

[a] If not otherwise agreed, use the higher voltage level with the higher value for internal resistance, or use the lower voltage level with the lower value for internal resistance.

aaa-043416

Figure 49. ISO test pulses description (3 of 3)

12.3 ISO pulses schematic

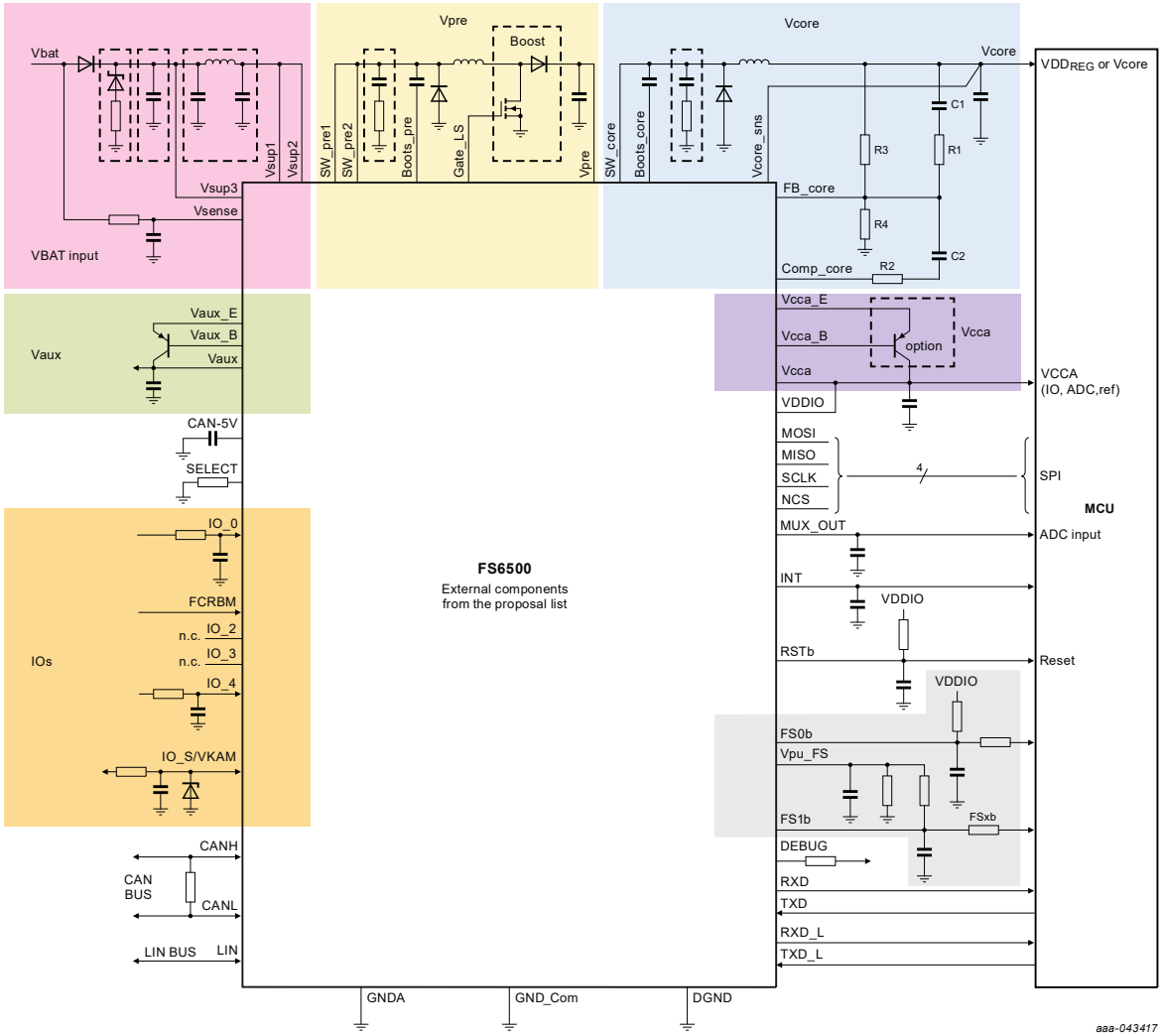


Figure 50. ISO pulses schematic

12.4 Product setup

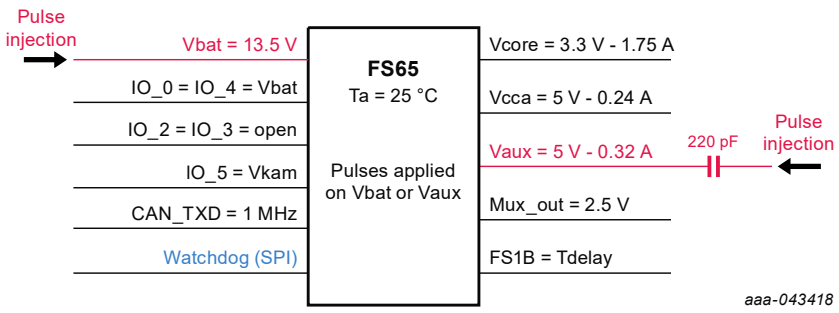


Figure 51. Product setup

Product setup in normal mode **without** fault (RSTB=1, **FS0B=FS1B=1**) and **with** fault (RSTB=1, **FS0B=FS1B=0**).

Fault: No watchdog refresh asserts FS0B low when Fault Error Counter = 3.

12.5 Results

Table 20. Results

Applied on	Pulse type	Nb of pulse or test time	Pulse description and product setup	Without Fault Class	With Fault Class
Vbat	Pulse 1	500	FaultClassTransient Test Pulse 1 (-150 V) - buck boost	C	A[1]
			Transient Test Pulse 1 (-150 V) - buck only	B	A[1]
	Pulse 2a	500	Transient Test Pulse 2a (+112 V) - buck boost	B	A
			Transient Test Pulse 2a (+112 V) - buck only	B	A
	Pulse 2b	10	Transient Test Pulse 2b - buck boost	C	A
			Transient Test Pulse 2b - buck only	C	A
	Pulse 3a	1 Hr	Transient Test Pulse 3a (-220 V) - buck boost	A	A
			Transient Test Pulse 3a (-220 V) - buck only	A	A
	Pulse 3b	1 Hr	Transient Test Pulse 3b (+150 V) - buck boost	A	A
			Transient Test Pulse 3b (+150 V) - buck only	A	A
	Pulse 4	10	Transient Test Pulse 4 (Vmin=2.7 V) - buck boost	A[2]	A
			Transient Test Pulse 4 (Vmin=4.5 V) - buck only - Vcca=Vaux=5 V	C[2]	A
			Transient Test Pulse 4 (Vmin=4.5 V) - buck only - Vcca=Vaux=3.3 V	A[2]	A
	Pulse 5	5	Transient Test Pulse 5 (≤40 V) - buck boost	B	B
			Transient Test Pulse 5 (≤40 V) - buck only	B	B
Vaux	Pulse 1	500	Transient Test Pulse 1 (-150 V) - buck boost	A	A
			Transient Test Pulse 1 (-150 V) - buck only	A	A
	Pulse 2a	500	Transient Test Pulse 2a (+112 V) - buck boost	A	A
			Transient Test Pulse 2a (+112 V) - buck only	A	A
	Pulse 3a	1 Hr	Transient Test Pulse 3a (-220 V) - buck boost	A	A
			Transient Test Pulse 3a (-220 V) - buck only	A	A
	Pulse 3b	1 Hr	Transient Test Pulse 3b (+150 V) - buck boost	A	A
			Transient Test Pulse 3b (+150 V) - buck only	A	A

[1] After FS1B assertion by the digital FS1B_TIME delay, if the analog backup delay is activated due to loss of power supply or loss of Fail-safe oscillator (considered as a Multiple Point Fault), a glitch will be generated at FS1B from VPU_FS to VPU_FS_TH voltage for the backup delay duration.
[2] Transient Test Pulse 4 (Vmin=2.7 V) - buck boost

12.6 Failing criteria

12.6.1 Class A without fault (RSTB = 1, FS0B = FS1B = 1)

- Monitoring of supply voltages: V_{CORE} (3.3 V) ±3.0 %, V_{CCA} (5.0 V) ±3.0 %, V_{AUX} (5.0 V) ±3.0 %, V_{CAN} (5.0 V) ±5.0 %
- No activation of RSTB, FS0B, FS1B
- No SPI configuration change (init. registers)
- No diag and status registers change

12.6.2 Class A with fault (RSTB = 1, FS0B = FS1B = 0)

- Fault still reported (FS0B = FS1B = 0) during and after the stress

12.6.3 Class B without fault (RSTB = 1, FS0B = FS1B = 1)

- All functions return automatically to within normal limits after exposure is removed
- One or more of the supply or reference voltages can go beyond specified tolerances
- No activation of RSTB, FS0B, FS1B
- No SPI configuration change (init. registers)
- No diag and status registers change

12.6.4 Class C without fault (RSTB = 1, FS0B = FS1B = 1)

- All functions return automatically to within normal limits after exposure is removed
- RSTB activation occurs
- FS0B or FS1B activation occurs (SPI command required to release FSxB pins)

12.6.5 Class C with fault (RSTB = 1, FS0B = FS1B = 0)

- One or more of fault outputs change (RSTB = 0 or FS0B = 1 or FS1B = 1) during the stress but return automatically to within normal limits after exposure is removed

13 Physical layers certifications

13.1 Reference documents

- ISO 11898-2:2003, Road vehicles - Controller area network (CAN), Part 2: High-speed medium access unit
- ISO 11898-5:2007, Road vehicles - Controller area network (CAN), Part 5: High-speed medium access unit with low-power mode
- C&S: CAN High Speed Transceiver Conformance Test according to "GIFT ICT group - Conformance test specification V1.0"
- IBEE (Zwickau): IEC TS 62228, Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Application – AUDI, BMW, Daimler, Porsche, Volkswagen – Revision 1.3 / 2012
- IBEE(Zwickau): IEC TS 62228, new draft definitions for "Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Application"; Volkswagen / 2016
- J2962-1/2: Latest draft version from 2014 (official release under voting)

13.2 Results

FS6500 and FS4500 have several part number derivatives depending on CAN and LIN physical layers embedded. The certification results for the different part numbers are summarized in Table 21.

Table 21. Certification results summary

	FS650xC	FS650xL	FS651xC	FS651xL	FS652xC	FS652xL	FS45xxC	FS45xxL
C&S Conformance	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
IBEE IEC_TS_62228_2012	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
SAE J2962-1	N/A	Pass	N/A	Pass	N/A	Pass	N/A	Pass
SAE J2962-2 (1)	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass
IBEE (draft) IEC_TS_62228_2016	Marginally failed on some frequencies (see details in chapter 12.4)							

Notes:
1. ESD protection option 2 is recommended to pass J2962-2
2. FS652x version requires PCB layout and GND connection attention due to high current (up to 2.2 A)

13.3 V_{BAT} conducted emission spectrum

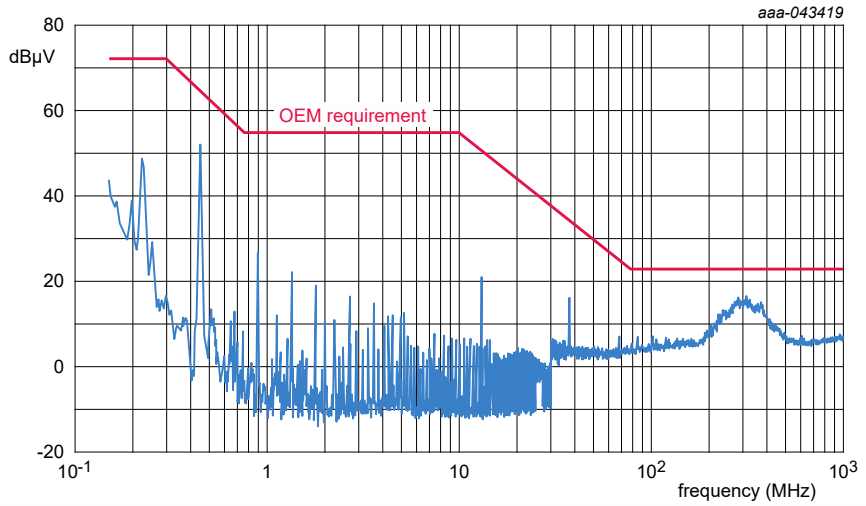


Figure 52. V_{BAT} spectrum during conducted emission

13.4 IBEE: IEC_TS_62228_2016 (draft)

- Conducted Emission marginally failed up to +3 dB at 3 MHz during CAN FD transmission at 2 Mbit/s (Figure 53).

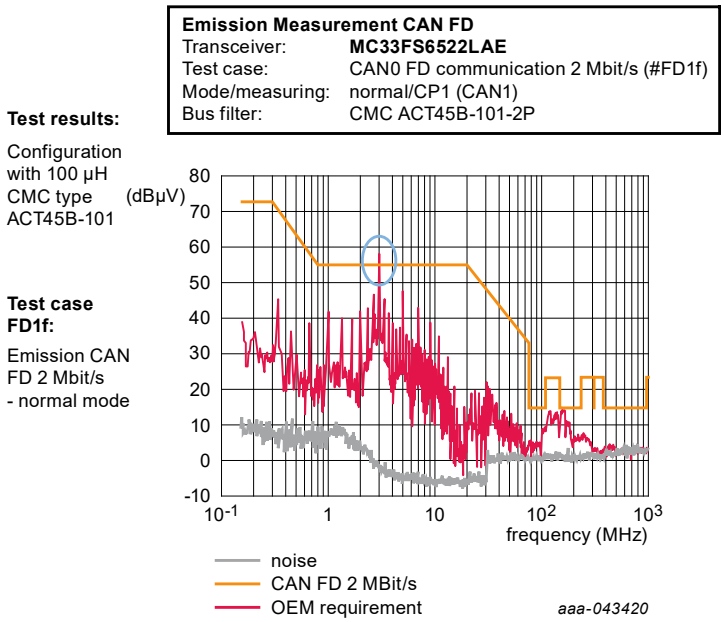


Figure 53. Conducted emission marginality

- Immunity marginally failed up to +1 dB within 2.2 to 2.6 MHz range, with mask on the receiver and balanced coupling setup, during CAN FD transmission at 2 Mbit/s (Figure 54).
- Immunity marginally failed up to +5 dB within 1.8 to 3.2 MHz range, with mask on the receiver and unbalanced coupling setup, during CAN FD transmission at 2 Mbit/s (Figure 54).

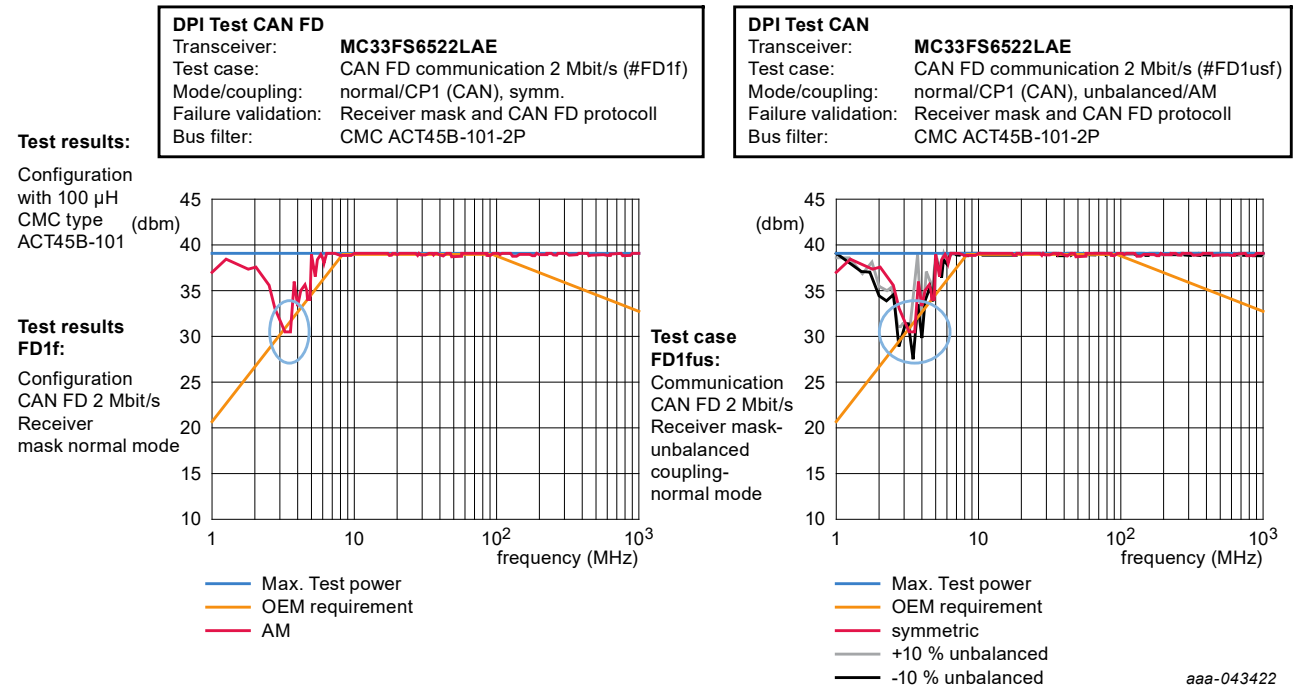


Figure 54. Direct power injection (DPI) marginality

14 FS6500 and FS4500 quick start guide

14.1 Flow chart

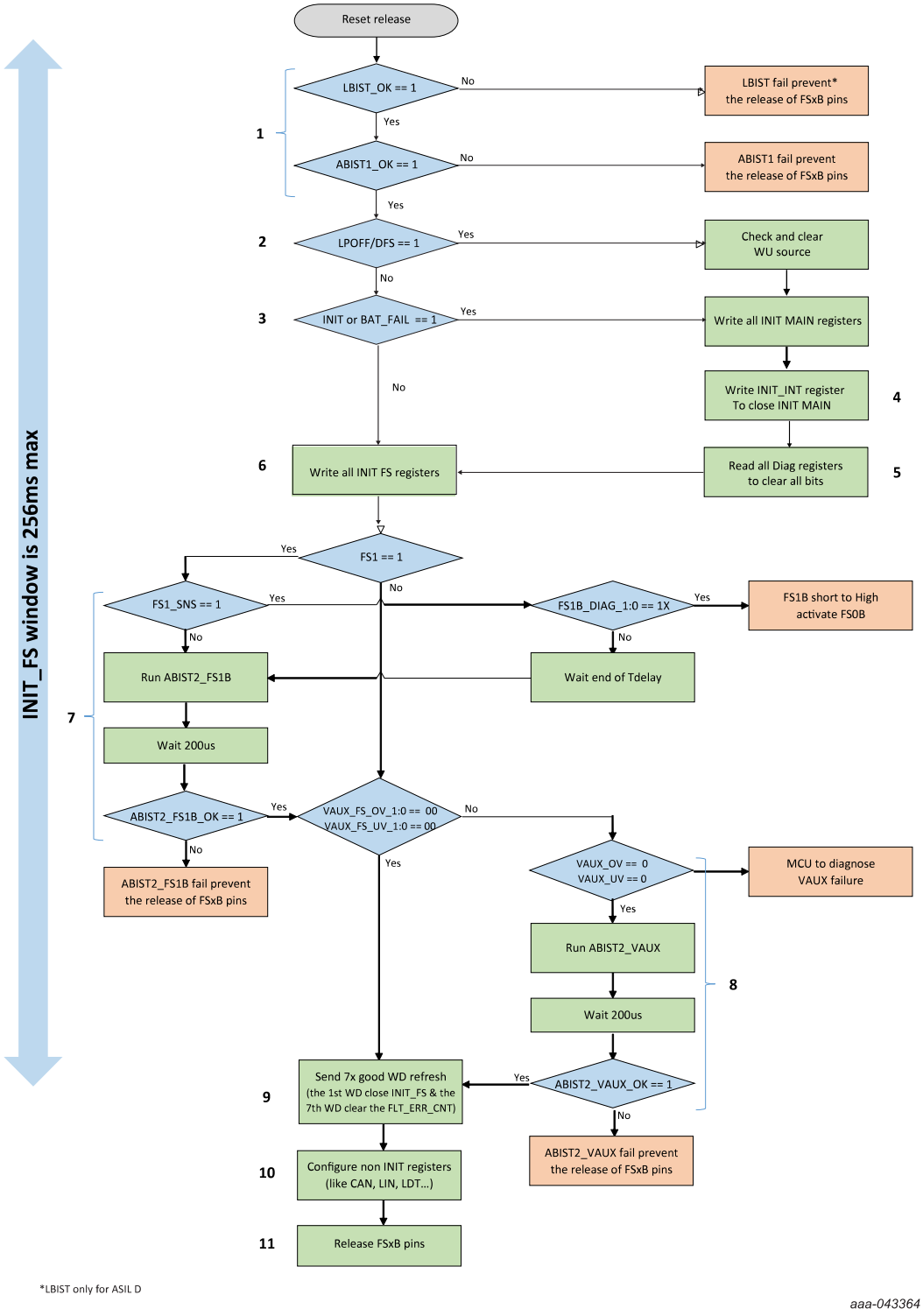


Figure 55. Flow chart

14.2 Start-up SPI sequence

Start-up SPI sequence example based on FS6500 and FS4500 flow chart from previous page (Fail-safe access in Green)

Table 22. Start-up SPI sequence

		Register	Read	Write	Comment
1	Check BIST	BIST	0x4400		Check LBIST_OK and ABIST1_OK bits[1]
2	Check WU source	WU_SOURCE	0x1200		Check Wake up sources if wake up from LPOFF
3	Check POR	INIT_VREG	0x0200		Check BAT_FAIL bit
4	INIT_MAIN	INIT_VREG		0x8210	Activate Vcan monitoring Vaux tracker disable
		INIT_WU1		0x8440	Default value IO_0 wake up on rising edge or high-level enable
		INIT_WU2		0x8600	Default value
		NIT_INH_INT		0x8A00	Default value
		INIT_INT		0x8900	Default value
5	Read Diag registers	DIAG_VPRE	0x1800		Clear VPRE_UV after POR or Wake up
		DIAG_VCORE	0x1A00		Clear VCORE_FB_UV after POR or Wake up
		DIAG_VCCA	0x1C00		Clear VCCA_UV after POR or Wake up
		DIAG_VAUX	0x1E00		Clear VAUX_UV after POR or Wake up
		DIAG_VSUP_VCAN	0x2000		Clear VSNS_UV and VSUP_UV_7 after POR Clear VCAN_UV after wake up
6	INIT_FS	INIT_FS1B_Timing		0xC265	Default value
		INIT_SUPERVISOR		0xC70C	Default value
		INIT_FAULT		0xC80C	FLT_ERR_CNT=6, FS1B has no impact on CAN
		INIT_FSSM		0xCB0C	IO_2:3 and IO_4:5 are not safety critical
		INIT_SF_IMPACT		0xCD18	Default value FS1B Tdelay, Reset only at WD_CNT_ERR final value
		INIT_WD_CNT		0xD90C	Default value WD_CNT_ERR = WD_CNT_RFR = 6
		INIT_VCORE_UVOV_IMPACT		0xE3E7	Default value VCORE_FB_OV impact on RSTB and FS0B, VCORE_FB_UV impact on FS0B only
		INIT_VCCA_UVOV_IMPACT		0xE5E7	Default value VCCA_OV impact on RSTB and FS0B, VCCA_UV impact on FS0B only
		INIT_VAUX_UVOV_IMPACT		0xE6E7	Default value VAUX_OV impact on RSTB and FS0B, VAUX_UV impact on FS0B only

Table 22. Start-up SPI sequence*...continued*

		Register	Read	Write	Comment
7	ABIST FS1B	Device_ID_FS	0x6800		Check FS1 bit
		RELEASE_FSxB	0x5400		Check FS1B_SNS bit
		BIST		0xC44D	Start FS1B ABIST
		BIST	0X4400		Check FS1B ABIST result
8	ABIST VAUX	BIST		0xC424	Start VAUX ABIST[2]
		BIST	0X4400		Check VAUX ABIST result
9	7x good WD refresh	WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD34D	Watchdog Answer to be calculated[3]
		WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD29B	Watchdog Answer to be calculated[3]
		WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD237	Watchdog Answer to be calculated[3]
		WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD26E	Watchdog Answer to be calculated[3]
		WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD2DC	Watchdog Answer to be calculated[3]
		WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD2B9	Watchdog Answer to be calculated[3]
		WD_LFSR	0x5000		Read LFSR
		WD_ANSWER		0xD372	Watchdog Answer to be calculated[3]
10	CAN_LIN_ MODE	CAN_LIN_MODE		0xB0C0	CAN in normal operation mode
11	RELEASE FSxB	SF_OUTPUT_ REQUEST		0xD60C	Close S1 switch between VPRE and VPU_FS[4]
		WD_LFSR	0x5000		Read LFSR
		RELEASE_FSxB		0xD4A7	Release both FS0B and FS1B at the same time RELEASE_FSxB_4:0 to be calculated

[1] LBIST for ASIL D only
[2] ABIST on FS1B and VAUX can be launch simultaneously with SPI command 0xC465. The wait time remains 200 µs for both ABIST.
[3] For ASIL B version, only write commands in WD_ANSWER register are needed.
[4] When FS1B is used, the switch S1 can be closed earlier, just after ABIST2 on FS1B, to allow the charge of Cpd while the Fault Error Counter is cleared and reduce the application starting time.

14.3 Reading registers overview

Table 23. Reading registers overview

Logic	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read command
MAIN	INIT_VREG	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	RESERVED	TAUX_LIM_OFF	VAUX_TRK_EN	BATFAIL	0x0200
	INIT_WU1	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0	0x0400
	INIT_WU2	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	RESERVED	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0	0x0600
	INIT_INT	INT_DURATION	INT_INH_LIN	INT_INH_ALL	INT_INH_VSNS	INT_INH_VPRE	INT_INH_VCORE	NT_INH_ VOTHERS	INT_INH_CAN	0x0800
	INIT_INH_INT	RESERVED	RESERVED	RESERVED	NT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0	0x0A00
	LONG_DURATION_TIMER	F2	F1	F0	REG_SE	LDT_RUNNING	MODE	LDT ENABLE	LDT_INT	0x0C00
	HW_CONFIG	LS_DETECT	RESERVED	VCCA_PNP_ DETECT	VCCA_HW	VAUX_HW	1	DFS_HW	DBG_HW	0x1000
	WU_SOURCE	IO_5_WU	IO_4_WU	IO_3_WU	IO_2_WU	IO_0_WU	AUTO_WU	LDT_WU	PHY_WU	0x1200
	DEVICE_ID	VCORE_1	VCORE_0	PHY1	PHY0	VKAM	DEV_REV_2	DEV_REV_1	DEV_REV_0	0x1400
	IO_INPUT	IO_5	IO_4	0	IO_3	O_2	0	0	IO_0	0x1600
	DIAG_VPRE	BOB	VPRE_STATE	TWARN_PRE	TSD_PRE	VPRE_OV	VPRE_UV	ILIM_PRE	0	0x1800
	DIAG_VCORE	0	VCORE_STATE	TWARN_CORE	TSD_CORE	VCORE_FB_OV	VCORE_FB_UV	0	0	0x1A00
	DIAG_VCCA	0	0	TWARN_CCA	TSD_CCA	VCCA_OV	VCCA_UV	ILIM_CCA	ILIM_CCA_OFF	0x1C00
	DIAG_VAUX	0	0	0	TSD_AUX	VAUX_OV	VAUX_UV	LIM_AUX	ILIM_AUX_OFF	0x1E00
	DIAG_VSUP_VCAN	VSNS_UV	VSUP_UV_7	IPFF	TSD_CAN	VCAN_OV	VCAN_UV	ILIM_CAN	0	0x2000
	DIAG_CAN_FD	CANH_BATT	CANH_GND	CANL_BATT	CANL_GND	CAN_DOM	0	RXD_REC	TXD_DOM	0x2200
	DIAG_CAN_LIN	LIN_DOM	TXDL_DOM	0	RXDL_REC	LIN_OT	0	CAN_OT	CAN_OC	0x2400
	DIAG_SPI	SPI_ERR	0	SPI_CLK	0	SPI_REQ	0	SPI_PARITY	0	0x2600
	MODE	VKAM_EN	RESERVED	RESERVED	RESERVED	INIT	NORMAL	DFS	LPOFF	0x2A00
	REG_MODE	RESERVED	RESERVED	RESERVED	RESERVED	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN	0x2C00
	IO_OUT_AMUX	IO_OUT_4_EN	IO_OUT_4	RESERVED	RESERVED	RESERVED	AMUX_2	AMUX_1	AMUX_0	0x2E00
	CAN_LIN_MODE	CAN_MODE_1	CAN_MODE_0	CAN_AUTO_DIS	LIN_MODE_1	LIN_MODE_0	LIN_AUTO_DIS	CAN_WU	LIN_WU	0x3000
	LDT_AFTER_RUN_1	B15	B14	B13	B12	B11	B10	B9	B8	0x3400
	LDT_AFTER_RUN_2	B7	B6	B5	B4	B3	B2	B1	B0	0x3600
	LDT_WAKE_UP_1	B23	B22	B21	B20	B19	B18	B17	B16	0x3800
	LDT_WAKE_UP_2	B15	B14	B13	B12	B11	B10	B9	B8	0x3A00
	LDT_WAKE_UP_3	B7	B6	B5	B4	B3	B2	B1	B0	0x3C00
FAIL-SAFE	INIT_FS1B_TIMING	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0	0x4200
	BIST	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	LBIST_OK[1]	ABIST2_FS1B_OK	ABIST2_VAUX_OK	ABIST1_OK	0x4400
	INIT_SUPERVISOR	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_ RANGE	0x4600
	INIT_FAULT	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FLT_ERR_FS	FS1B_CAN_ IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0	0x4800
	INIT_FSSM	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	IO_45_FS	IO_23_FS[1]	PS[1]	RSTB_DURATION	0x4A00
	INIT_SF_IMPACT	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	TDLY_TDUR	DIS_8S	WD_IMPACT_1	WD_IMPACT_0	0x4C00
	WD_WINDOW	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0	0x4E00

Table 23. Reading registers overview*...continued*

Logic	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read command
	WD_LFSR	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0	0x5000
	WD_ANSWER	RSTB	FSxB	WD_BAD_ DATA[1]	FSO_G	IO_FS_G	WD_BAD_ TIMING	ERR_INT_HW	ERR_INT_SW	0x5200
	RELEASE_FSxB	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	RESERVED	FS1B_SNS	FS0B_SNS	RSTB_SNS	0x5400
	SF_OUTPUT_REQUEST	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	FS1B_DRV	FS1B_DLY_DRV	FS0B_DRV	RSTB_DRV	0x5600
	INIT_WD_CNT	SPI_FS_ERR	SPI_FS_CLK	PI_FS_REQ	SPI_FS_PARITY	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0	0x5800
	INIT_WD_CNT	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR_0	0x5800
	DIAG_SF_IOS	RSTB_EXT	RSTB_DIAG	FS0B_DIAG_1	FS0B_DIAG_0	FS1B_DIAG_1	FS1B_DIAG_0	IO_23_FAIL[1]	IO_45_FAIL	0x5A00
	WD_COUNTER	WD_ERR_2	WD_ERR_1	WD_ERR_0	RESERVED	WD_RFR_2	WD_RFR_1	WD_RFR_0	RESERVED	0x5C00
	DIAG_SF_ERR	FLT_ERR_2	FLT_ERR_1	FLT_ERR_0	RESERVED	V2P5_M_A_OV	V2P5_M_D_OV	FCRBM_OV	FCRBM_UV	0x5E00
	INIT_VCORE_OVUV_IMPACT	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCORE_FS_OV_1	VCORE_FS_OV_0	VCORE_FS_UV_1	VCORE_FS_UV_0	0x6200
	INIT_VCCA_OVUV_IMPACT	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0	0x6400
	INIT_VAUX_OVUV_IMPACT	SPI_FS_ERR	SPI_FS_CLK	SPI_FS_REQ	SPI_FS_PARITY	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0	0x6600
	DEVICE_ID_FS	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DFS_HW	FS1	0x6800

[1] RESERVED in ASIL B

14.4 Writing registers overview

Table 24. Writing registers overview

Logic	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Read command
MAIN	INIT_VREG	ICCA_LIM	TCCA_LIM_OFF	IPFF_DIS	VCAN_OV_MON	0	TAUX_LIM_OFF	VAUX_TRK_EN	0	0x8300
	INIT_WU1	WU_IO0_1	WU_IO0_0	WU_IO2_1	WU_IO2_0	WU_IO3_1	WU_IO3_0	WU_IO4_1	WU_IO4_0	0x8440
	INIT_WU2	WU_IO5_1	WU_IO5_0	CAN_DIS_CFG	CAN_WU_TO	0	LIN_J2602_DIS	LIN_SR_1	LIN_SR_0	0x8600
	INIT_INT	INT_DURATION	INT_INH_LIN	INT_INH_ALL	INT_INH_VSNS	INT_INH_VPRE	INT_INH_VCORE	NT_INH_ VOTHERS	INT_INH_CAN	0x8900
	INIT_INH_INT	0	0	0	NT_INH_5	INT_INH_4	INT_INH_3	INT_INH_2	INT_INH_0	0x8A00
	LONG_DURATION_TIMER	F2	F1	F0	REG_SE		MODE	LDT ENABLE	0	0x8D04
	MODE	VKAM_EN	LP_OFF_AUTO_ WU	GO_LPOFF	INT_REQ	Secure_3	Secure_2	Secure_1	Secure_0	0xAB0C
	REG_MODE	VCORE_EN	VCCA_EN	VAUX_EN	VCAN_EN	Secure_3	Secure_2	Secure_1	Secure_0	0xADF3
	IO_OUT_AMUX	IO_OUT_4_EN	IO_OUT_4	0	0	0	AMUX_2	AMUX_1	AMUX_0	0xAE00
	CAN_LIN_MODE	CAN_MODE_1	CAN_MODE_0	CAN_AUTO_DIS	LIN_MODE_1	LIN_MODE_0	LIN_AUTO_DIS	0	0	0xB0B4
	LDT_AFTER_RUN_1	B15	B14	B13	B12	B11	B10	B9	B8	0xB500
	LDT_AFTER_RUN_2	B7	B6	B5	B4	B3	B2	B1	B0	0xB600
	LDT_WAKE_UP_1	B23	B22	B21	B20	B19	B18	B17	B16	0xB900
	LDT_WAKE_UP_2	B15	B14	B13	B12	B11	B10	B9	B8	0xBA00
	LDT_WAKE_UP_3	B7	B6	B5	B4	B3	B2	B1	B0	0xBC00
FAIL-SAFE	INIT_FS1B_TIMING	FS1B_TIME_3	FS1B_TIME_2	FS1B_TIME_1	FS1B_TIME_0	Secure_3	Secure_2	Secure_1	Secure_0	0xC265
	BIST	0	ABIST2_FS1B	ABIST2_VAUX	0	Secure_3	Secure_2	Secure_1	Secure_0	0xC40C
	INIT_SUPERVISOR	VCORE_5D	VCCA_5D	VAUX_5D	FS1B_TIME_ RANGE	Secure_3	Secure_2	Secure_1	Secure_0	0xC70C
	INIT_FAULT	FLT_ERR_FS	FS1B_CAN_ IMPACT	FLT_ERR_IMP_1	FLT_ERR_IMP_0	Secure_3	Secure_2	Secure_1	Secure_0	0xC859
	INIT_FSSM	IO_45_FS	IO_23_FS[1]	PS[1]	RSTB_DURATION	Secure_3	Secure_2	Secure_1	Secure_0	0xCB4D
	INIT_SF_IMPACT	TDLY_DUR	DIS_8S	WD_IMPACT_1	WD_IMPACT_0	Secure_3	Secure_2	Secure_1	Secure_0	0xCD18
	WD_WINDOW	WD_WINDOW_3	WD_WINDOW_2	WD_WINDOW_1	WD_WINDOW_0	Secure_3	Secure_2	Secure_1	Secure_0	0xCE30
	WD_LFSR	WD_LFSR_7	WD_LFSR_6	WD_LFSR_5	WD_LFSR_4	WD_LFSR_3	WD_LFSR_2	WD_LFSR_1	WD_LFSR_0	0xD0B2
	WD_ANSWER	WD_ANSWER_7	WD_ANSWER_6	WD_ANSWER_5	WD_ANSWER_4	WD_ANSWER_3	WD_ANSWER_2	WD_ANSWER_1	WD_ANSWER_0	0xD34D
	RELEASE_FSxB	RELEASE_FSxB_7	RELEASE_FSxB_6	RELEASE_FSxB_5	RELEASE_FSxB_4	RELEASE_FSxB_3	RELEASE_FSxB_2	RELEASE_FSxB_1	RELEASE_FSxB_0	0xD500
	SF_OUTPUT_REQUEST	FS1B_LOW_REQ	FS1B_DLY_REQ	FS0B_LOW_REQ	RSTB_REQ	Secure_3	Secure_2	Secure_1	Secure_0	0xD64D
	INIT_WD_CNT	WD_CNT_ERR_1	WD_CNT_ERR_0	WD_CNT_RFR_1	WD_CNT_RFR0	Secure_3	Secure_2	Secure_1	Secure_0	0xD90C
	INIT_VCORE_OVUV_IMPACT	VCORE_FS_OV_1	VCORE_FS_OV_0	VCORE_FS_UV_1	VCORE_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0	0xE3E7
	INIT_VCCA_OVUV_IMPACT	VCCA_FS_OV_1	VCCA_FS_OV_0	VCCA_FS_UV_1	VCCA_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0	0xE6E7
	INIT_VAUX_OVUV_IMPACT	VAUX_FS_OV_1	VAUX_FS_OV_0	VAUX_FS_UV_1	VAUX_FS_UV_0	Secure_3	Secure_2	Secure_1	Secure_0	

[1] RESERVED in ASIL B

14.5 Release FSxB calculation procedure

1- ABIST2_VAUX_OK = 1, except if VAUX_FS_OV_1:0 = VAUX_FS_UV_1:0 = "00"

2- ABIST2_FS1B_OK = 1, if part number with FS1B

3- Close S1 switch between VPRE and VPU_FS if FS1B is pulled up to VPU_FS

4- Fault Error Counter must be at "0". Decrease it with "N" consecutive good WD refresh with "N" = FLT_ERR_2:0 x (WD_RFR_2:0 + 1)

5- Read LSFR data via the SPI

6- Invert all bits of LFSR and swap MSB and LSB bits. The new byte is used to fill in the RELEASE_FSxB register as described in the following table:

	WD_LFSR_7:0	b7	b6	b5	b4	b3	b2	b1	b0
Release FS0B	RELEASE_FSxB_7:0	0	1	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b3}$	$\overline{b4}$
Release FS1B	RELEASE_FSxB_7:0	1	1	0	$\overline{b3}$	$\overline{b4}$	$\overline{b5}$	$\overline{b6}$	$\overline{b7}$
Release FS0B and FS1B	RELEASE_FSxB_7:0	1	0	1	$\overline{b0}$	$\overline{b1}$	$\overline{b2}$	$\overline{b6}$	$\overline{b7}$
Note: It is recommended to release FS0B in application mode rather than boot loader mode.									

The RELEASE_FSxB write command must be done after the WD_LFSR read command, within the same WD period, and one time only. If FS0B and FS1B are released sequentially, the procedure must be done a first time for FS0B, and a second time for FS1B.

14.6 Watchdog answer calculation procedure

(Note: This calculation procedure is only needed for ASIL D rated devices. As per ASIL B devices, any writing in WD_ANSWER register is sufficient to get a good WD refresh (simple watchdog.)

At power up, when the RSTB is released as high (after around 16.5 ms), the INIT phase starts for a maximum duration of 256 ms and this is considered as a fully open watchdog window. During this initialization phase the MCU sends the seed for the LFSR, or uses the default LFSR value generated (0xB2), available in the WD_LFSR register. Using this LFSR, the MCU performs a simple calculation based on the formula below. As an example, the result of this calculation based on LFSR default value (0xB2) is 0x4D.

15 References

The following are URLs where you can obtain information on related NXP products and application solutions:

NXP.com support pages	Description	URL
FS6500-FS4500	Power System Basis Chip with CAN Flexible Data and LIN Transceivers data sheet	https://www.nxp.com/webapp/Download?colCode=FS6500-FS4500
FS6500-FS4500 (ASIL B)	FS65-FS45 ASIL B Datasheet (Grade 1)	https://www.nxp.com/webapp/Download?colCode=FS6500-FS4500-ASILB&appType=moderatedWithoutFAE
AN4661	Designing the VCORE Compensation Network	http://www.nxp.com/files/analog/doc/app_note/AN4661.pdf
AN4388	Quad Flat Package (QFP)	http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf
Power Dissipation Tool (Excel file)		http://www.nxp.com/files/analog/software_tools/FS6500-FS4500-power-dissipation-calculator.xlsx
Vcore compensation network simulation tool (CNC)		Upon demand
Non ISO pulses report		Upon demand
FMEDA	FS6500/FS4500 FMEDA	Upon demand
FS6500-FS4500 SMUG	FS6500/FS4500 Safety Manual - User Guide	https://www.nxp.com/webapp/Download?colCode=FS6500-FS4500SMUG
FS6500-FS4500 SMUG (ASIL B)	FS6500–FS4500, ASILB Grade 1, safety manual	https://www.docstore.nxp.com/products/product-hierarchy?query=sm646612
KITFS6523 CAEEVM	FS6500 Evaluation board with FS1B	http://www.nxp.com/products/power-management/linear-regulator/fs6523-system-basis-chip-dcdc-2.2a-vcore-fs1b-ldt-can:KITFS6523CAEEVM
KITFS6522 LAEEVM	FS6500 Evaluation board with LIN	http://www.nxp.com/products/power-management/linear-regulator/fs6522-system-basis-chip-dcdc-2.2a-vcore-ldt-can-lin:KITFS6522LAEEVM
KITFS4503 CAEEVM	FS4500 Evaluation board with FS1B	http://www.nxp.com/products/power-management/linear-regulator/fs4503-system-basis-chip-linear-0.5a-vcore-fs1b-ldt-can:KITFS4503CAEEVM
FRDMFS6523 CAEVM	FS6500 Freedom board with FS1B	http://www.nxp.com/about/about-nxp/technology-leadership/process-technology/thin-film-storage-tfs-with-flexmemory-technology/fs6523-system-basis-chip-with-kl25z:FRDMFS6523CAEVM
FRDMFS4503 CAEVM	FS4500 Freedom board with FS1B	http://www.nxp.com/about/about-nxp/technology-leadership/process-technology/thin-film-storage-tfs-with-flexmemory-technology/freedom-board-fs4503-system-basis-chip-ldo-500ma-vcore-fs1b-ldt-can:FRDMFS4503CAEVM
FS6500 Product Summary Page		http://www.nxp.com/products/power-management/linear-regulator/fail-silent-system-basis-chip-with-dc-dc-up-to-2.2a-on-vcore:FS6500
FS4500 Product Summary Page		http://www.nxp.com/products/power-management/linear-regulator/fail-silent-system-basis-chip-with-ldo-up-to-500ma-on-vcore:FS4500
Analog Power Management Home Page		http://www.nxp.com/products/power-management

16 Revision history

Revision	Date	Description
10.0	27 August 2024	• Removed from NXP secure files and published on nxp.com • Updated to current template • Updated legal information
9.0	7/2023	• Updated Figure 1 • Added three entries to Table 5 • Added Section 3.12, VAUX 3.3 V tracker regulating at 5 V during LBIST after wake-up • Added Section 3.13, VAUX 3.3 V tracker oscillation at light load • Added Section 3.14, Fault error counter counting issue • Updated Figure 8 • Rearranged entries in Table 22
8.0	9/2021	• Converted from FrameMaker format to DITA format • Assigned CDS art numbers to all art • Added ASIL B references throughout, as needed • Added ASIL B part number selector guide in Section 2.1.3 "Part number selector guide" • Updated Section 3 to include ASIL B events • Updated D_Vcore reference in Table 11 • Updated Figure 55 • Adjusted Table 23 to accommodate ASIL B addition • Adjusted Table 24 to accommodate ASIL B addition • Added Section 3.7 "FS1B backup delay automatically triggered" through Section 3.11 "VAUX short to VBAT at start-up"
7.0	6/2019	• Added Section 4.2, Connection of unused pins, page 12 • Updated Section 5.3, VAUX, page 15 • Updated Section 6.7, Reset and fail-safe outputs - RSTB, FS0B, and FS1B, page 33 • Updated Section 14.1, Flow chart, page 53
6.0	10/2018	• Added Section 3.3, FS1b TIME DELAY, page 9 • Added Section 3.4, NO WAKE UP BY CAN, page 9 • Added Section 3.5, Unexpected OV/UV when returning from low power off mode, page 9 • Added Section 3.6, Unexpected CAN_5V Ilim flag, page 9
5.0	11/2017	• Added Section 2.9, Watchdog, page 5 • Added Section 3.2, LPOFF current excursion, page 9 • Added Section 2.11, MCU programming, page 6 • Updated Section 6.5, FS6500 and FS4500 linear regulators, VCCA and VAUX, page 30 • Updated Section 13.1, Reference documents, page 51 • Updated Section 13.2, Results, page 51 • Added Section 13.4, IBEE: IEC_TS_62228_2016 (draft), page 52 • Applies to silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
4.0	5/2017	• Updated Figure 1 • Updated Section 2.11, MCU programming, page 6 • Applies to silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
3.0	1/2017	• Updated Physical layers certifications results Section 13.2, Results, page 51 • Updated Section 14.2, Start-up SPI sequence, page 54 • Updated Section 14.3, Reading registers overview, page 55 • Updated Section 14.4, Writing registers overview, page 56 • Corrected FS0B release command script calculation Section 14.5, Release FSxB calculation procedure, page 57

Revision	Date	Description
		• Applies to silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
2.0	10/2016	• Updated document to NXP form and style • Added MCU Mapping with FS6500 and FS4500 Section 9, MCU mapping with FS6500 and FS4500, page 38 • Added ISO Pulses Section 12, ISO pulses, page 46 • Added Physical Layers Certification Section 13, Physical layers certifications, page 51 • Added FS6500 and FS4500 Quick Starter Guide Section 14, FS6500 and FS4500 quick starter guide, page 53 • Applies to silicon revision DEV_REV_2:0 = "010" in DEVICE_ID register
1.0	1/2016	• Initial Release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

Suitability for use in automotive applications (functional safety) — This NXP product has been qualified for use in automotive applications. It has been developed in accordance with ISO 26262, and has been ASIL classified accordingly. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents