Freescale Semiconductor
Application Note

Document Number: AN4200
Rev. 0, 09/2010

Modifying Bootloader and Kernel to Support a Different SDRAM on the i.MX25 using WinCE 6.0™

by *Multimedia Applications Division*
Freescale Semiconductor, Inc.
Austin, TX

This application note describes the software changes that are required to support a different synchronous dynamic random access memory (SDRAM) in an i.MX25 processor using Windows Embedded CE 6.0 (WinCE 6.0) board support package (BSP). This includes the basic SRAM parameters, different SRAM configuration options in the i.MX25 processor, and files that are required to be modified in the BSP.

Contents

1 Introduction

SDRAM is the fundamental device of any design that uses the i.MX25 system-on-chip (SoC). The components used in the reference designs are selected in such a way to satisfy the requirements of the customers. However, when SDRAM is required to be changed, it is difficult to solve the requirements of the customers. This application note provides information that is required to perform software changes in the WinCE 6.0 BSP when an SDRAM is changed in the i.MX25 processors.

freescale™ semiconductor

1.1 Basic SDRAM AC Parameters

The most important SDRAM parameters for the configuration of the enhanced SDRAM controller (ESDRAMC) in the i.MX25 processor are the SDRAM AC operating condition parameters. Table 1 lists the SDRAM AC parameters that are used to configure the ESDRAMC in the i.MX25 processor.

Table 1. Basic SDRAM AC Parameters

Symbol	Description
t_{MDR}	LOAD MODE REGISTER (LMR) to ACTIVE or REFRESH command
t_{WR}	Write recovery time (write to precharge)
t_{RAS}	ACTIVE to PRECHARGE command
t_{RRD}	Bank A ACTIVE to bank B ACTIVE command
t_{CAS}	READ to DATA out period (known as CAS LATENCY)
t_{RP}	PRECHARGE command period
t_{RCD}	ACTIVE to READ or WRITE delay
t_{RC}	ACTIVE to ACTIVE command period
t_{WTR}	LPDDR READ to WRITE command delay
t_{XP}	LPDDR EXIT power down to the immediate valid command delay

1.2 ESDRAMC Configuration Options

ESDRAMC provides interface and control for the SDRAM memories. The ESDRAMC module of the i.MX25 processor is highly configurable and can operate with multiple SDRAM. This module supports the following features:

- Optimizes memory access in consecutive memory locations through memory command anticipation (latency hiding):
  - Hides latency by optimizing the commands to both the chip selects (command anticipation)
  - Supports SDRAM burst length configuration of 4 or 8 words
  - Supports different internal burst lengths (1/4/8 words) by using the burst truncate commands
- Supports SDRAM, low power double data rate (LPDDR), and non-mobile double data rate 1 (DDR1) devices of four banks (with a memory capacity of 64 Mbytes, 128 Mbytes, 256 Mbytes, or 512 Mbytes and 1 Gbyte) and single data rate. However, support for the DDR2 devices is limited as it allows four banks without the ODT control signal:
  - Two independent chip selects
  - Up to 128 Mbytes per chip select
  - Activates up to four banks simultaneously per chip select
- Supports 16-bit LPDDR/DDR2 devices
- Supports PC133-compliant interface:
  - 133 MHz system clock, which is achievable with an option of –7 for the PC133-compatible memories

  - Single fixed-length (4/8 word) burst or full-page access ESDRAMC
  - Access time of 9-1-1-1-1-1-1-1 at 133 MHz frequency (when the memory bus is available for read access, the row is opened and the CAS latency is configured to 3 cycles). The access time includes the M3IF delay (assuming that there is no arbitration penalty)
- Supports software that are configurable for different system and memory device requirements:
  - 16-bit memory data bus width (same for both the chip selects)
  - Number of row and column addresses
  - Row cycle delay (t_{RC})
  - Row precharge delay (t_{RP})
  - Row to column delay (t_{RCD})
  - Column to data delay (CAS latency)
  - LMR to ACTIVE command (t_{MRD})
  - WRITE to PRECHARGE command (t_{WR})
  - WRITE to READ command (t_{WTR}) for the LPDDR memories
  - LPDDR exit power down to the immediate valid command delay (t_{XS})
  - ACTIVE to PRECHARGE command (t_{RAS})
  - Bank active to ACTIVE command (t_{RRD})

These features can be configured in both the chip selects. The ESDRAMC has eleven configuration registers. However, this application note focuses only on three configuration registers—the registers that require modifications when SDRAM is replaced. See the *i.MX25 Multimedia Applications Processor Reference Manual* (IMX25RM) for information about the others registers.

The three ESDRAMC configuration registers are described as follows:

- ESDCTLx—used to configure the ESDRAMC. The i.MX25 processor has two ESDCTLx registers—one for each chip select. This register controls various memory and control settings. Table 2 gives a description of the ESDCTLx register fields.

NOTE

See the *i.MX25 Multimedia Applications Processor Reference Manual* (IMX25RM) for more information about the ESDCTLx register.

Table 2. ESDCTLx Register Fields

Bits	Name	Description
31	SDE	ESDRAMC enable This control bit enables/disables the ESDRAMC. 0 Disabled 1 Enabled
30–28	SMODE	SDRAM controller operating mode This bit field determines the operating mode of the ESDRAMC. These modes are primarily used for the SDRAM initialization. 000 Normal read/write 001 PRECHARGE command 010 Auto-refresh command 011 LMR command 100 Manual self refresh 101 Through 111 are reserved
27	SP	Supervisor protect This control bit is used to restrict the user accesses within the chip select region. 0 User mode accesses are allowed to the chip select region 1 User mode accesses are prohibited
26–24	ROW	Row address width This control field specifies the number of row addresses used by the memory array. 000 11 row addresses 001 12 row addresses 010 13 row addresses 011 14 row addresses 100 Through 111 are reserved
23–22		Reserved
21–20	COL	Column address width This control field specifies the number of column addresses in the memory array and determines the break point in the address multiplexer. 00 8 column addresses 01 9 column addresses 10 10 column addresses 11 Reserved
19–18	—	Reserved

Table 2. ESDCTLx Register Fields (continued)

Bits	Name	Description
17–16	DSIZ	SDRAM memory data width This field defines the width of the SDRAM memory external data bus. Here, memories that are aligned to D[31:16] use DQM2 and DQM3 and memories that are aligned to D[15:0] use DQM0 and DQM1. 00 Reserved 01 16-bit memory width aligned to D[15:0] (reset value for CSD0) 10 Reserved (reset value for CSD1) 11 Reserved
15–13	SREFR	SDRAM refresh rate This control-bit field enables/disables the SDRAM refresh cycles and controls the refresh rate. The SDRAM refresh cycles are referenced with respect to a 32-kHz clock. As determined by this bit field, one, two, four, eight, or sixteen rows are refreshed at each rising edge. Multiple refresh cycles are separated by the row cycle delay that is specified in the SRC control field. Table 3 gives the settings to encode the SREFR bit field.
12	—	Reserved
11–10	PWDT	Power down timer This field determines if the SDRAM is placed in a power-down condition after a selectable delay from the previous access. Count based time-outs do not force the SDRAM to an idle condition (for example, any active banks that remain open). The power-down timer feature is disabled by the hardware reset. Table 4 gives the settings to encode the PWDT bit field.
9	—	Reserved
8	FP	Full page This bit should be set to 1 if the burst length of the SDRAM, which is connected to the CSD, is configured to the FP mode. The ESDCTL register terminates the accesses that are less than FP by inducing a BURST TERMINATE (BT) command. 0 Burst length of the external memory device is not set to full page 1 Burst length of the external memory device is set to full page
7	BL	Burst length This bit configures the access burst length. The ESDCTL burst length configuration should match the external SDRAM/LPDDR memory device (configured through a special operating mode, LMR) to ensure a proper operation. 0 External memory device which is connected to the CSD is configured to a burst length of 4 1 External memory device which is connected to the CSD is configured to a burst length of 8
6	—	Reserved
5–0	PRCT	Precharge timer This bit precharges a bank when 2xPRCT does not clock (HCLK, up to 133 MHz) any activity. Table 5 gives the settings to encode the PRCT bit field. Closing (due to PRECHARGE command) the most recently used/open row in an inactive bank within a chip select reduces the power consumption of the external-memory device. The PRCT is used when the PWDT is disabled (00) or set to any time no banks are active (01) and cannot be used with any other PWDT settings.

Table 3 gives the settings to encode the SREFR bit field.

Table 3. SREFR Bit Field Settings

SREFR[2:0]	Refresh Clocks for Each Row	Rows/64 ms @ 32 kHz	Row Rate @ 32 kHz (μs)
000	Refresh Disabled (bit field reset value)		
001	1	2048	31.25
010	2	4096	16.62
011	4	8192	7.81
100	8	16384	3.91
101	16	32768	1.95
110	Reserved		
111	Reserved		

Table 4 gives the settings to encode the PWDT bit field.

Table 4. PWDT Bit Field Settings

PWDT[1:0]	PWDT	Memory Device Operating Mode
00	Disabled (bit field reset value)	Run mode
01	No banks are active	Precharge power-down
10	64 clocks (HCLK) after completion of the previous access	Active power-down
11	128 clocks (HCLK) after completion of the previous access	Active power-down

Table 5 gives the settings to encode the PRCT bit field.

Table 5. PRCT Bit Field Settings

PRCT[5:0]	PRCT
000000	Disabled (bit field reset value)
000001	2 clocks to precharge
000010	4 clocks to precharge
000011	6 clocks to precharge
000100	8 clocks to precharge
000101	10 clocks to precharge
000110	12 clocks to precharge
000111	14 clocks to precharge
001000	16 clocks to precharge
—	—
010000	32 clocks to precharge

Table 5. PRCT Bit Field Settings

PRCT[5:0]	PRCT
—	—
100000	64 clocks to precharge
—	—
111111	126 clocks to precharge

- ESDCFGx—register contains the important time settings. Table 6 gives the description of the ESDCFGx register fields.

NOTE

See the *i.MX25 Multimedia Applications Processor Reference Manual* (IMX25RM) for more information about the ESDCFGx register.

Table 6. ESDCFGx Register Options

Bits	Name	Description
31–23	—	Reserved
22–21	t_{XP}	LPDDR exit power down to the immediate valid command delay This control field determines the minimum delay between an issued valid command and the LPDDR after exiting from the power-down mode. The t_{XP} value gives the number of clocks that should be inserted after exiting the power-down mode and the subsequent new valid command. 00 1 clock delay 01 2 clock delay 10 3 clock delay 11 4 clock delay
20	t_{WTR}	LPDDR WRITE to READ command delay Data for any write burst is generally followed by a subsequent READ command. The LPDDR controller automatically induces t_{WTR} number of idle cycles between the WRITE and READ commands. The t_{WTR} should be configured according to the LPDDR device type that is used and is referenced from the first positive clock edge after the last data-in pair. 0 1 clock 1 2 clocks
19–18	t_{RP}	SDRAM row precharge delay This control bit determines the number of idle clocks that should be inserted between a PRECHARGE command and the immediate row-activate command of the same bank. Hardware reset initializes the controller to insert 3 clocks. A subsequent command to the same bank cannot be issued after the PRECHARGE command until the t_{RP} condition is met. 00 1 clock 01 2 clocks 10 3 clocks 11 4 clocks
17–16	t_{MRD}	SDRAM LMR to ACTIVE command This control bit determines the minimum number of idle clocks that should be inserted between LMR and ACTIVE commands. Hardware reset initializes the controller to insert 2 clocks. 00 1 clock 01 2 clocks 10 3 clocks 11 4 clocks

Table 6. ESDCFGx Register Options (continued)

Bits	Name	Description
15	t_{WR}	SDRAM WRITE to PRECHARGE command Data for a fixed length write burst is generally followed by or truncated with a PRECHARGE command of the same bank (provided that the auto-PRECHARGE command is not activated). Also, data for a full-page write burst is truncated with a PRECHARGE command of the same bank. These clock values are applicable to the SDRAM and LPDDR memory devices. 0 1 clock 1 2 clocks
14–12	t_{RAS}	SDRAM ACTIVE to PRECHARGE command These control bits determine the minimum number of clocks that are required between the ACTIVE and PRECHARGE commands in the same bank. Hardware reset initializes the controller to insert 6 clocks. 000 1 clock 001 2 clocks 010 3 clocks 011 4 clocks 100 5 clocks 101 6 clocks 110 7 clocks 111 8 clocks
11–10	t_{RRD}	Bank A ACTIVE to bank B ACTIVE command This field determines the number of idle clocks that should be inserted between the consecutive ACTIVE commands in different banks. A subsequent ACTIVE command to a different row in the same bank can be issued only after the previously active row has been closed (precharged). This can be performed while the first bank is accessed, which results in the reduction of the total row-access overhead. 00 1 clock 01 2 clocks 10 3 clocks 11 4 clocks
9–8	t_{CAS}	SDRAM CAS latency This field determines the latency between the READ commands and the availability of data on the bus. This field does not affect the second and subsequent data words in a burst and has no effect on the write cycles. The CAS latency is initialized to 3 clocks following a hardware reset. 00 Reserved 01 Reserved2 10 2 clocks (SDR and LPDDR SDRAM CAS latency) 11 3 clocks (SDR and LPDDR SDRAM CAS latency2)
7	—	Reserved

Table 6. ESDCFGx Register Options (continued)

Bits	Name	Description
6–4	t_{RCD}	SDRAM row to column delay This field determines the number of clocks that should be inserted between a row-activate command and the subsequent READ or WRITE command of the same bank. The hardware reset initializes the delay to 3 clocks. 000 1 clock 001 2 clocks 010 3 clocks 011 4 clocks 100 5 clocks 101 6 clocks 110 7 clocks 111 8 clocks
3–0	t_{RC}	SDRAM row cycle delay This control field determines the minimum delay between a refresh and the subsequent refresh or read/write access. This delay corresponds to the minimum row-cycle time that is captured in the t_{RC}/t_{RFC} memory timing specification. 0000 20 clocks 0001 2 clocks 0010 3 clocks 0011 4 clocks 0100 5 clocks 0101 6 clocks 0110 7 clocks 0111 8 clocks 1000 9 clocks 1001 10 clocks 1010 11 clocks 1011 12 clocks 1100 13 clocks 1101 14 clocks 1110 14 clocks 1111 16 clocks

- Enhanced SRAM miscellaneous register (ESDMISC)—configures various memory and control settings for the ESDRAMC register. Table 6 gives the description of the ESDMISC register fields.

NOTE

See the *i.MX25 Multimedia Applications Processor Reference Manual* (IMX25RM) for more information about the ESDRAMC register.

Table 7. ESDRAMC Register Options

Bits	Name	Description
31	SDRAM_RDY	External SDRAM/LPDDR device status This is a read-only status bit that indicates the status of the external memory devices. 0 SDRAM/LPDDR external device is not ready for use (reset value) 1 SDRAM/MMDR external device is ready for use
30–10	—	Reserved

Table 7. ESDRAMC Register Options (continued)

Bits	Name	Description
9	DDR2_EN	Regular (non-mobile) DDR2 device status This bit is common for both the chip selects. 0 DDR2 device is not used (reset value) 1 DDR2 device is used
8	DDR_EN	Regular (non-mobile) device status This bit is common for both the chip selects. 0 DDR1/DDR2 device is not used (reset value) 1 Non-mobile DDR device is used (DDR2 or DDR1)
7	FRC_MSR	Force measurement When this bit is set, the measurement unit starts a new measurement until this bit is cleared.
6	MA10_SHARE	MA10 share This bit should be enabled when the MA10 address line is shared with the other memory-controller address line. When this bit is enabled, the ESDRAMC requests for the address line from the M3IF before issuing the precharge-all command (during auto-refresh cycles). 0 MA10 share is disabled 1 MA10 share is enabled
5	LHD	Latency hiding disable This bit disables the command anticipation (latency hiding) mechanism. 0 Latency hiding is enabled 1 Latency hiding is disabled
4	MDDR_MDIS	LPDDR delay line measure disable This read/write bit disables the delay-line measure unit (when the bit is set). After reset, this bit is cleared and enables the delay-line measure unit. The measure time period is estimated to be around 2000 clock cycles of the AHB HCLK. 0 LPDDR delay-line measure unit is enabled 1 LPDDR delay-line measure unit is disabled
3	MDDR_DL_RST	LPDDR delay line soft reset This write only bit resets the delay-line unit (when this bit is set). The delay-unit automatically (if LPDDR_MDIS is cleared) starts a new measurement after the reset is disabled. 0 LPDDR delay line is not reset 1 LPDDR delay line is reset
2	MDDR_EN	Enables the DDR SDRAM device. 0 SDR SDRAM is used 1 DDR SDRAM is used (either mobile or non-mobile)
1	RST	Software initiated local module reset This bit generates the local module reset for the ESDRAMC. When the RST bit is set, a one-cycle reset pulse is send to the controller. 0 Soft reset is disabled 1 Soft reset is initiated
0	—	Reserved

2 BSP SDRAM Dependent Files

The files that are modified in a BSP when SDRAM is required to be changed are as follows:

- `Oemaddrtab_cfg.inc`—contains the OEM address table definition. This table maps the 4-GB physical address space to the 512-MB unmapped space in the kernel.
- `image_cfg.inc`—contains the memory map addresses that are based on images. This file is used only in the low-level `*.s` files.
- `image_cfg.h`—contains the base address that is used in images. This file is used in the `*.c` files.
- `xldr_sdram_init.inc`—contains the low-level code that configures the ESDRAMC.
- `eboot.bib`—contains the bootloader-memory layout and is used by the platform builder in the conversion process of the bootloader to an executable binary file (`.bin` and `.nbo`). This files is not required to be changed in the i.MX25 BSP. This is because all the memory sections that are defined in the BSP are set on the first part of the memory. However, there are BSPs that set the bootloader memory sections at the end of the memory and it is on this BSP that the file should be changed when the total RAM size changes.
- `config.bib`—used by the platform builder to create the OS-binary image. This file contains two sections—MEMORY and CONFIG. The MEMORY section defines the memory table for the run-time image.

2.1 BSP File Modification

This section describes the changes in certain files when the memory in the i.MX25 product development kit (PDK) is required to be changed.

NOTE

The described changes are based on the files in the software development kit (SDK).

2.1.1 xldr_sdram_init.inc

The `xldr_sdram_init.inc` file sets the configuration for the ESDCTLx, ESDCFGx, and ESDMISC registers and should be modified whenever the SDRAM AC parameters changes. Only the sections that set the configuration registers are required to be modified. This section is commented as to be modified in the `xldr_sdram_init.inc` file fragment, which is as follows:

```
; Configure for DDR2
        ldr     r0, =0x24C                                          ; to be modified
        str     r0, [r1, #ESDRAMC_ESDMISC_OFFSET]


        ;---------------------------------------
        ; Configure DDR2 memory on CSD0
        ;---------------------------------------
        ldr     r2, =CSP_BASE_MEM_PA_CSD0

        ; Configure timing parameters
        ldr     r0, =0x0076E83F                                     ; to be modified
        str     r0, [r1, #ESDRAMC_ESDCFG0_OFFSET]
```

```
; Set precharge command
;
;   DSIZ - 16-bit align to D[15:0] (1 << 16)        = 0x00010000
;   COL - 10 column addresses (2 << 20)             = 0x00200000
;   ROW - 13 Row addresses (2 << 24)                = 0x02000000
;   SP - User mode access (0 << 27)                 = 0x00000000
;   SMODE - Precharge command (1 << 28)             = 0x10000000
;   SDE - Enable controller (1 << 31)               = 0x80000000
;                                                   ------------
;                                                     0x92210000
ldr     r0, =0x92210000                                     ; to be modified
str     r0, [r1, #ESDRAMC_ESDCTL0_OFFSET]

; Access SDRAM with A10 high to precharge all banks
ldr     r0, =0x0
strb    r0, [r2, #0x400]


; Set load mode command
;
;   DSIZ - 16-bit align to D[15:0] (1 << 16)        = 0x00010000
;   COL - 10 column addresses (2 << 20)             = 0x00200000
;   ROW - 13 Row addresses (2 << 24)                = 0x02000000
;   SP - User mode access (0 << 27)                 = 0x00000000
;   SMODE - Load mode command (3 << 28)             = 0x30000000
;   SDE - Enable controller (1 << 31)               = 0x80000000
;                                                   ------------
;                                                     0xB2210000
ldr     r0, =0xB2210000                                     ; to be modified
str     r0, [r1, #ESDRAMC_ESDCTL0_OFFSET]

; DDR2 EMR2
ldr     r0, =0x0
ldr     r3, =0x82000000
strb    r0, [r3]

; DDR2 EMR3
ldr     r0, =0x0
ldr     r3, =0x83000000
strb    r0, [r3]

; DDR2 EMR1: enable DLL, disable /DQS
ldr     r0, =0x0
ldr     r3, =0x81000400
strb    r0, [r3]

; DDR2 MR: reset DLL, BL=8, CL=3
ldr     r0, =0x0
strb    r0, [r2, #0x333]

; Set precharge command
;
;   DSIZ - 16-bit align to D[15:0] (1 << 16)        = 0x00010000
;   COL - 10 column addresses (2 << 20)             = 0x00200000
;   ROW - 13 Row addresses (2 << 24)                = 0x02000000
;   SP - User mode access (0 << 27)                 = 0x00000000
;   SMODE - Precharge command (1 << 28)             = 0x10000000
```

```
        ;   SDE - Enable controller (1 << 31)               = 0x80000000
        ;                                                   ------------
        ;                                                     0x92210000
        ldr     r0, =0x92210000                                     ; to be modified
        str     r0, [r1, #ESDRAMC_ESDCTL0_OFFSET]

        ; Access SDRAM with A10 high to precharge all banks
        ldr     r0, =0x0
        strb    r0, [r2, #0x400]

        ; Set autorefresh command
        ;
        ;   DSIZ - 16-bit align to D[15:0] (1 << 16)        = 0x00010000
        ;   COL - 10 column addresses (2 << 20)             = 0x00200000
        ;   ROW - 13 Row addresses (2 << 24)                = 0x02000000
        ;   SP - User mode access (0 << 27)                 = 0x00000000
        ;   SMODE - Autorefresh command (2 << 28)           = 0x20000000
        ;   SDE - Enable controller (1 << 31)               = 0x80000000
        ;                                                   ------------
        ;                                                     0xA2210000
        ldr     r0, =0xA2210000                                     ; to be modified
        str     r0, [r1, #ESDRAMC_ESDCTL0_OFFSET]

        ; Use writes to refresh all banks of SDRAM
        ldr     r0, =0x0
        strb    r0, [r2]
        strb    r0, [r2]

        ; Set load mode command
        ;
        ;   DSIZ - 16-bit align to D[15:0] (1 << 16)        = 0x00010000
        ;   COL - 10 column addresses (2 << 20)             = 0x00200000
        ;   ROW - 13 Row addresses (2 << 24)                = 0x02000000
        ;   SP - User mode access (0 << 27)                 = 0x00000000
        ;   SMODE - Load mode command (3 << 28)             = 0x30000000
        ;   SDE - Enable controller (1 << 31)               = 0x80000000
        ;                                                   ------------
        ;                                                     0xB2210000
        ldr     r0, =0xB2210000                                     ; to be modified
        str     r0, [r1, #ESDRAMC_ESDCTL0_OFFSET]

        ; DDR2 MR: end DLL reset, BL=8, CL=3
        ldr     r0, =0x0
        strb    r0, [r2, #0x233]

        ; Hold for more than 200 cycles
        ldr     r0, =0x100
hold
        subs    r0, r0, #1
        bne     hold

        ; DDR2 EMR1: OCD calibration default
        ldr     r0, =0x0
        ldr     r3, =0x81000780
        strb    r0, [r3]

        ; DDR2 EMR1: OCD calibration exit, enable DLL, disable /DQS
```

```
        ldr     r0, =0x0
        ldr     r3, =0x81000400
        strb    r0, [r3]

        ; Set normal mode command
        ;
        ;   PRCT - Precharge timer disabled (0 << 5)        = 0x00000000
        ;   BL - Burst of 8 for SDR/DDR (1 << 7)            = 0x00000080
        ;   FP - No full page mode (0 << 8)                 = 0x00000000
        ;   PWDT - Power down timeout disabled (3 << 10)    = 0x00000000
        ;   SREFR - 4 rows refreshed each clock (3 << 13)   = 0x00006000
        ;   DSIZ - 16-bit align to D[15:0] (1 << 16)        = 0x00010000
        ;   COL - 10 column addresses (2 << 20)             = 0x00200000
        ;   ROW - 13 Row addresses (2 << 24)                = 0x02000000
        ;   SP - User mode access (0 << 27)                 = 0x00000000
        ;   SMODE - Normal mode command (0 << 28)           = 0x00000000
        ;   SDE - Enable controller (1 << 31)               = 0x80000000
        ;                                                   ------------
        ;                                                     0x82216080
        ldr     r0, =0x82216080                                     ; to be modified
        str     r0, [r1, #ESDRAMC_ESDCTL0_OFFSET]
```

2.1.2 config.bib

The `config.bib` file is required to be changed when the SDRAM size changes. Only the section that sets the total RAM, which is available for the OS, should be modified. This section is commented as to be modified in the `config.bib` file fragment, which is as follows:

```
;***************************** MEMORY SECTION *****************************

MEMORY

; --------------------------- RAM image --------------------------------

;   Start Addr      End Addr        Mem Type    Region Name     Size

;   0x80000000      0x80100000      SDRAM       reserved         1 MB

;   0x80100000      0x81100000      SDRAM       NK              16 MB

;   0x81100000      0x84000000      SDRAM       RAM             47 MB

; ----------------------------------------------------------------------

;                   Name            Address     Size        Type

                    BOOT_AND_OTHER  80000000    00100000    RESERVED

                    NK              80100000    01000000    RAMIMAGE

                    RAM             81100000    02F00000    RAM         ; to be modified

IF IMGFLASH
        ; no support for NOR flash available
ENDIF
```

2.1.3 Image_cfg.h

The `Image_cfg.h` file is required to be changed when the SDRAM size changes. Only the section that sets the total available RAM should be modified. This section is commented as to be modified in the `Image_cfg.h` file fragment, which is as follows:

```
//------------------------------------------------------------------------------
// RAM image defines
#define IMAGE_BOOT_RAMDEV_RAM_PA_START      IMAGE_BOOT_RAM_PA_START
#define IMAGE_BOOT_RAMDEV_RAM_SIZE          (64*1024*1024)             // to be modified
#define IMAGE_BOOT_RAMDEV_RAM_PA_END
(IMAGE_BOOT_RAMDEV_RAM_PA_START+IMAGE_BOOT_RAMDEV_RAM_SIZE-1)

// Share args
#define IMAGE_SHARE_ARGS_RAM_OFFSET         0
#define IMAGE_SHARE_ARGS_RAM_PA_START
(IMAGE_BOOT_RAMDEV_RAM_PA_START+IMAGE_SHARE_ARGS_RAM_OFFSET)
#define IMAGE_SHARE_ARGS_UA_START           OALPAtoVA(IMAGE_SHARE_ARGS_RAM_PA_START, FALSE)
#define IMAGE_SHARE_ARGS_RAM_SIZE           (4*1024)
```

2.1.4 image_cfg.inc

The `image_cfg.inc` file is required to be changed when the SDRAM size changes. Only the section that sets the total available RAM should be modified. This section is commented as to be modified in the `image_cfg.inc` file fragment, which is as follows:

```
;;------------------------------------------------------------------------------
;; RAM image defines
IMAGE_BOOT_RAMDEV_RAM_PA_START      EQU     CSP_BASE_MEM_PA_CSD0  ;; 64 MB RAM CSD0
IMAGE_BOOT_RAMDEV_RAM_UA_START      EQU     (0xA0000000)
IMAGE_BOOT_RAMDEV_RAM_CA_START      EQU     (0x80000000)
IMAGE_BOOT_RAMDEV_RAM_SIZE          EQU     (64*1024*1024)             ;; to be modified
IMAGE_BOOT_RAMDEV_RAM_PA_END        EQU
(IMAGE_BOOT_RAMDEV_RAM_PA_START+IMAGE_BOOT_RAMDEV_RAM_SIZE-1)
```

2.1.5 Oemaddrtab_cfg.inc

The `Oemaddrtab_cfg.inc` file is required to be changed when the SDRAM size changes. Only the section that sets the mapping of the RAM memory space should be modified. This section is commented as to be modified in the `Oemaddrtab_cfg.inc` file fragment, which is as follows:

```
;-------------------------------------------------------------------------------
;
; TABLE FORMAT
;       cached address, physical address, size
;-------------------------------------------------------------------------------

g_oalAddressTable

        DCD 0x80000000, CSP_BASE_MEM_PA_CSD0, 64    ; RAM image mapping       to be modified
        DCD 0x91300000, CSP_BASE_REG_PA_NANDFC, 36          ; NANDMA + NANDSA + NANDFC
        ; we keep a gap of 36 MB because of the logical addressing of the NAND binaries
        DCD 0x93700000, CSP_BASE_MEM_PA_IRAM,  64           ; Internal RAM
        ; we keep a gap of 64MB because of the logical addressing of the SD/MMC binaries
        DCD 0x97700000, CSP_BASE_REG_PA_AIPS1, 1
```

```
        DCD 0x97800000, CSP_BASE_REG_PA_AIPS2, 1
        DCD 0x97900000, CSP_BASE_REG_PA_AVIC,  1
        DCD 0x97a00000, CSP_BASE_REG_PA_PERIPH_REGS1,  1    ; some peripheral regs (such as FEC)
        DCD 0x97b00000, CSP_BASE_MEM_PA_SPI, 1               ;SPI FLASH
        DCD 0x97c00000, CSP_BASE_MEM_PA_CSD1, 4
        ; we keep a gap of 4MB because of the logical addressing of the SPI and I2C binaries
        DCD 0x00000000, 0x00000000, 0                        ; Terminate table


;-------------------------------------------------------------------------------

END
```

3 Revision History

Table 8 provides a revision history for this application note.

Table 8. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	09/2010	Initial release.

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: AN4200
Rev. 0
09/2010