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Application Note

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Key Architectural Differences Between the i.MX233 and i.MX25

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This application note provides a comparison of the key architectural differences between the i.MX233 and i.MX25, Freescale's ARM®-based 32-bit application processors. This document provides a quick overview of various aspects of these processors including the core, security, peripherals, and connectivity. Each section contains a table that compares the features of the two processors. If the two processors have a similar or identical feature, the row for that feature is green. If the feature is somewhat different, the row is yellow. If the feature is very different, the row is red. If a feature is only available for one of the processor, the cell having the feature is grey and the other cell on that row is not shaded.

The i.MX233 is a system on chip (SoC) designed for applications such as portable media players, portable navigation devices and various other handheld multimedia devices that require low power, high performance and integration, and quality audio and video playback. The 90 nm SoC is based on the ARM926EJ-S™ core coupled with on-chip audio and power management functions. This highly-integrated SoC eliminates over ten previously-discrete ICs typically found on portable navigation devices. Unlike other ICs based on an ARM9™ core, the i.MX233 integrates the analog functions on the

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same silicon die as the processor. Refer to the i.MX233 device documentation for more information.

The i.MX25 family of multimedia applications processors includes several key features that allow users to reduce their overall system bill of materials cost such as DDR2 support, two embedded USB PHYs, 3.3 V I/O support, general purpose 12-bit ADCs and a touch screen controller. In addition, the i.MX25 continues to make the industrial and general embedded market a key focus with the integration of 10/100 ethernet MAC, SDIO connectivity, up to SVGA (800×600) resolution TFT LCD support, camera sensor interface, and 400 MHz CPU speed grade. Improving on the strength of previous i.MX platforms, the i.MX25 processor provides additional tamper detection security that monitors and helps prevent against system integrity attacks from hackers, making it the right choice for any type of secure device, whether it is a wired or wireless payment terminal (POS), or any other type of product needing secure system boot and tamper detection. The i.MX25 also complements the i.MX ARM11™ portfolio by maintaining a large share of peripheral commonality with the i.MX35 multimedia applications processor family. Refer to the i.MX25 device documentation for more detailed information.

1 System Core

At the core of both the i.MX233 and i.MX25 is Freescale's fast, proven, power-efficient implementation of the ARM926EJ-S™ core (Figure 1). Both processors include a stand-alone ARM CoreSight Embedded Trace Marcocell, ETM9CSSingle, that provides instruction and data trace for the ARM9 microprocessor.

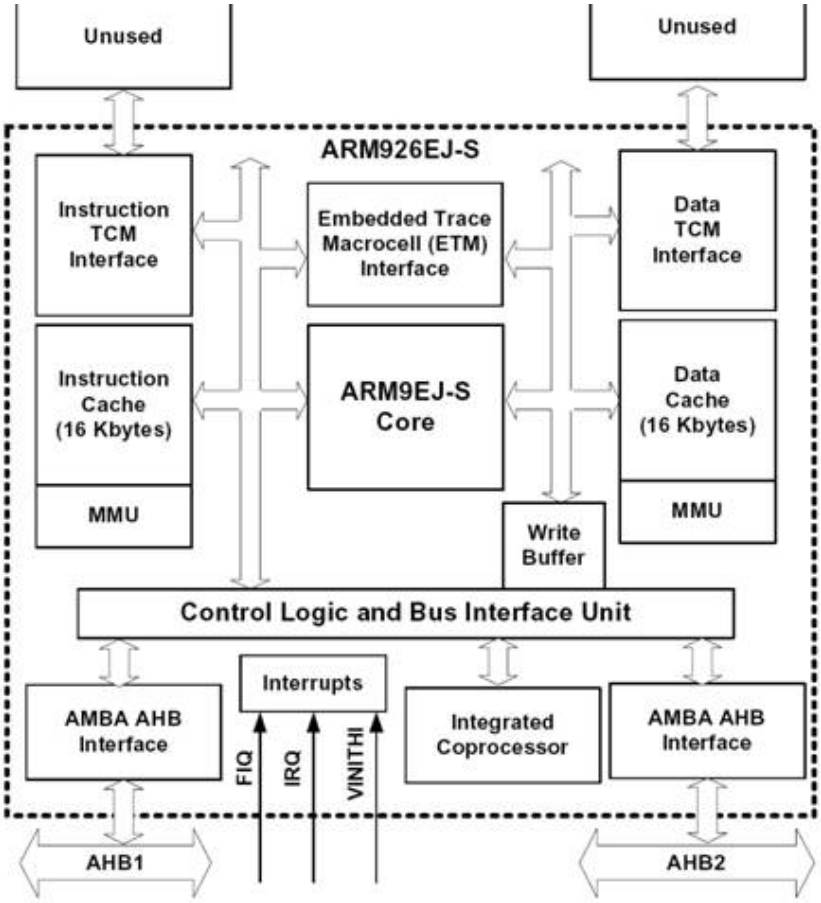


Figure 1. ARM926 RISC Processor Core

Table 1 shows a comparison of the system core features for the i.MX233 and i.MX25.

Table 1. System Core Comparison

Feature	i.MX233	i.MX25
MCU Core	ARM926EJ-S, 454 MHz	ARM926EJ-S, 400 MHz
Caches	16 Kbyte data + 16 Kbyte instruction	16 Kbyte data + 16 Kbyte instruction
On-chip RAM	32 Kbyte	128 Kbyte
On-chip ROM	64 Kbyte	32 Kbyte
On-chip Secure RAM	N/A	2 Kbyte
OC One-Time-Programmable	1 Kbit OCOTP	IC Identification Module (IIM)
Embedded Trace Macrocell (ETM)	Yes	Yes
JTAG Interface	1-wire serial/6-wire parallel	Secure JTAG (parallel only)

1.1 i.MX233 System Core

The i.MX233 can run up to 454 MHz. The i.MX233 includes a 16 Kbyte data cache, a 16 Kbyte instruction cache, 32 Kbyte of on-chip RAM as well as 64 Kbyte of on-chip ROM. The i.MX233 includes a serial JTAG module that maps one-wire protocol to six-wire JTAG interface. The HW_DIGCTL_USE_SERIAL_JTAG bit in the digital control block selects whether serial or parallel JTAG is used. The default configuration is set by the USE_PARALLEL_JTAG bit in the HW_OCOTP_ROM0 shadow register and it is loaded by the ROM code on boot up. If the bit is not blown, serial JTAG is used by default.

The i.MX233 includes 1 Kbits of On-Chip One-Time-Programmable (OCOTP) ROM for storing hardware and software capability bits, various ROM configuration bits, and Freescale operations and unique-ID fields. The OCOTP ROM can also be used for storing a customer-programmable cryptography key. There are four words of storage for general use. In addition, a 32-bit word is dedicated to control the read and write locking of various OTP regions which are copied to a shadow register.

1.2 i.MX25 System Core

The i.MX25 can run up to 400 MHz. The i.MX25 includes a 16 Kbyte data cache and a 16 Kbyte instruction cache. The i.MX25 also includes 128 Kbyte of on-chip RAM, 32 Kbyte of on-chip ROM, and 2 Kbyte of on-chip secure RAM for storage of sensitive information. The i.MX25 includes a secure JTAG port which protects the debug port from attack by regulating or blocking access to the system debug features.

The i.MX25 includes an IC Identification Module (IIM) which provides the primary user-visible mechanism for interfacing with on-chip fuse elements. The fuses are used for unique device identifiers, mask version numbers, cryptographic keys and various control signals that require permanent non-volatility. The IIM can also provide up to 28 volatile control signals and can generate a second 168-bit SCC key.

2 Security Features

Table 2 shows a comparison of the security features for the i.MX233 and i.MX25.

Table 2. Security Features Comparison

Feature	i.MX233	i.MX25
Security Hardware	Data Co-Processor: • AES • Hashing	RTICv3 SCCv3 DryIce RNGB
Secure ROM	OCOTP ROM	IC Identification Module (IIM)
Secure RAM	N/A	2 Kbyte
Secure JTAG	N/A	Yes
Secure Boot	128-bit AES H/W decryption	HAB with SHA-256

2.1 i.MX233 Data Co-Processor (DCP)

The i.MX233 DCP module provides support for general encryption and hashing functions typically used for security functions. The following sections discuss the blocks of the i.MX233 DCP.

2.1.1 Advanced Encryption Standard (AES)

The AES block of the i.MX233 DCP implements a 128-bit key/data encryption/decryption block as defined by the National Institute of Standards and Technology (NIST) as US FIPS PUB 197 (see http://csrc.nist.gov/publications/PubsFIPS.html for more information).

The DCP implements four SRAM-based keys that can be used by software to securely store keys on a semi-permanent basis. Keys are written using the programmed I/O (PIO) interface by specifying a key index to indicate which key to load and a subword pointer to indicate which word to write within the key. After a subword is written, the subword pointer is automatically incremented so that the higher-order words of the key can be programmed without rewriting the key index. The keys written to the storage are not readable.

After a system reset, the OTP controller reads the e-fuse devices, provides OTP key information over a parallel 128-bit interface and captures the key into the key RAM.

The DCP supports two forms of encryption. The most basic form is Electronic Code Book (ECB) mode where the output is only a function of the key and the plaintext. The other form, Cipher Block Chaining (CBC) mode, can be implemented around ECB to provide addition security. CBC takes the previously encrypted data and logically XORs it with the next incoming plaintext before performing the encryption. During decryption, the process is reversed and the previously encrypted data is XORed with the decrypted ECB data to provide the plaintext.

2.1.2 Hashing

The hashing module on the i.MX233 DCP implements the SHA-1 hashing algorithm and a modified CRC-32 checksum algorithm. These algorithms produce a signature for a block of data that can be used to determine whether the data is intact.

The CRC-32 algorithm implements a 32-bit CRC algorithm similar to the one used by Ethernet and many other protocols. The SHA-1 block implements a 160-bit hashing algorithm that operates on 512-bit (64-byte) blocks as defined by US FIPS PUB 180-1 (see http://csrc.nist.gov/publications/PubsFIPS.html for more information). The module can be used to generate a unique signature for a block of data to validate the integrity of the data by comparing the resulting digest with the original digest.

2.2 i.MX233 Secure Boot

The i.MX233 contains a secure boot loader in the ROM code to support a secure boot. The ARM core jumps to the on-chip ROM at reset. There is no method to jump to user code directly. The boot loader allows the system to boot from various interfaces such as USB, NAND, SD/MMC, I^2C or SPI. The secure boot images are encrypted using a randomly selected session key from a Freescale-supplied `elftosb` application. The session key is encrypted by the OTP key and determined by the ROM during the authentication process. The boot loader authenticates and decrypts the boot image on reset. A proprietary authentication scheme (not HAB) based on a CDC-MAC signature calculated using the DCP and OTP key is used by the boot loader to authenticate the boot images. Only authenticated images are booted by the boot loader. Non-secure boot is also supported, but it can only be enabled through the OTP bits.

2.3 i.MX25 Security Hardware

The i.MX25 processor has a number of hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, robust tamper detection secure boot, and secure software downloads.

The Runtime Integrity Checker (RTICv3) and HASH accelerator include SHA-1 and SHA-256 message authentication to ensure the integrity of the peripheral memory contents. The RTICv3 is used to assist the boot authentication process by verifying the memory contents during system boot. The RTICv3 can also verify the memory contents during run-time execution.

The Secure RAM module (SSCv3) and the Security Monitor provide secure storage of sensitive information on both on-chip RAM and off-chip non-volatile memory. When used with on-chip memory, the data stored in RAM can be cleared, if necessary, to prevent unauthorized access. When used with off-chip memory, the data is stored in an encrypted form using an encryption key that is unique to each device and accessible only to the Secure RAM module.

The DryIce module provides volatile storage of encryption keys with robust tamper detection and secure key erase for Point Of Sale (POS) terminals. The DryIce module also provides a trusted time source for DRM schemes. The trusted time source consists of a 47-bit secure time counter running from a 32.768 kHz clock source and a 32-bit monotonic counter. The DryIce module is powered by both the SoC power supply and a backup power source to maintain the secure counter and key storage in the event of power loss.

The i.MX25 has a hardware random number generator (RNGB) for generating true random numbers.

2.4 i.MX25 High Assurance Boot (HAB)

The secure boot of i.MX25, shown in Figure 2, is supported by the HAB with SHA-256. The HAB component of the ROM protects against the potential threat of attackers modifying areas of code or data in programmable memory. The HAB also prevents attempts to gain access to features which should not be available.

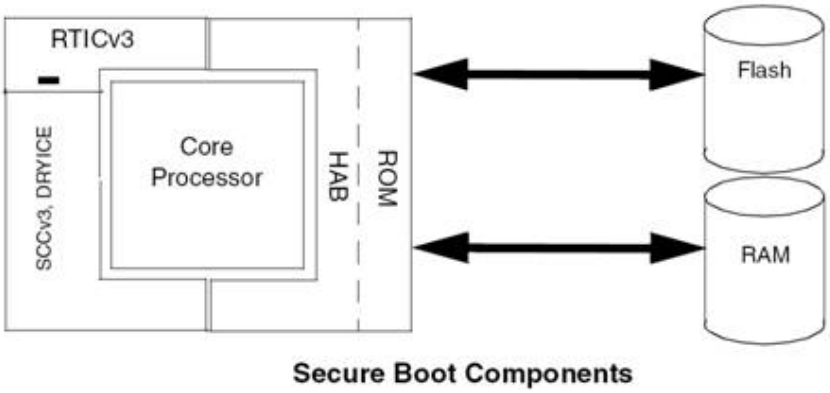


Figure 2. i.MX25 Secure Boot Components

3 External Memory and Storage

Both the i.MX233 and i.MX25 can efficiently interface with many different external memories and storage devices such as Flash memory, Secure Digital (SD) and Compact Flash (CF). Table 3 shows a comparison of the external memory and storage features for the i.MX233 and i.MX25.

Table 3. External Memory and Storage Comparison

Feature	i.MX233	i.MX25
Memory and Storage Hardware Interface	External Memory Interface (EMI) General Purpose Media Interface (GPMI) • NAND Flash Synchronous Serial Port (SSP)	External Memory Interface (EMI) • Multi-Master Memory Interface (M3IF) • Enhanced SD RAM Ctrl (ESDRAMC) • NAND Flash Controller (NFC) • Wireless External Interface Module (WEIM) Advanced Technology Attachment (ATA) Enhanced SD Host Interface (eSDHC)
SDRAM	2.5 V DDR1 1.8 V Mobile DDR	3.3 V SDRAM 1.8 V DDR2 1.8 V Mobile DDR
NAND Flash	Up to four 8-bit/16-bit NAND SLC/MLC NAND 8-bit Reed Solomon ECC 20-bit BCH ECC	Up to four 8-bit/16-bit NAND SLC/MLC NAND 8-bit Reed Solomon ECC Internal RAM Buffer
NOR Flash	N/A	Yes
ATA	N/A	UDMA-5
SD/CF/MMC	Yes	Yes

3.1 i.MX233 Memory Interface

The i.MX233 supports off-chip DRAM storage using the External Memory Interface (EMI) controller. The EMI consists of two major components: the DRAM controller and the Delay Compensation Circuitry (DCC). The EMI supports 2.5 V DDR1 and 1.8 V Mobile DDR.

The DRAM controller supports up to two external chip-selects and a maximum of 128 Mbytes of DRAM storage. The 128-pin LQFP has one chip select and supports a maximum of 64 Mbytes of DRAM. The 169-pin BGA has two chip selects and supports a maximum of 128 Mbytes of DRAM. Programmable registers within the DRAM controller allow flexibility for device timings, low-power operation, and performance tuning.

The i.MX233 General-Purpose Media Interface (GPMI) is a flexible interface that supports up to four NAND Flash devices. The NAND Flash mode has configurable address and command behavior, providing support for future devices.

The GPMI has several features to efficiently support NAND Flash:

- Individual chip select and ready/busy pins for four NAND Flashes
- Individual state machine and DMA channel for each chip select
- Special command modes that work with the DMA controller to perform all normal NAND Flash functions without CPU intervention
- Configurable timing based on a dedicated clock that allows optimal balance of high NAND Flash performance and low system power

The i.MX233 has hardware Error Correction Code (ECC) accelerators to provide forward error correction for interfacing to MLC NAND Flashes. The ECC engine on the i.MX233 implements Bose Ray-Choudhury Hocquenghem (BCH-ECC) to provide up to 20 bits of correction. For backwards-compatibility, there is also an Reed Solomon (RS-ECC8) engine which only provides 4 or 8 bits of correction. Both engines are tightly coupled to the GPMI and are for mutually exclusive use with completely separate programming modules and DMA structures.

External media such as SD, MMC, or CF are also supported by the i.MX233 Synchronous Serial Ports (SSP). To support SD, SDIO, MMC, and high-speed (4-bit and 8-bit) MMC cards, the SSP is configured in SD/SDIO/MMC mode. In this mode, the SSP supports simultaneous command and data transfers. Commands are sent to the card and responses are returned to the host on the CMD line. Register data is sent as a command response on the CMD line. Block data read from or written to the card Flash is transferred on the DAT line(s). The SSP also supports the SDIO IRQ.

3.2 i.MX25 Memory Interfaces

The i.MX25 EMI handles all the external memory accesses. The EMI manages the following external memory controllers to support different memory devices:

- Multi Master Memory Interface (M3IF)
- Enhanced SDRAM/LPDDR memory controller (ESDRAMC/MDDRC)
- NAND Flash memory controller (NFC)
- SRAM/PSRAM/ Flash memory controller (WEIM)

The M3IF is capable of supporting multiple requests from up to eight masters through input ports interface. The M3IF supports memory snooping, such as monitoring a region (from two Kbyte to 16 Mbytes) in external memory for write accesses. Some versions of the M3IF also support memory watermark protection for up to eight different chip selects for hardware-preselected masters.

The ESDRAMC/MDDRC provides interface and control for synchronous SDR, LPDDR and DDR1 devices. It also provides support for 4-bank DDR2 devices, and can connect to 8-bank DDR2 devices (though it can only access 4-banks with no ODT control signal). The controller supports 64-Mbit 128-Mbit, 256-Mbit, 512-Mbit, and 1-Gbit (4 banks) synchronous DRAM with two independent chip selects and with up to 128 Mbytes addressable memory per chip select. Only 16-bit SDRAM is supported by the controller. The controller has a PC133 compliant interface that supports SDR at 133 MHz and DDR at 266 MHz, with JEDEC standard pin-out and operations (see http://www.jedec.org/ for more information). Consecutive memory accesses are optimized through memory command anticipation or latency hiding. The controller also has a built-in auto-refresh timer and state machine with self-refresh entry and exit support to keep the data in the SDRAM valid during system reset and low power modes.

The NFC provides a glueless interface to both 8-bit and 16-bit NAND Flash with page sizes of 512 bytes, 2 Kbytes or 4 Kbytes. The NFC has an internal RAM buffer (4 Kbytes + 512 bytes) which can be configured as Boot RAM or operated as a buffer during normal operation. The NFC supports both SLC and MLC NAND Flashes. MLC NAND Flash is supported using two Reed Solomon RS(511,503) error correction codes which correct 4/8 error bits in 528/538 bytes (512 bytes main + 16/26 bytes spare). The i.MX25 includes an internal bootcode loader to provide advanced data protection during power-up when booting from external NAND Flash.

The WEIM interfaces to external devices and includes generation of chip selects, clocks and control for external peripherals and memory. The WEIM provides asynchronous and synchronous access to 16-bit or 32-bit devices with SRAM-like interfaces. The WEIM has six chip selects for external devices with selectable protection for each chip select. The WEIM includes a programmable data port size wait-state generator for each chip select. The WEIM supports asynchronous accesses with programmable setup and hold times for control signals. For synchronous accesses, the WEIM supports burst read mode for AMD, Intel, and Micron burst Flash memories and burst write mode for PSRAM (CellularRAMTM from Micron, Infineon, Cypress). The WEIM also supports multiplexed address/data bus operation, external cycle termination/postpone with DTACK signal and Big/Little-endian modes of operation per access.

4 Audio Features

The i.MX233 includes both digital and analog audio interfaces, including a serial audio interface (SAIF), a Sony-Philips Digital Interface Format (SPDIF) transmitter, and various analog audio input/output options. The i.MX25 includes only digital audio interfaces: an enhanced serial audio interface (ESAI), a

synchronous serial audio interface (SSI/I^{2}S) and a digital audio multiplexer (AUDMUX) for selecting input sources. Table 4 shows a comparison of the audio features for the i.MX233 and i.MX25.

Table 4. Audio Features Comparison

Feature	i.MX233	i.MX25
Serial Audio Interface	Dual Serial Audio Interface (SAIF) Half duplex	Enhanced Serial Audio Interface (ESAI) Full duplex
SPDIF digital audio out	Yes	N/A
Digital Audio Mux	N/A	Yes
Analog Audio Outputs	Stereo Headphone Amplifier Mono Speaker Amplifier	N/A
Analog Audio Inputs	Mono microphone input Two stereo line inputs	N/A

4.1 i.MX233 SAIF

The i.MX233 includes two SAIF modules. The block diagram for the i.MX233 SAIF is shown in Figure 3.

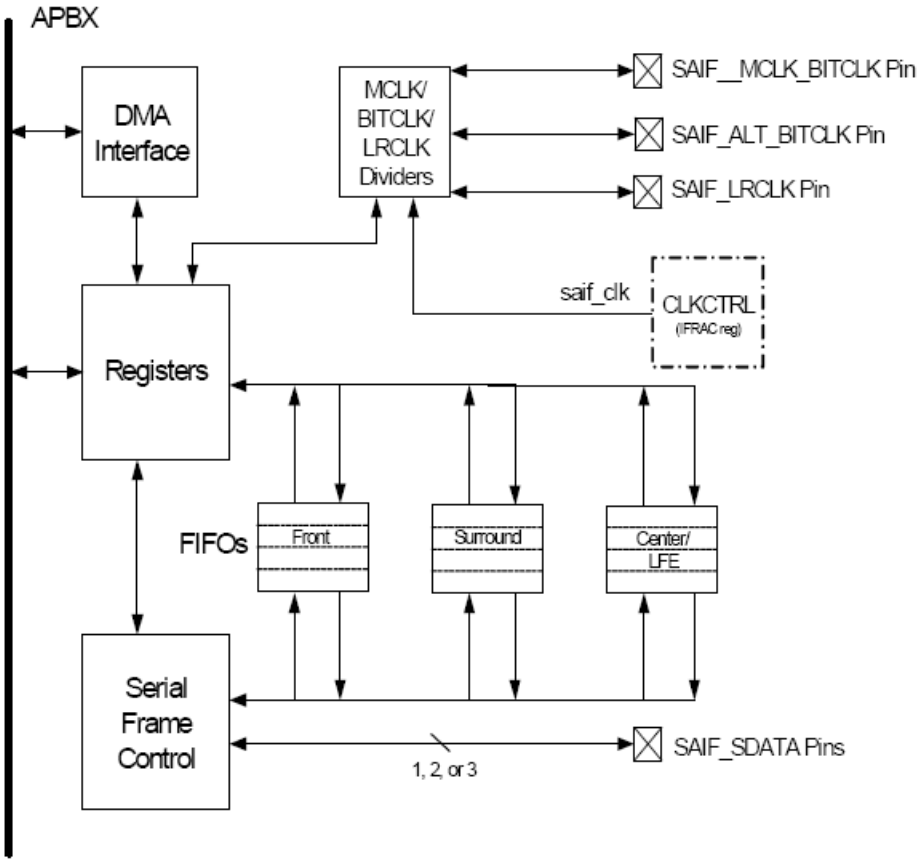


Figure 3. i.MX233 SAIF Block Diagram

The SAIF module is only available on the 169-pin BGA package. The SAIF provides the following functions:

- 3, 4, or 5-wire serial interface to most of the industry common analog codecs
- Half-duplex operations
- 16-bit to 24-bit serial stereo digital audio PCM play/record
- Two, four or six channels supported with three stereo pairs (mono supported in two-channel mode)
- Generic frame control supports I^2S, left- and right-justified frame formats, as well as other non-standard variants of these formats
- Master and slave BITCLK and LRCLK modes (clocks driven to codec or received from codec), as well as optional master MCLK mode
- Sample rates from 8 to 192 kHz using a high-resolution fractional divider driven by the PLL
- Programmable over-sample rate for MCLK output (32×, 48×, 64×, 96×, 128×, 192×, 256×, 384×, and 512×) supports codecs found in systems with both audio and video
- Four-entry FIFOs (per sample pair) buffer either two-channel sample pairs (17–24-bit PCM) or four-packed-channel sample pairs (16-bit PCM)
- Samples transferred to/from the FIFO by the APBX DMA interface, a FIFO service interrupt, or software polling

The SAIF port is a half-duplex port. It can transmit or receive PCM audio, but not simultaneously. Data is communicated one sample at a time serially, alternating between left and right samples. One to three serial data lines (SDATA0–SDATA2) can be used to transmit either two (stereo/mono), four (stereo/surround), or six (stereo/surround/center/LFE) channels of digital PCM audio data. Sample boundaries are delineated by a left/right clock (LRCLK) pin, and individual bits within each sample are delineated by a bit clock (BITCLK) pin.

The LRCLK can be programmed to toggle every 16, 24, or 32 BITCLK transitions. Because data ranges from 16 to 24 bits, serial data within each LRCLK period can either fully occupy the LRCLK cycle or cause the LRCLK period to contain BITCLK cycles in which no data is being communicated. Because of this, three basic types of sample frame formats can be programmed: I^2S, left-justified, and right-justified. Many programming options exist to alter these basic frame types, such as the LRCLK signal polarity, BITCLK edge selection to drive/sample serial data, and sample justification/delay within an LRCLK period.

For codecs that do not contain their own PLL, or for applications which do not include a crystal oscillator to drive the codec, the SAIF can provide a master clock (MCLK) reference that can be configured from 512× down to 32× of the audio data sample rate. This master clock is used for the internal logic of the off-chip codec and to synchronize the BITCLK/LRCLK/SDATA inputs for DAC operation.

The digital PCM audio sample rate is determined by programming a fractional divider within the clock controller module.

4.2 i.MX233 SPDIF Transmitter

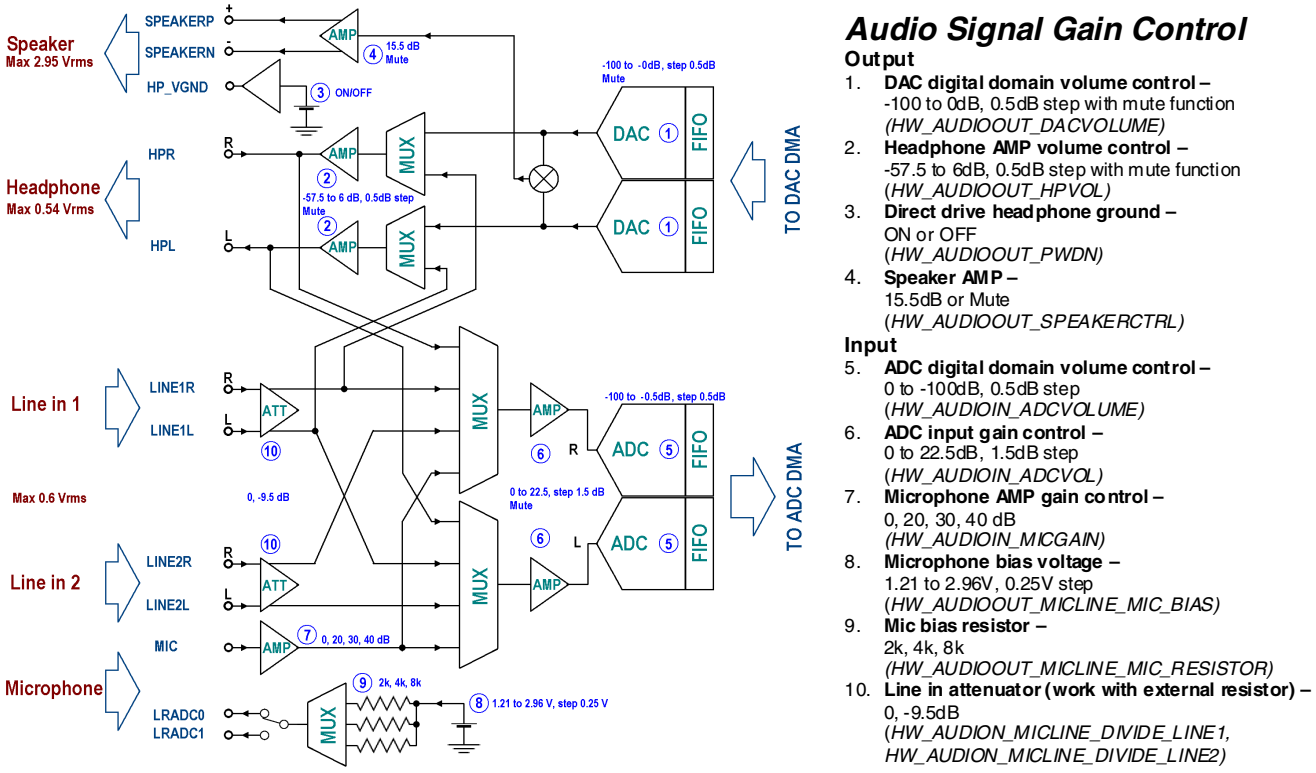
The i.MX233 includes a SPDIF transmitter module which transmits data according to the SPDIF digital audio interface standard (IEC-60958, see http://www.aes.org/ for more information). Data samples are

transmitted as blocks of 192 frames, each frame consisting of two 32-bit sub-frames. A 32-bit sub-frame is composed of a 4-bit preamble, a 24-bit data payload (such as a left- or right-channel PCM sample), and a 4-bit status field. The status fields are encoded according to the IEC-60958 consumer specification, reflecting the contents of the HW_SPDIF_FRAMECTRL and HW_SPDIF_CTRL registers. See the IED-60958 specification for proper programming of these fields.

The sub-frame is transmitted serially, LSB-first, using a biphase-mark channel-coding scheme. This encoding allows a SPDIF receiver to recover the embedded clock signal. The sub-frame information can be changed on-the-fly but is not reflected in the serial stream until the current frame is transmitted. This ensures consistency of the frame and the generated parity appended to that frame.

4.3 i.MX233 Analog Audio

The i.MX233 contains an integrated high-quality mixed signal audio subsystem, including high-quality sigma delta D/A and A/D converters (DAC with 97 dB SNR and ADC with 87 dB SNR), as shown in Figure 4. The D/A converter is the mainstay of the audio decoder/player product application, while the A/D converter is used for voice recording and MP3 encoding applications.



Audio Signal Gain Control

Output

1. **DAC digital domain volume control –** -100 to 0dB, 0.5dB step with mute function *(HW_AUDIOOUT_DACVOLUME)*
2. **Headphone AMP volume control –** -57.5 to 6dB, 0.5dB step with mute function *(HW_AUDIOOUT_HPVOL)*
3. **Direct drive headphone ground –** ON or OFF *(HW_AUDIOOUT_PWDN)*
4. **Speaker AMP –** 15.5dB or Mute *(HW_AUDIOOUT_SPEAKERCTRL)*

Input

5. **ADC digital domain volume control –** 0 to -100dB, 0.5dB step *(HW_AUDIOIN_ADCVOLUME)*
6. **ADC input gain control –** 0 to 22.5dB, 1.5dB step *(HW_AUDIOIN_ADCVOL)*
7. **Microphone AMP gain control –** 0, 20, 30, 40 dB *(HW_AUDIOIN_MICGAIN)*
8. **Microphone bias voltage –** 1.21 to 2.96V, 0.25V step *(HW_AUDIOOUT_MICLINE_MIC_BIAS)*
9. **Mic bias resistor –** 2k, 4k, 8k *(HW_AUDIOOUT_MICLINE_MIC_RESISTOR)*
10. **Line in attenuator (work with external resistor) –** 0, -9.5dB *(HW_AUDION_MICLINE_DIVIDE_LINE1, HW_AUDION_MICLINE_DIVIDE_LINE2)*

Figure 4. i.MX233 Mixed Signal Audio Subsystem

The i.MX233 includes a low-noise headphone driver that allows the i.MX233 to directly drive low-impedance (16 Ω) headphones. The direct drive, or capless mode, removes the need for large expensive DC blocking capacitors in the headphone circuit. The headphone power amplifier can detect headphone shorts and report them through the interrupt collector. A digitally programmable master volume control allows user control of the headphone volume. Use of the headphone amplifier volume control is

recommended as the digital control may reduce SNR performance. Annoying clicks and pops are eliminated by zero-crossing updates in the volume/mute circuits and by headphone driver startup and shutdown circuits.

The microphone circuit has a mono-to-stereo programmable gain pre-amp and an optional microphone bias generator. In addition, there is a stereo line input for external audio sources. Also integrated is a class A-B mono speaker amplifier which must be powered from a sufficiently high-enough current 4.2 V source such as the battery. The speaker amplifier supports bridge-tied configuration only and is capable of providing an output up to 1.75 W_{rms} with a 4.2 V supply and a 4 Ω speaker load.

4.4 i.MX25 ESAI

The i.MX25 includes an ESAI which provides a full-duplex serial port for communication with a variety of serial devices, including industry-standard codecs, SPDIF transceivers, and other DSPs. The ESAI consists of independent transmitter and receiver sections, each with its own clock generator.

The ESAI block diagram is shown in Figure 5. The ESAI is called synchronous because all serial transfers are synchronized to a clock. Additional synchronization signals are used to delineate the world frames. The normal mode of operation is used to transfer data at a periodic rate, one word per period. The network mode is similar in that it is also intended for periodic transfer; however, it supports up to 32 words (time slots) per period. This mode can be used to build time division multiplexed (TDM) networks. In contrast,

the on-demand mode is intended for non-periodic transfers of data and to transfer data serially at high speed when the data becomes available.

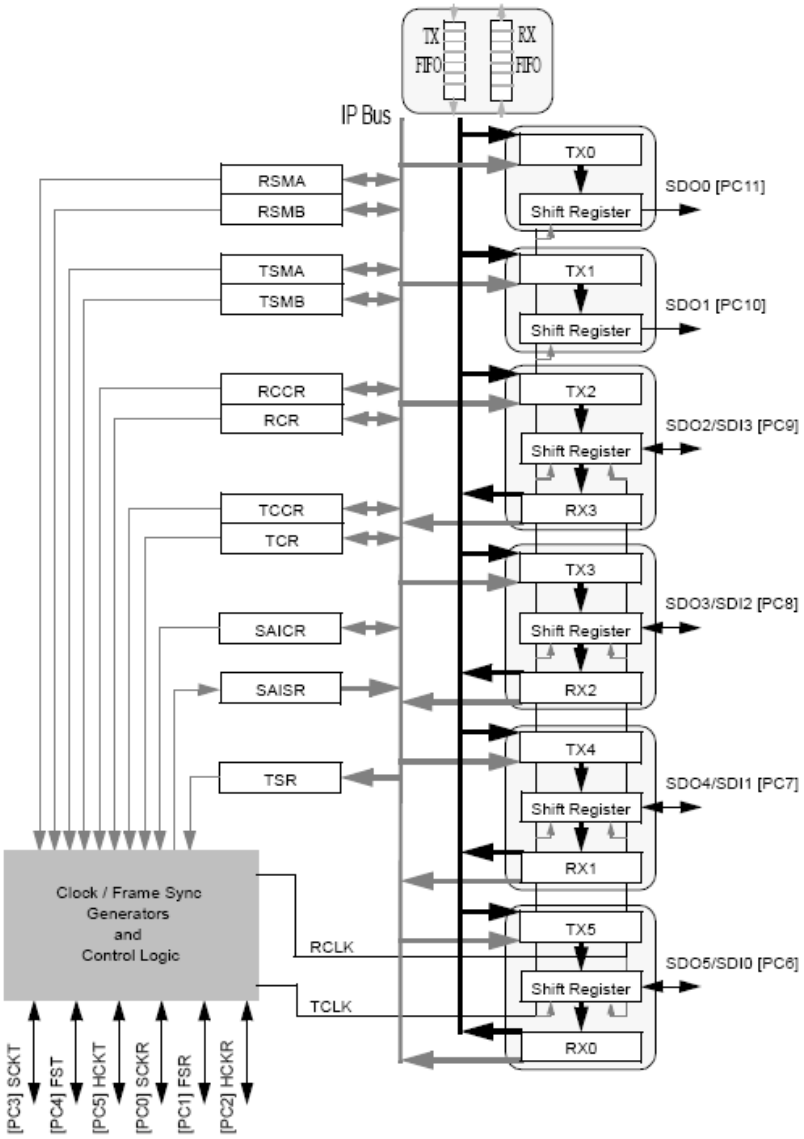


Figure 5. i.MX25 ESAI Block Diagram

The ESAI provides the following features:

- Independent (asynchronous mode) or shared (synchronous mode) transmit and receive sections with separate or shared internal/external clocks and frame syncs, operating in master or slave mode
- Up to six transmitters and four receivers with SDO2/SDI3, SDO3/SDI2, SDO4/SDI1 and SDO5/SDI0 pins shared by transmitters 2 to 5 and receivers 0 to 3; SDO0 and SDO1 pins are used by transmitters 0 and 1 only
- Programmable data interface modes supported are I^2S, LSB aligned, and MSB aligned
- Programmable word length (8, 12, 16, 20 or 24 bits)

- Flexible selection between system clock or external oscillator as input clock source, programmable internal clock divider and frame sync generation
- AC97 support
- Time Slot Mask registers for reduced CPU overhead (for both transmit and receive)
- 128-word transmit and receive FIFO

4.5 i.MX25 Digital AUDMUX

The i.MX25 includes a digital AUDMUX, which is a programmable interconnect for voice, audio and synchronous data routing between the host serial interfaces (SSIs) and peripheral serial interfaces (audio codecs). The AUDMUX has two sets of interfaces: internal ports to on-chip peripherals and external ports to off-chip audio devices. Data is routed by configuring the appropriate internal and external ports.

5 Display and Video

Both the i.MX233 and i.MX25 provide an integrated LCD controller to easily interface with an external LCD module and to provide advanced display processing features. The i.MX233 also includes TV-Out functionality. Table 5 shows a comparison of the display and video features for the i.MX233 and i.MX25.

Table 5. Display and Video Features Comparison

Feature	i.MX233	i.MX25
LCD Interface	Yes	Yes
Resolution	Up to 640 x 480	Up to 800 x 600
Bit/Pixel	8, 16, 18, 24 (color)	1, 2, 4 (mono) 4, 8, 12, 16, 18, 24 (color)
TV-Out	Yes	N/A
Display Processing	Pixel Processing Pipeline (PXP) 8 Overlays Color Key/Alpha Blend Color Space Conversion and Scaling Rotation	1 Overlay (Graphic Window) Color Key/Alpha Blend Panning
CMOS Sensor Interface	N/A	Yes

5.1 i.MX233 Display Processing

The i.MX233 has significantly advanced display processing and output capabilities. The display processing and output consists of four distinct modules as show in Figure 6. These are:

- Display Controller LCDIF
- Pixel Processing Pipeline (PXP)
- PAL/NTSC TV-Encoder
- 10-bit Video DAC (VDAC) for analog composite output

These features allow for all post video-decode pixel processing to be handled in hardware with minimal CPU intervention. Multiple pixel formats and display configurations are also supported.

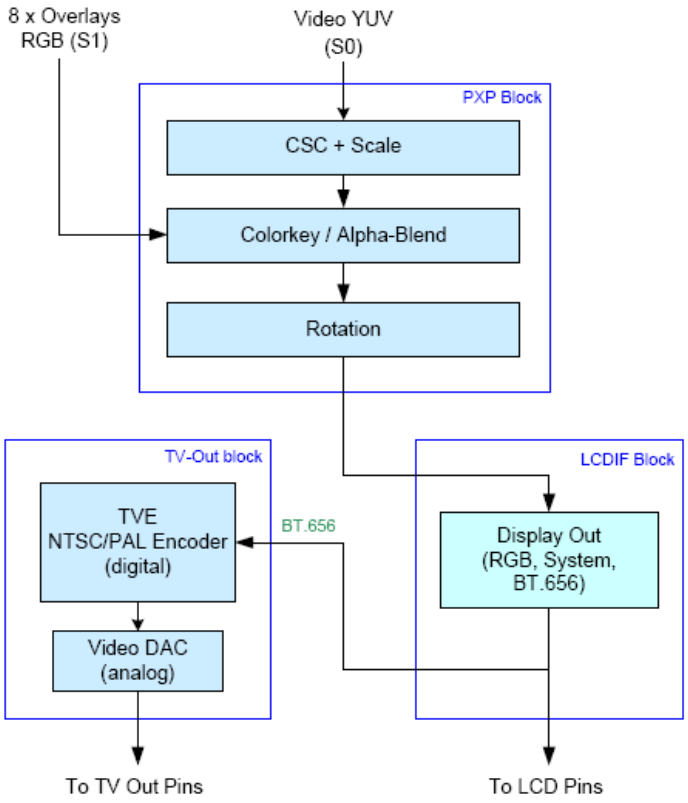


Figure 6. i.MX233 Display Processing Sub-system

The i.MX233 Display Controller (LCDIF) supports the following features:

- 24-bit full color parallel RGB (DOTCLK) mode to drive up to VGA (640×480) full color display at refresh rates up to 60 Hz
- Full 24-bit system mode (8080/6080/VSYNC/WSYNC); read-mode is not supported
- 8, 16, 18 or 24 bpp color display panels
- ITU-R BT.656 compliant D1 digital video output mode with on-the-fly RGB to YCbCr color-space-conversion; this output also feeds the integrated TV-Encoder
- Wide variety of input and output formats allowing for conversion between input and output (RGB565 input to RGB888 output); as well as packed pixel format support

The i.MX233 PXP, shown in Figure 7, performs all necessary post display frame pre-processing in hardware with minimal memory overhead. This allows for the CPU to have maximum processing bandwidth for video-decode operations. For example, the PXP can be used to perform alpha blending of graphics data in graphic or video buffers before sending the data to an LCD display or TV encoder. The

PXP also supports image rotation for handheld devices that require both portrait and landscape image support.

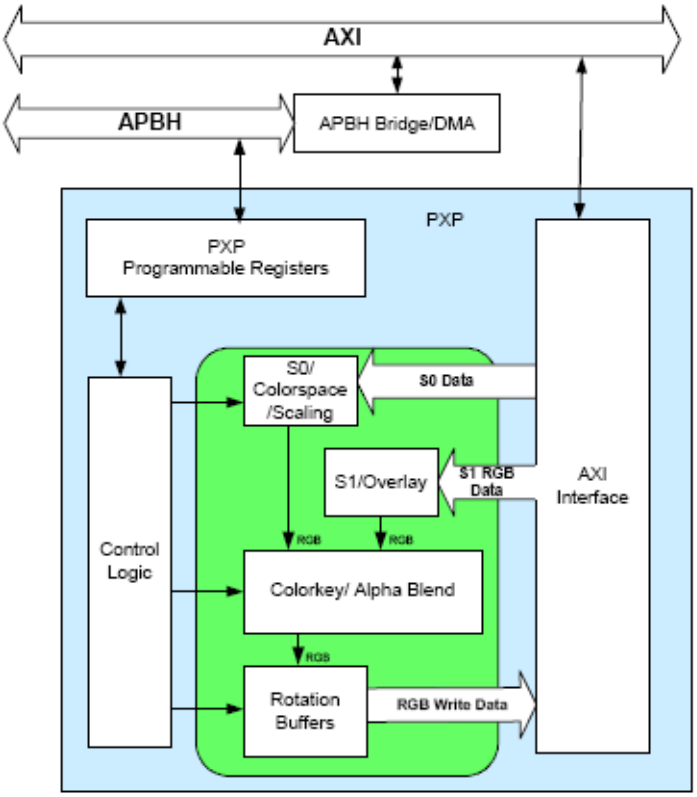


Figure 7. i.MX233 PXP Block Diagram

The PXP has a background image (S0) and one or more overlay images that can be blended with the background. Each overlay image must be a multiple of eight pixels in both height and width and the offset of the overlay into the background image must be a multiple of eight pixels. As the PXP processes data, it reads each 8×8 block from the background image and finds the highest priority (lowest numbered) overlay that is co-located at that block coordinates. The PXP then fetches the overlay and performs the alpha blending and color key operations on the two blocks. The resulting 8×8 pixel block is then written to the corresponding block in the output buffer.

For the S0 plane, the PXP supports RGB images (unscaled) or colorspace conversion (YUV-RGB) and scaling of YUV images. The S1 plane consists of up to eight overlay regions of 16 or 32-bit RGB data. The S0 and S1 planes may then be combined by alpha blending, color key substitution, or raster operations (ROPs) to form the output image. The resulting image may be rotated clockwise in 90° increments or flipped horizontally or vertically. The PXP supports letterboxing and interlacing of progressive content.

The PAL/NTSC TV-Encoder is part of the i.MX233 integrated TV-Out functionality. The encoder takes input directly from the LCDIF without intermediate memory access. In order to utilize the TV-Out path, the LCDIF must be configured to output in ITU-R BT.656/BT.601 D1 digital video stream mode. This stream is synchronized to the internal 108 MHz clock of the TV-Encoder. At this point, the TV-Encoder encodes the stream into a format suitable for the VDAC. Before being sent to the VDAC, the output of the TV-Encoder is passed through a pixel interpolating filter which helps to lessen the requirements for off-chip video filtering.

The i.MX233 includes a fully integrated low-power 10-bit VDAC which takes the direct TV-Encoder output and generates a compliant composite analog video signal (CVBS). Also supported are optional source termination and automatic jack detection (by interrupt) allowing the VDAC to be enable/disabled automatically.

5.2 i.MX25 LCD Controller (LCDC)

The i.MX25 includes a LCDC, shown in Figure 8, which provides display data for external gray-scale or color LCD panels. LCDC is capable of supporting black-and-white, gray-scale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels. The LCDC provides the following features:

- Standard panel interface for common LCD drivers
- Panel interface of 1, 2, or 4-bit for monochrome panels and 4, 8, 12, 16, 18, 24-bit for color panels
- Hardware generated cursor with blink, color, and size programmability
- Logical operation between color hardware cursor and background
- Hardware panning (soft horizontal scrolling)
- Graphic window support for viewfinder function in color display
- Graphic window color keying for graphical hardware cursor
- 256 transparency levels for alpha blending between graphic window and background plane

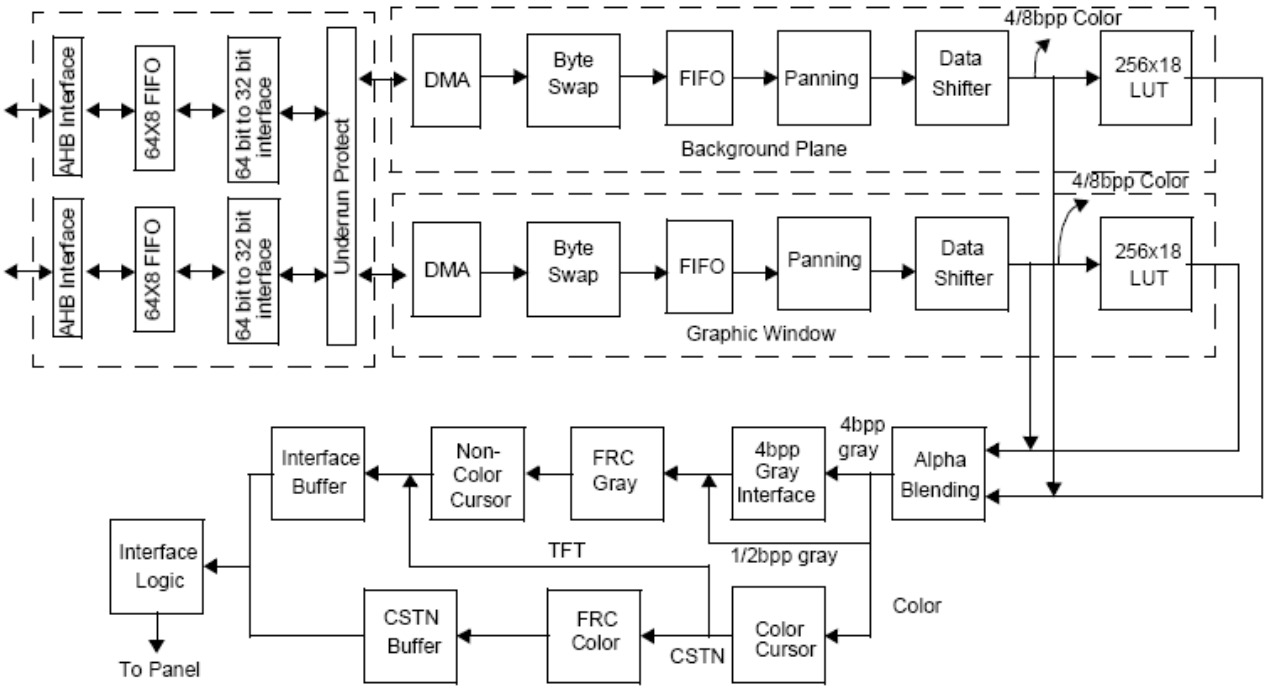


Figure 8. i.MX25 LCD Controller Block Diagram

A graphic window is supported in the LCD color panel screen for viewfinder and graphic hardware cursor functions. The graphic window start address, width and height are software programmable. The position of the graphic window is specified by the graphic window position register. The graphic window and background plane can be alpha blended with a constant alpha for the entire window, so that all pixels in

the graphic window have the same transparency level (256 possible levels). In addition, one of the pixel colors can be chosen for color keying in which the selected pixel color in the graphic window is made completely transparent.

5.3 i.MX25 Smart LCD Controller (SLCDC)

The i.MX25 contains a SLCDC module, shown in Figure 9, for transferring data from a display memory buffer to an external display device. The DMA transfers data transparently with minimal software intervention. In addition, the DMA bus utilization is controllable and deterministic.

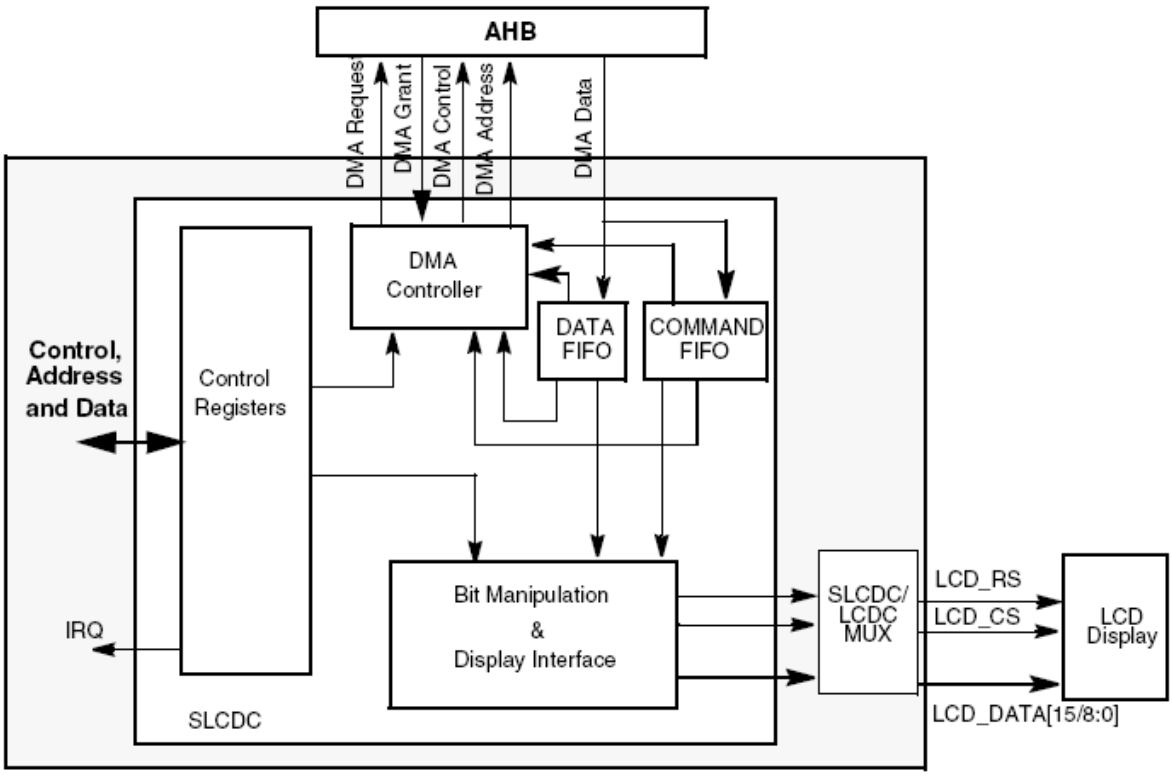


Figure 9. i.MX25 SLCDC System Diagram

As displays become larger and more colorful, demands on the processor increase and more CPU power is needed to render and manage the image. The role of the SLCDC is to reduce the CPU involvement in the data transfer from memory to the display device so that the CPU can concentrate on image rendering. The DMA is used to optimize the data transfer. Embedded control information needed by the display device is automatically read from a second buffer in the system memory and inserted into the data stream at the proper time to completely eliminate the CPUs role in the transfer.

Several display sizes and types are used in different products that use the SLCDC. The SLCDC module has the capability of directly interfacing to the selected display devices. Both serial and parallel interfaces are supported. The SLCDC module only supports writes to the display controller. SLCDC read operations from the display controller are not supported.

5.4 i.MX25 CMOS Sensor Interface (CSI)

The i.MX25 includes a CSI which allows the device to connect directly to external CMOS images sensors. The interface is configurable to support the most commonly available CMOS sensors. The CSI supports both dumb sensors with only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and only Bayer and statistics data output, as well as smart sensors that support CCIR656 video decoder formats and perform additional processing of the image. The CSI also provides a configurable master clock frequency output to the sensor and supports statistic data generation for Auto Exposure (AE) and Auto White Balance (AWB) control of the camera (only for Bayer data and 8-bit/pixel format).

6 Power Management

The i.MX233 has an integrated DC-DC switched controller which allows the device to operate directly from Li-Ion batteries. Both the i.MX233 and i.MX25 provide advanced power management features which make them suitable for low power applications. Table 6 shows a comparison of the power management features for the i.MX233 and i.MX25.

Table 6. Power Management Features Comparison

Feature	i.MX233	i.MX25
Internal Power Supply	DC-DC Switched Converter 4 linear regulators	N/A
Power Management	Adaptive Voltage Control (AVC) Clock Gating Silicon speed and temperature sensors Multiple peripheral clock domains	Dynamic Voltage and Frequency Scaling (DVFS) Clock Gating Active well bias (AWB)
Low-power Mode	Wait for Interrupt RTC mode	Wait Doze Stop Sleep

6.1 i.MX233 Power Management

The i.MX233 contains a sophisticated power management unit (PMU) that includes an integrated DC-DC converter, four linear regulators and a regulated 4.2 V output. The PMU can operate from a Li-Ion battery using the DC-DC converter or from a 5 V supply using the linear regulators and the PMU can automatically switch between them without interrupting operation. The PMU includes circuits for battery and system voltage brownout detection, as well as on-chip temperature, digital speed, and process monitoring.

The integrated PMU converter can be used to provide programmable power for the device as well as the entire application on up to five rails:

- VDDIO (nominal 3.3 V)—DC-DC or linear-regulator from 5 V
- VDDD (nominal 1.2 V)—DC-DC or linear-regulator from VDDA
- VDDA (nominal 1.8 V)—DC-DC or linear-regulator from VDDIO
- VDDM (nominal 2.5 V)—linear-regulator from VDDIO

- VDD4P2 (nominal 4.2 V)—linear regulator when connected to 5 V source

The 4.2 V regulated output also allows for programmable current limits:

- Total load plus battery charge current (5 V limit)
- Battery charge current
- Load current (for both on-chip and off-chip circuits)

The 4.2 V circuit is capable of adjusting distribution of the current supply between the load and the battery-charger depending on programmed current limits and load conditions. For example, when charging the battery and exceeding the 5 V current limit, the 4.2 V regulator steals current from the battery-charger circuit and diverts the current to the load circuit.

The DC-DC converter can operate from a standard Li-Ion battery up to 4.2 V. The converter uses off-chip reactive components (L/C) and can operate in either pulse-width or frequency-modulated mode depending on the load condition. The real-time clock includes an alarm function that can be used to wake-up the DC-DC converter, which then wakes up the rest of the system.

All major functional clock domains/branches have trunk level clock gating for power management. The intent is to gate clock domains off when modules are not necessary for certain applications. This clock gating is instantiated using an ICG element from the standard cell library. Software must enable the clock domain that drives on-chip devices when trunk level clock gating is implemented. The i.MX233 also has multiple peripheral clock domains to control the clocks of individual peripherals in order to save power while optimizing performance. The i.MX233 can be put into a deep suspend mode which reduces the CPU speed to the minimum frequency and shuts down all the peripherals.

The i.MX233 integrates a silicon speed sensor to measure the performance characteristics of an individual die at its ambient temperature and process parametrics. The information given by the speed senor can be monitored by system software to keep the operating voltage to a minimum.

There are two low-power modes on the i.MX233: wait for interrupt mode and RTC mode. In wait for interrupt mode, the CPU clock is stopped and the processor halts and waits for an interrupt to occur. In RTC mode, the CPU and all the peripherals except the RTC are shutdown. The i.MX233 consumes less than 30 µA in RTC mode.

6.2 i.MX25 Power Management

The i.MX25 has three voltage segments:

- Digital Logic—nominal voltage is 1.2 V
- DryIce—sourced from internal power switch, powered from core power supply or coin battery
- Analog—supplies the OSC24M, PLLs, USBPHY, Fusebox, and Touch Screen Controller

The two main active power savings technique are:

- Clock gating—includes two levels of clock gating: clock tree roots (in CRM) and clock tree leaf nodes (in the Modules)
- The Dynamic Voltage/Frequency Scaling (DVFS)—allows simple S/W dynamic voltage frequency scaling; the frequency of the MCU clock domain and the voltage of the device can be changed on the fly while all modules (including the MCU) continue their normal operation

The i.MX25 clock gating reduces the active power consumption by gating the clock to each module while the module is in an idle state. Another technique for reducing power is Active Well Bias (AWB). AWB reduces static power consumption by applying back bias on transistors. AWB can be applied on the ARM core and EMI while they are not functioning.

The i.MX25 low-power modes, shown in Table 7, can reduce the system power to various levels. The ARM core can be put into standby mode, clocks can be gated, PLLs can be stopped in some cases, and the oscillator can be powered off. Furthermore, the core logic voltage can be reduced to state-retention level when the device is idle.

Table 7. i.MX25 Low-Power Modes

Power Mode	Conditions			
	Core	Well Bias	Clocks	Modules
Run	ARM is active	Well bias is off	Clocks are on	Modules are active
Wait	ARM is in wait for interrupt mode	Well bias is off	MCUPLL is on USBPLL is off OSC24M is on OSC32K is on	All other modules are off
Doze	ARM platform clock is off	Well bias is on	MCUPLL is on USBPLL is off OSC24M is on OSC32K is on	All other modules are off
Stop	All PLLs are off	Well bias is on	OSC24M is off OSC32K is on	All other modules are off
Sleep	All PLLs are off Core voltage is dropped to 1 V	Well bias is on	OSC24M is off OSC32K is on	All other modules are off

7 Network

The i.MX233 does not provide any network features. The i.MX25 includes a Fast Ethernet Controller (FEC) and a Controller Area Network (CAN) module. Table 8 shows a comparison of the network features for the i.MX233 and i.MX25.

Table 8. Networking Features Comparison

Feature	i.MX233	i.MX25
Ethernet	N/A	Fast Ethernet Controller (FEC) 10/100
CAN	N/A	Controller Area Network (CAN)

7.1 i.MX25 FEC

The i.MX25 FEC, shown in Figure 10, supports both 10 and 100 Mbps Ethernet/IEEE 802.3 networks.

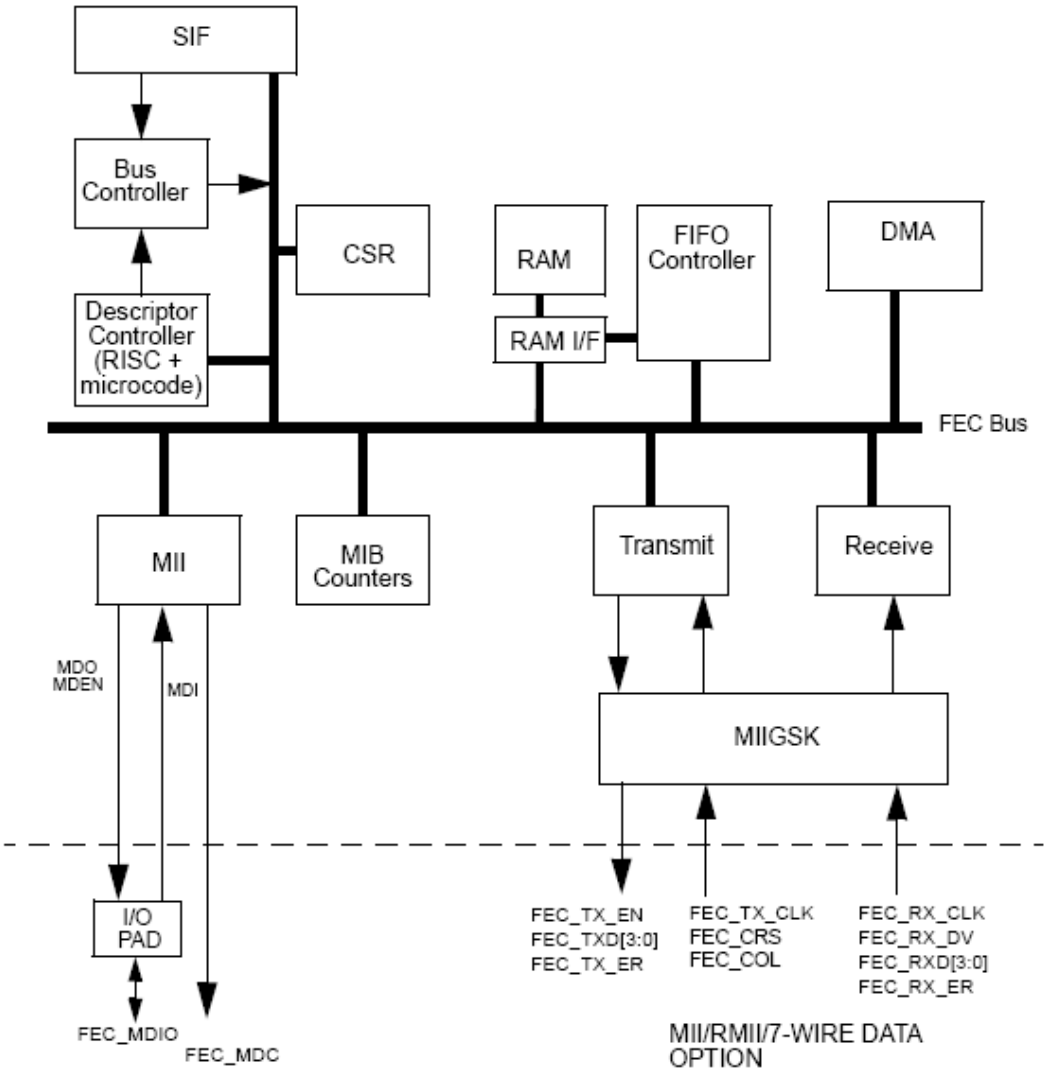


Figure 10. i.MX25 FEC Block Diagram

An external transceiver interface and transceiver function are required to complete the interface to the media. The FEC supports three different standard MAC-PHY (physical) interfaces for connection to an external Ethernet transceiver: 10/100 Mbps MII, 10/100 Mbps RMII and the 10 Mbps-only 7-wire interface, which uses a subset of the MII pins.

7.2 i.MX25 Controller Area Network (FlexCAN)

The i.MX25 FlexCAN module is a communication controller implementing the CAN protocol according to the CAN2.0B protocol specification. A general block diagram, shown in Figure 11, describes the main submodules implemented in the FlexCAN module, including two embedded memories, one for storing

message buffers and one for storing individual Rx mask registers. Support for 64 message buffers is provided.

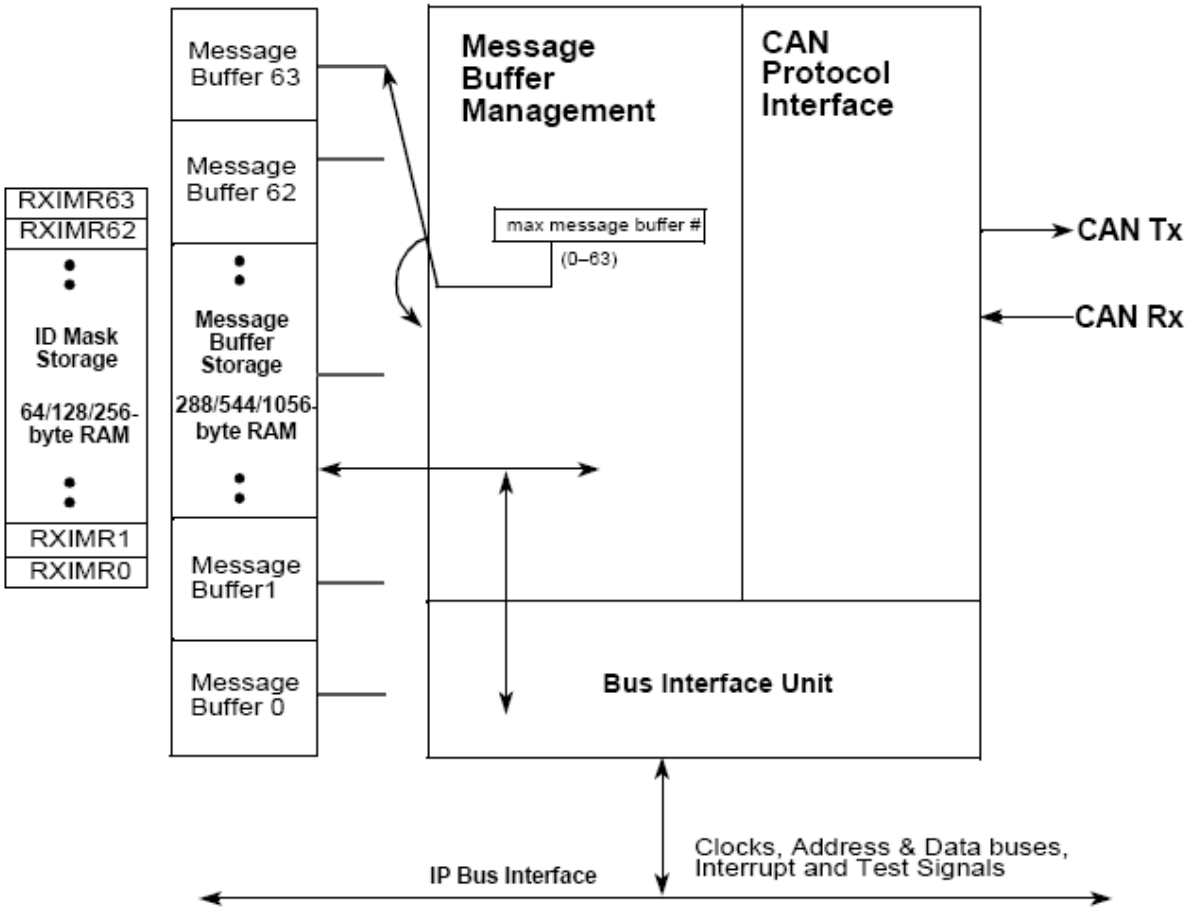


Figure 11. i.MX25 FlexCan Block Diagram

8 Communications

Both the i.MX233 and i.MX25 provide a rich set of peripherals for external communications such as UART and I^2C. Table 9 shows a comparison of the communications features for the i.MX233 and i.MX25.

Table 9. Communications Features Comparison

Feature	i.MX233	i.MX25
UART	3 UART	5 UART
UART Speed	Up to 3.25 Mbps	Up to 4 Mbps
IrDA	N/A	UART IrDA compatible
I^2C Interface	Yes	Yes
Serial Peripheral Interface	Synchronous Serial Port (SSP)	Configurable Serial Peripheral Interface (CSPI)
Synchronous Serial Interface (SSI)	N/A	Yes

Table 9. Communications Features Comparison (continued)

Feature	i.MX233	i.MX25
Subscriber Identification Module (SIM)	N/A	Yes
1-Wire Module	N/A	Yes

8.1 i.MX233 Communication Interfaces

The i.MX233 includes three EIA/TIA compatible UARTs: two for application use and one for debug use. The application UARTs are high-speed devices capable of running up to 3.25 Mbps with 16-byte receive and transmit FIFOs. The application UARTs support DMA and flow control (CTS/RTS). The debug UART can only run up to 115.2 Kbps and does not support DMA and flow control.

The i.MX233 contains a two-wire SMB/I^2C bus interface. It can act as either a slave or master on the SMB interface. The on-chip ROM supports boot operations from I^2C mastered EEPROMs, as well as a slave I^2C boot mode. The interface supports both standard speed (up to 100 Kbps) and fast speed (up to 400 Kbps) I^2C connections. Typical applications for the I^2C bus include EEPROM, LED/LCD, FM tuner, and cell phone baseband device connection.

The i.MX233 also contains two integrated synchronous serial ports (SSP) each with a dedicated DMA channel and a dedicated clock divider from the PLL. Each SSP supports a wide range of synchronous serial interfaces, including:

- 1, 4 or 8-bit high-speed MMC/SD/SDIO
- Motorola (1-bit) and Winbond (1, 2, and 4-bit) SPI with up to three slave selects
- TI SSI

8.2 i.MX25 Communication Interfaces

The i.MX25 includes five high speed TIA/EIA compatible UARTs which are capable of running up to 4 Mbps. Each UART has two independent, 32-entry FIFOs for transmit and receive. The UARTs also support DMA, flow control (CTS/RTS), and DCE/DTE capability as well as auto baud rate detection up to 115.2 Kbps. The IrDA functionality can be provided by the UART with the use of external circuitry, but the speed is limited to 115.2 Kbps.

The i.MX25 I^2C provides a standard two-wire serial interface for connecting the device with peripherals or host controllers. The I^2C module provides the functionality of a standard I^2C master and slave. This interface operates in both standard speed (up to 100 Kbps) and fast speed (up to 400 Kbps) depending on the pin loading and timing characteristics.

The i.MX25 Configurable Serial Peripheral Interface (CSPI) module is a full-duplex, synchronous, four-wire serial communication module. The CSPI contains an 8×32 receive buffer (RXFIFO) and an 8×32 transmit buffer (TXFIFO). Using data FIFOs, the CSPI allows rapid data communication with fewer software interrupts. The CSPI is master/slave configurable with four chip select signals to support multiple peripherals. The CSPI can operate on a frequency up to one-quarter of the reference clock frequency.

The i.MX25 also provides a Synchronous Serial Interface (SSI) which is a full-duplex, serial port that allows the device to communicate with a variety of serial devices. These serial devices can be standard

codecs, digital signal processors (DSPs), microprocessors, peripherals, and popular industry audio codecs that implement the inter-IC sound bus standard, I^2S and Intel AC97 standard.

The i.MX25 Subscriber Identification Module (SIM) is designed to facilitate communication to SIM cards or Eurochip pre-paid phone cards. The SIM block diagram is shown in Figure 12. The SIM module has two ports that can be used to interface with various cards. The interface with the MCU is a 32-bit connection to the IP bus.

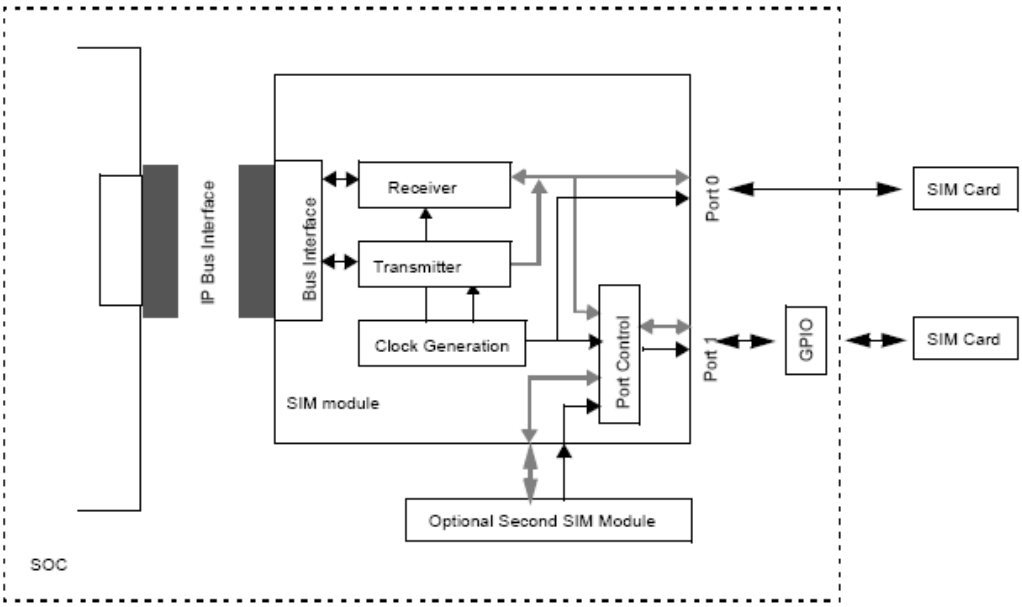


Figure 12. i.MX25 SIM Block Diagram

The i.MX25 includes a 1-Wire module, shown in Figure 13, to provide the communication link to a generic 1-Kbit add-only memory. The module sends or receivers one bit at a time with an option for software to manage the data using bytes. The required protocol for accessing the generic 1-Wire device is defined by Maxim-Dallas. The generic 1-Wire device holds battery characteristic information.

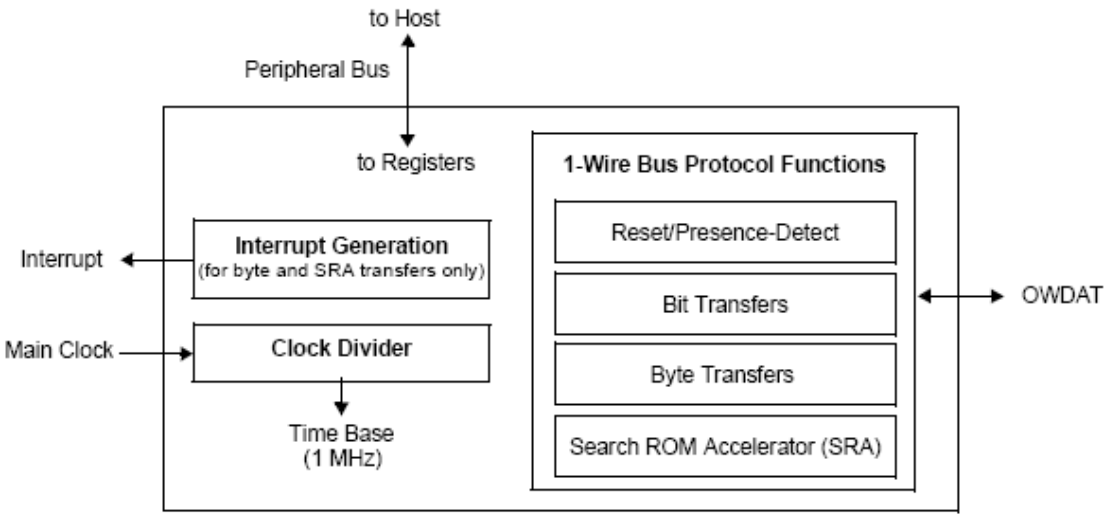


Figure 13. i.MX25 1-Wire Module Block Diagram

9 I/O Modules

Table 10 shows a comparison of the I/O modules for the i.MX233 and i.MX25.

Table 10. I/O Modules Comparison

Feature	i.MX233	i.MX25
USB 2.0 High Speed	1 HS port (Host/Device) with HS PHY (does not support LS)	1 HS port (OTG/Device) with HS PHY + 1 HS port (Host) with FS PHY
Pulse Width Modulator (PWM)	5 channels	4 channels
General Purpose I/O (GPIO)	Yes	Yes
I/O Multiplexer	Pin Multiplexing Scheme	Yes
Low Resolution ADC	Yes (12-bit resolution)	Yes (12-bit resolution)
Touch Screen Controller	Yes (4-wire resistive)	Yes (4/5-wire resistive)
Keypad Port (KPP)	N/A	Yes

9.1 USB Interface

Both the i.MX233 and i.MX25 include a high-speed Universal Serial Bus (USB) version 2.0 controller and an integrated USB transceiver macrocell interface (UTMI) PHY. The USB interface is capable of operating as either a USB device or a USB host.

The i.MX233 device interface can be attached to USB 2.0 hosts and hubs running in the USB 2.0 high-speed mode at 480 Mbps. The i.MX233 can also be attached to USB 2.0 full-speed interfaces at 12 Mbps, but the low-speed interfaces are not supported. The USB port is a dynamically configured port that can support up to five endpoints, each of which may be configured for bulk interrupt or isochronous transfers. The USB configuration information is read from on-chip memory by the USB controller DMA.

The i.MX25 contains a USB 2.0 On-The-Go (OTG) as well as a USB 2.0 host, both of which are capable of operating in high-speed mode at 480 Mbps. Both ports can also operate in USB 2.0 full-speed (12 Mbps) and low-speed (1.5 Mbps) modes. The OTG has an integrated HS PHY. The HS host has an integrated FS PHY, but is able to support HS external PHY through the ULPI interface. The module has DMA capabilities for handling data transfer between internal buffers and system memory.

9.2 PWM Controller

Both the i.MX233 and i.MX25 contain Pulse Width Modulator (PWM) output controllers. Applications for the PWM include LED and backlight brightness control. The PWM controller can be also be used with external components as a high voltage generator for an electroluminescent lamp (E.L.) display backlight. The i.MX25 PWM controller is optimized to generate tones and sound from stored audio images.

9.3 GPIO and Pin Multiplexing

The i.MX233 has four banks of pins, three of which can be used as general-purpose input/output (GPIO) pins. All digital pins have selectable output drive strength and weak internal keepers to minimize power loss due to undriven pins. The i.MX233 contains a rich set of specialized hardware interfaces, but does not

have enough pins to allow use of all interface signals simultaneously. A pin multiplexing scheme is used to choose which interfaces to enable. In addition, the GPIO pins may be used as interrupt inputs and the interrupt trigger type is configurable.

The i.MX25 allows pin sharing by multiple hardware interfaces with a input-output multiplexer (IOMUX). The IOMUX module deals with signal multiplexing and consists of combinational logic built with a basic IOMUX cell. Each pin, which is shared by multiple signals, has a related IOMUX cell to handle signal multiplexing. Each IOMUX cell can support up to eight mux modes (ATL0–ATL7), so that each pin can be ultimately shared by eight signals.

9.4 Touch Screen Controller and ADC

The i.MX233 contains a Low-Resolution ADC (LRADC) which provides 16 physical channels of 12-bit analog-to-digital conversion. Only eight virtual channels can be used at a time, but those eight channels can be mapped to any of the 16 physical channels. Some physical channels have dedicated inputs. The remaining six channels are available for other uses such as resistive button sense, touch-screens, or other analog input. Channels 0 and 1 have integrated current sources to drive external temperature monitor thermistors. Channels 2–5 have integrated drivers for resistive touch-screens with drive voltage generation and touch-detection interrupt circuit. The LRADC provides typical performance of 12-bit no-missing-codes, 9-bit/~56 dB SNR, and 1% absolute accuracy (limited by the bandgap reference).

The i.MX25 Touch Screen Controller (TSC) and associated Analog to Digital Converter (ADC) together provide a resistive touch screen solution for low cost PDAs, cell phones, ePOS devices, and multimedia players, as shown in Figure 14. The ADC has 12-bit resolution and supports a sample rate up to 125 kHz. The module implements simultaneous touch screen control and auxiliary ADC operation for temperature, voltage and other measurement functions. The module includes the driver switches for controlling the screen and an input multiplexer to allow one of four additional inputs to be supported. The ADC reference voltage can be configured in differential and single ended modes. The controller supports pen touching screen detection for automatically interrupting the processor to measure only as needed.

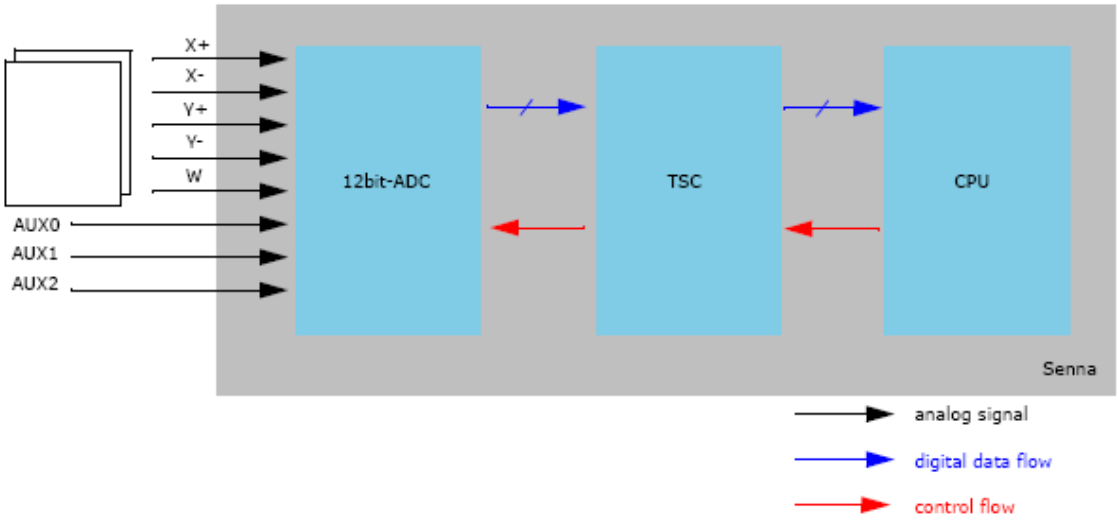


Figure 14. i.MX25 TSC in System

9.5 i.MX25 Keypad Port (KPP)

The i.MX25 KPP, shown in Figure 15, is a 16-bit peripheral that can be used as a keypad matrix interface or as GPIO. The KPP is designed to interface with a keyboard matrix with 2-point contact or 3-point contact keys. The KPP is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPP is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad.

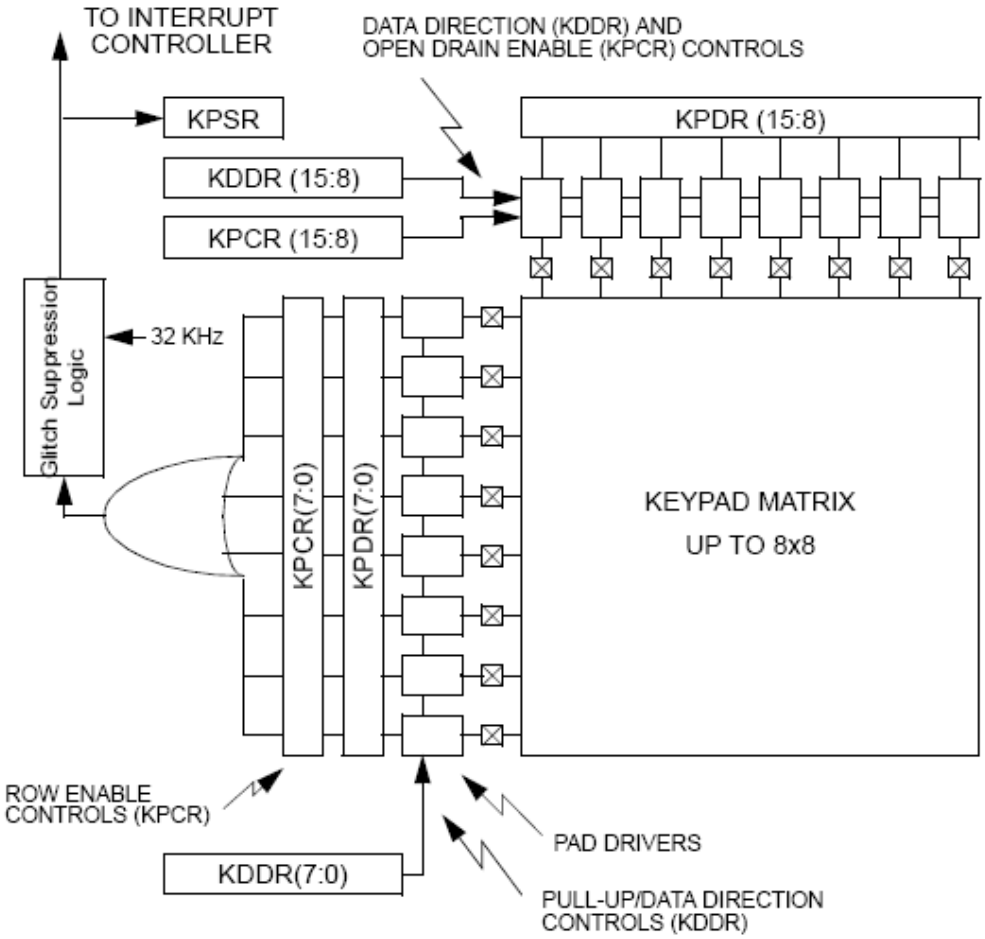


Figure 15. i.MX25 KPP Peripheral Block Diagram

10 Boot Modes

Both the i.MX233 and i.MX25 can be booted from a number of different interfaces. Table 11 shows a comparison of the boot modes for the i.MX233 and i.MX25.

Table 11. Boot Modes Comparison

Feature	i.MX233	i.MX25
I^2C	Yes	Yes
SPI	Yes	Yes

Table 11. Boot Modes Comparison (continued)

Feature	i.MX233	i.MX25
SD/MMC	Yes	Yes
NAND	Yes	Yes
JTAG	Yes	Yes
NOR Flash	N/A	Yes
USB	Yes	N/A
UART	N/A	Yes
WEIM	N/A	Yes

10.1 i.MX233 Boot Modes

The boot modes supported by the i.MX233 ROM are listed in Table 12. The boot mode can be selected either through external resistors or by OTP eFuse bit programming.

Table 12. i.MX233 ROM Supported BOM Modes

Port	Boot Mode
USB	Encrypted/unencrypted USB slave boot mode
I^2C	Encrypted/unencrypted I^2C master—boots from 3.3 V EEPROM
SPI1	Encrypted/unencrypted SPI master from SSP1—boots from 3.3 V Flash memory
SPI2	Encrypted/unencrypted SPI master from SSP2—boots from 3.3 V Flash and EEPROM
SSP1	Encrypted/unencrypted SD/MMC master from SSP1—boots from 3.3 V 1-bit, 4-bit and 8-bit SD/MMC cards
SSP2	Encrypted/unencrypted SD/MMC master from SSP2—boots from 3.3 V 1-bit, 4-bit and 8-bit SD/MMC cards
GPMI	Encrypted/unencrypted NAND, 3.3 V 8-bit wide and ECC4 and ECC8
JTAG_WAIT	Unencrypted startup—waits for JTAG debugger connection

The boot pins on the i.MX233 are located on LCD_RS, LCD_DATA[5] and LCD_DATA[3:0]. LCD_RS is pulled up to enable boot mode selection from the LCD data pins. The ROM probes the LCD_RS pin and if it is pulled up, the boot ROM decodes the boot mode vector from the data pins. If LCD_RS is pulled down, then the boot mode is determined by the OTP eFuse bits. In either case, the ROM code selects the boot mode according to the selection map illustrated in Table 13.

Table 13. i.MX233 Boot Mode Selection Map

ETM Enable/ LCD_ DATA[5]	BM3/ LCD_ DATA[3]	BM2/ LCD_ DATA[3]	BM1/ LCD_ DATA[1]	BM0/ LCD_ DATA[0]	Port	Boot Mode
0/1	0	0	0	0	USB	USB (unencrypted/encrypted is under OTP control)
0/1	0	0	0	1	I^2C	I^2C master
0/1	0	0	1	0	SPI	SPI m aster SSP1 boot from Flash

Table 13. i.MX233 Boot Mode Selection Map (continued)

ETM Enable/ LCD_ DATA[5]	BM3/ LCD_ DATA[3]	BM2/ LCD_ DATA[3]	BM1/ LCD_ DATA[1]	BM0/ LCD_ DATA[0]	Port	Boot Mode
0/1	0	0	1	1	SPI	SPI m aster SSP2 boot from Flash
0/1	0	1	0	0	GPMI	NAND
0/1	0	1	0	1	—	Reserved
0/1	0	1	1	0	JTAG_WAIT	Startup waits for JTAG debugger connection
x	0	1	1	1	—	Reserved
0/1	1	0	0	0	SPI	SPI m aster SSP2 boot from EEPROM
0/1	1	0	0	1	SSP1	SD/MMC master on SSP1
0/1	1	0	1	0	SSP2	SD/MMC master on SSP2
x	1	0	1	1	—	Reserved
0/1	1	1	0	0	—	Reserved
0/1	1	1	0	1	—	Reserved
x	1	1	1	0	—	Reserved
x	1	1	1	1	—	Reserved

10.2 i.MX25 Boot Modes

The i.MX25 processor boots using the HAB contained within internal ROM. The ROM configures the hardware and validates the image residing in memory using the HAB library. The boot image can be loaded from different memory/device sources and the boot image is controlled by the boot mode pins, BMOD[1:0], sampled at the exit of reset. The i.MX25 boot mode types are summarized in Table 14.

Table 14. i.MX25 Boot Mode Summary

BMOD[1:0]	Boot Type	Boot Details
0 0	Internal Boot	Executing ROM code, which handles booting from following sources: • NOR Flash (WEIM, 16-bit, slow asynchronous mode for debugging purpose) • OneNAND • SPI (serial Flash, Chip Select #1)/I^2C • NAND Flash, MLC NAND 0.5 Kbyte/512 byte, 2 Kbyte/4 Kbyte page (e-fuse selectable) • SD/MMC (support high capacity)/MoviNAND boot (through MMC interface)
0 1	Reserved	Reserved
1 0	External (Direct) Boot	HW only (Direct boot through interface, independent of boot ROM code) boot from WEIM interface
1 1	USB/UART Boot Loader	Load and execute code through serial devices: • USB (Full-speed, by integrated PHY or external) • UART

10.2.1 i.MX25 Internal Boot

Internal boot is selected by driving value of 0b00 on the BMOD[1:0] pins at device power up. In this mode, the core boots from internal ROM. The boot code performs hardware initialization, application image validation using the HAB library, and then jumps to an address derived from the application image. If any error occurs during internal boot, the boot code jumps to the UART/USB secure download. Internal boot mode is the only secure boot mode.

The internal boot supports the following boot Flash devices:

- NOR Flash with WEIM interface, located on CS0, bus width of 16 bits
- OneNAND
- MLC NAND and SLC NAND Flash with NFC interface—page sizes of 512 bytes, 2 Kbyte or 4 Kbyte, bus width of 8 or 16 bits
- SD/MMC through the eSDHC interface, supporting high capacity cards
- EEPROM boot through the SPI (serial Flash) and I^2C (through CSPI and I^2C modules respectively)

The boot ROM determines the boot device by reading BT_MEM_CTL[1:0] bits on the eFuse as shown in Table 15.

Table 15. i.MX25 Internal Boot Memory Control Type

BT_MEM_CTL[1:0]	Boot Memory Control Type (Memory Device)
0 0	WEIM
0 1	NAND Flash
1 0	Reserved
1 1	Expansion Device (SD/MMC/MoviNAND, support high storage, EEPROMs)

10.2.2 i.MX25 External Boot

External boot is supported on the i.MX25 from the WEIM interface only. It is selected by driving a value of 0b10 on the BMOD[1:0] pins at device power up, provided that the fuse DIR_BT_DIS is not burned. In this mode, the core boots directly from an external memory, and this mode supports either muxed or non-muxed address data boot from the WEIM interface. This mode is a non-secure boot mode.

10.2.3 i.MX25 UART/USB Boot Loader

The UART/USB boot loader is selected by driving value of 0b11 on the BMOD[1:0] pins, at device power up. Bootable UART is selected by the BT_UART_SRC[2:0] fuses. Selection between UART and USB download boot device is determined by polling the UART and USB controllers in turn. The device that shows activity first, is selected.

For the UART, activity is detected by the Receive Data Ready (RDR) flag showing at least one character has been read into the FIFO. The bootable UART (UART 1–5) is selected by the BT_UART_SRC[2:0] fuses.

For the USB, either of the integrated on-chip PHYs can be used, as well as an external PHY using the ULPI interface. For typical application board usage, the internal PHY option is recommended. The external PHY option is not recommend because it comes at the expense of availability of pins. Activity is detected by the setup endpoint status register showing that the setup transaction is received. Booting from the OTG port is not possible on the current silicon revision due to an errata on the USB OTG VBus pin.

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