Freescale Semiconductor
Application Note

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PowerQUICC III MPC8555E and MPC8541E Bring-Up Guidelines

by *Freescale Semiconductor, Inc.*

This document provides bring-up guidelines for designs based on the MPC8555E and the MPC8541E devices from the PowerQUICC III family of integrated communications processors (collectively referred to throughout this document as PowerQUICC III). This document can also be useful in debugging newly designed systems by highlighting the aspects of a design that merit special attention during initial system startup.

Contents

1. Getting Started 1
2. Power 3
3. Clocking 6
4. Debug 9
5. Power-On Reset/Reset Configurations 13
6. Functional Blocks 16
7. Revision History 23

1 Getting Started

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC III device, it is recommended that you familiarize yourself with the available documentation, software, microcodes, models, and tools.

1.1 References

Some of the references below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer or sales representative.

- Collateral
  - *MPC8555E/MPC8541E PowerQUICC III Integrated Communications Processor Reference Manual* (MPC8555ERM)
  - MPC8555E / MPC8541E Device Errata (MPC8555ECE)
  - *MPC8555E Integrated Processor Hardware Specifications* (MPC8555EC)
  - *MPC8541E Integrated Processor Hardware Specifications* (MPC8541EC)
- Available Tools
  - CPM Performance Tool
  - Boot Sequencer Generator Tool
  - Pin Mux Tool
  - UPM Programming Tool
- Models
  - IBIS
  - BSDL, Rev 1.1 silicon

1.2 Device Errata

The device errata documents (MPC8555ECE, MPC8541ECE) describe the latest fixes and workarounds for the PowerQUICC III family of devices. You should thoroughly research these errata documents before starting a design with the respective PowerQUICC III device.

1.3 Communications Processor Module (CPM) Performance and Bus Utilization Tool

The PowerQUICC III CPM runs by time-sharing multiple communication protocols. To estimate the CPM load factor for a particular combination of protocols, use the CPM Performance Evaluator tool, which is available on the MPC8555E/MPC8541E device web site. At startup, the tool initializes all parameters with default values that may not be the optimal values for your design. For example, the tool initializes with transmit and receive rates of ‘0’. These values must be changed according to the needs of the application.

1.4 Boot Sequencer Tool

The PowerQUICC III features the boot sequencer to allow configuration of any memory-mapped register before power-on reset (POR) completes. The register data to be changed is stored in an I^2C EEPROM. The PowerQUICC III requires a particular data format for register changes as outlined in the MPC8555ERM. The boot sequencer tool is a C code file. When compiled and given a sample data file, it generates the appropriate raw data format as outlined in the MPC8555ERM—that is, an s-record file that can be used to program the EEPROM.

1.5 Pin Mux Tool (MPC8555 only)

The on-chip serial communications peripherals use four 32-bit parallel ports to exchange data with the physical interfaces. On each pin of the parallel ports, several signals are multiplexed. If none of the signals available on a certain pin are necessary in a certain application, the pin can be used for a general purpose I/O. To verify the availability of the I/O functions chosen through pin multiplexing, designers are encouraged to use the MPC8555 Parallel Ports Pin Mux tool. After selecting the signals required by your application, this utility assists in defining the pin configuration of each parallel port. A report can then be generated that includes all your selections and C-initialization code for the registers associated with the parallel ports. The Pin Mux tool is available on the MPC8555E device web site.

1.6 UPM Programming Tool

The UPM Programming Tool features a GUI for a user-friendly programming interface. It allows programming of all three PowerQUICC III UPM machines. The GUI consists of a wave editor, table editor, and report generator. You can edit directly the waveform or the RAM array. At the end of programming, the report generator prints out the UPM ram array that can be used in a C-program. The UPM Programming Tool is available on the MPC8555E or MPC8541E device web site.

1.7 Available Training

Our third-party partners are part of an extensive Design Alliance Program. Our current training partners are listed on our external web site under the Design Alliance Program. In addition, training material from past Smart Network Developer's Forums is available. These training materials are a valuable resource in understanding the PowerQUICC III.

2 Power

This section provides design considerations for the PowerQUICC III power supplies, as well as power sequencing. For information on AC and DC electrical specifications and thermal characteristics for the PowerQUICC III, refer to the MPC8555EEC and the MPC8541EEC. For power sequencing recommendations refer to Section 2.3, "Power Sequencing."

2.1 Power Supply

The PowerQUICC III has a core voltage V_{DD} that operates at a lower voltage than the I/O voltages GV_{DD}, LV_{DD}, and OV_{DD}. It is recommended that the core voltage V_{DD} of the PowerQUICC III be supplied through a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage, 1.2 V (±5%), is supplied across V_{DD} and GND.

The I/O blocks of the PowerQUICC III are supplied with 2.5 V (±5%) across GV_{DD} and GND, 2.5 V (±5%) or 3.3 V (±5%) across LV_{DD} and GND, and 3.3 V (±5%) across OV_{DD} and GND. Typically, these are supplied by simple linear regulators. This increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design. No external signals on PowerQUICC

III are 5-V-tolerant. All input signals need to meet the G/L/OV_{IN} DC specification of the respective I/O block. See Table 1.

Table 1. Power Supplies

Type	Name	Block	(V)
Core	V_{DD}	—	1.2
PLL	AV_{DD}	Core PLL, Platform PLL, CPM PLL, PCI1, PCI2	1.2
I/O	GV_{DD}	DDR	2.5
I/O	LV_{DD}	TSEC	2.5 / 3.3
I/O	OV_{DD}	CPM, LBIU, DMA, MII-mgt, PIC1, PCI2, I^2C	3.3

2.2 Power Consumption

The MPC8555EEC and the MPC8541EEC hardware specifications provide estimated power dissipation for various frequency configurations of the core complex bus (CCB) clock and the e500 core frequencies. Suitable thermal management is required to ensure that the junction temperature does not exceed the maximum specified value. The numbers provided in the hardware specification include dissipation for all blocks except the PLL supplies and the I/Os. Both must be added to the typical number to determine accurately whether a heat sink or other form of chip cooling mechanism is required.

2.3 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. These rates depend on the power supply, the type of load on each power supply, and the way different voltages are derived. The MPC8555E and MPC8541E require the power rails to be applied in a specific sequence to ensure proper device operation. The requirements for power-up are as follows:

1. V_{DD}, AV_{DD}
2. GV_{DD}, LV_{DD}, OV_{DD} (I/O supplies)

Items on the same line have no ordering requirements with respect to one another. Items on separate lines must be ordered sequentially so that voltage rails on a previous step reach 90 percent of their value before the voltage rails on the current step reach 10 percent of theirs. If the items on line 2 must precede items on line 1, take care to ensure that the delay does not exceed 50 mS and that the power sequence is not performed more than once per day in a production environment.

NOTE

To guarantee MCKE low during power-up, GVDD should be the last power supply to come up. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing is not required.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, then the port pins on the MPC8555E and MPC8541E CPMs may drive a logic-one or -zero during power-up.

Table 2 lists the current maximum ratings for the power supplies. Supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the Recommended Operating Conditions table in the hardware specification is recommended. Any information in the relevant hardware specification supersedes information in Table 2.

Table 2. Maximum Voltage Ratings

Type	Name	Block	(V)	(Vmax)
Core	Vdd	—	1.2	1.32
PLL	AVdd	Core PLL, Platform PLL, CPM PLL, PCI1, PCI2	1.2	1.32
I/O	GVdd	DDR	2.5	3.63
I/O	LVdd	TSEC	2.5 / 3.3	2.75 / 3.63
I/O	OVdd	CPM, LBIU, DMA, MII-mgt, PIC1,PCI2, I^2C	3.3	3.63

2.4 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.5 Decoupling

Due to large address and data buses and high operating frequencies, the PowerQUICC III can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC III system, and the PowerQUICC III itself requires a clean, tightly regulated source of power. Therefore, you should place at least one decoupling capacitor at each V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and pins of the PowerQUICC III. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part. These capacitors should have a value of 0.01 or 0.1 µF. To minimize lead inductance, only ceramic SMT (surface mount technology) capacitors should be used. In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, GV_{DD}, LV_{DD}, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF. Simulation is strongly recommended to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.6 PLL Power Supply Filtering

Each PowerQUICC III PLL is provided with power through independent power supply pins for the MPC8555E, and MPC8541E ($AV_{DD}1$, $AV_{DD}2$, $AV_{DD}3$, $AV_{DD}4$, and $AV_{DD}5$). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low-frequency filter as shown in Figure 1.

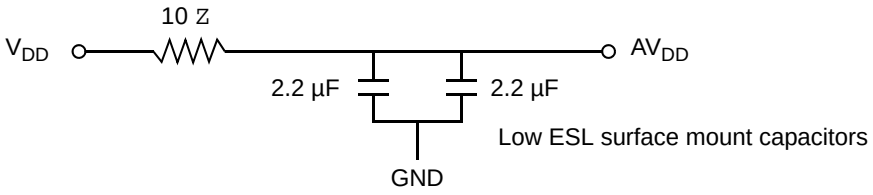


Figure 1. PLL Power Supply Filter Circuit

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is three independent filter circuits, one to each of the three AV_{DD} pins. Providing independent filters to each PLL reduces the opportunity to cause noise injection from one PLL to the other. This circuit is intended to filter noise in the PLL resonant frequency range, from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Each circuit should be placed as closely as possible to the specific AV_{DD} pin supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias. If possible, a separate plane for each PLL filtering circuit is recommended.

3 Clocking

3.1 System Clock

The system clock SYSCLK input is the primary clock source for all Synchronous blocks on the PowerQUICC III and must always be provided. The SYSCLK input is multiplied by a phase-lock loop (PLL) to generate the core complex bus (CCB) clock. The CCB clock is used by the L2 cache, CPM and DMA. It is divided by two to generate the DDR clocks MCK[0:5]. It is divided by 2/4/8 (in the LCRR[CLKDIV] register) to generate local bus clocks LCLK[0:2]. It is also multiplied by a second PLL (by the power-on reset setting LALE, LGPL2) to generate the e500 core clock. As there are no default settings for the two PowerQUICC III PLLs, power-on reset configuration of them within the system design is mandatory.

The PCI interface has two clock modes, Synchronous mode, and Asynchronous mode. The default clock mode (Synchronous) uses the SYSCLK. In Asynchronous mode each PCI (PCI1, PCI2) interface can be configured to use separate PCI clock input unrelated to the SYSCLK input. The PCI clock modes are configured during POR by TSEC2_TXD1, and TSEC2_TXD0 signals. See Figure 2 and Table 3.

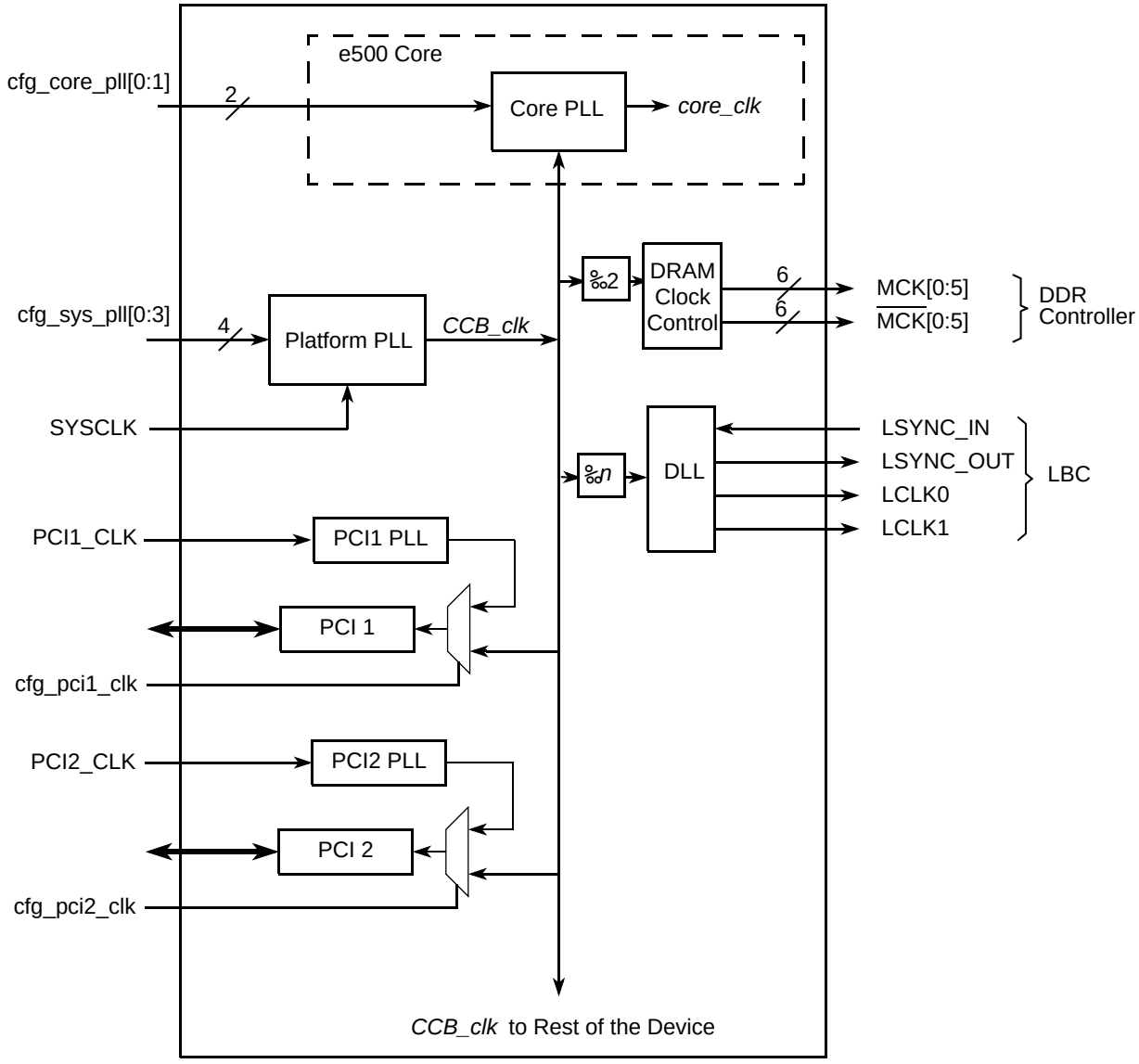


Figure 2. Clock Subsystem Block Diagram

Table 3. Clocking Quick Reference

Functional Block	Clock Derivation
Core (including L1)	CCB [2, 2.5, 3, 3.5]
DDR	CCB / 2
I^2C	CCB / (I2CFDR ratio)
L2 cache, CPM	CCB
Local Bus	CCB / [2,4,8]

Table 3. Clocking Quick Reference (continued)

Functional Block	Clock Derivation
PCI1, PCI2	SYSCLK, or PCI_CLK
TSEC	125MHz from PHY or External (certain modes)

3.2 Clocking Example

Let us assume that we want to maximize the frequencies of certain key interfaces. We can use the following inputs:

- SYSCLK = 66 MHz
- CCB multiplier = 5 (cfg_sys_pll)
- Core multiplier = 2.5 (cfg_core_pll)
- Local bus divider = 2 (LCRR[CLKDIV])

The resulting frequencies for the following interfaces are:

- Core = SYSCLK * cfg_sys_pll * cfg_core_pll = 833 MHz
- CPM = SYSCLK * cfg_sys_pll = 333 MHz
- DDR (MCKn) = SYSCLK * cfg_sys_pll/2 = 167MHz = 333 MHz data rate
- PCI = SYSCLK = 66 MHz
- Local Bus (LCLKn) = SYSCLK * cfg_sys_pll / CLKLDIV = 167 MHz

These are the current maximum frequencies. Check the relevant product web site for updated options.

3.3 Core Clock

The frequency of the core is determined at POR through the LALE and the LGPL2 pins. Below are the options for configuring the core clock as a multiple of the CCB clock. This information can be found in the *MPC8555E PowerQUICC™ III Integrated Communications Processor Reference Manual* (MPC8555ERM).

Table 4. Core Clock POR Configuration

LALE, LGPL2	Core: CCB
00	2:1
01	5:2 (2.5:1)
10	3:1
11	7:2 (3.5:1)

3.4 DDR SDRAM Clock Outputs

The DDR SDRAM clock outputs MCK[0:5] and MCK[0:5] are derived from the CCB clock. No configuration pins or register settings are required to generate the MCK/$\overline{\text{MCK}}$n frequencies because they are by default one-half the CCB clock frequency.

3.5 I^2C Clock

The I^2C clock rate is determined by a ratio set in the I2CFDR register. Refer to the MPC8555ERM.

3.6 L2 Cache and CPM Clocks

The clock rate for the L2 Cache and the CPM is the same as the CCB clock frequency.

3.7 Local Bus Clock Outputs

The local bus clock outputs LCLK[0:2] are derived from the CCB clock. By default the LCLKn frequency is CCB clock frequency divided by eight. However, by appropriately setting the System Clock Divider parameter in the Clock Ratio Register (LCRR[CLKDIV]), the LCLKn frequency can be configured as shown in Table 5.

Table 5. Local Bus Clock Divider Options

LCRR[CLKDIV]	LCLKn Frequency
0010	CCB Clock / 2
0100	CCB Clock / 4
1000 (Default)	CCB Clock / 8
All other values	Reserved

3.8 PCI Clock Input

There are two modes for PCI clock input—synchronous mode and asynchronous mode. In synchronous mode the input clock for the PCI interfaces on the MPC8555E and the MPC8541E is, by default, the system clock (SYSCLK input). In asynchronous mode each PCI (PCI1, PCI2) interface can be configured to use a separate PCI clock input unrelated to the SYSCLK input. The PCI clock mode is configured during POR by TSEC2_TXD1, and TSEC2_TXD0 signals.

3.9 TSEC Reference Clock Input

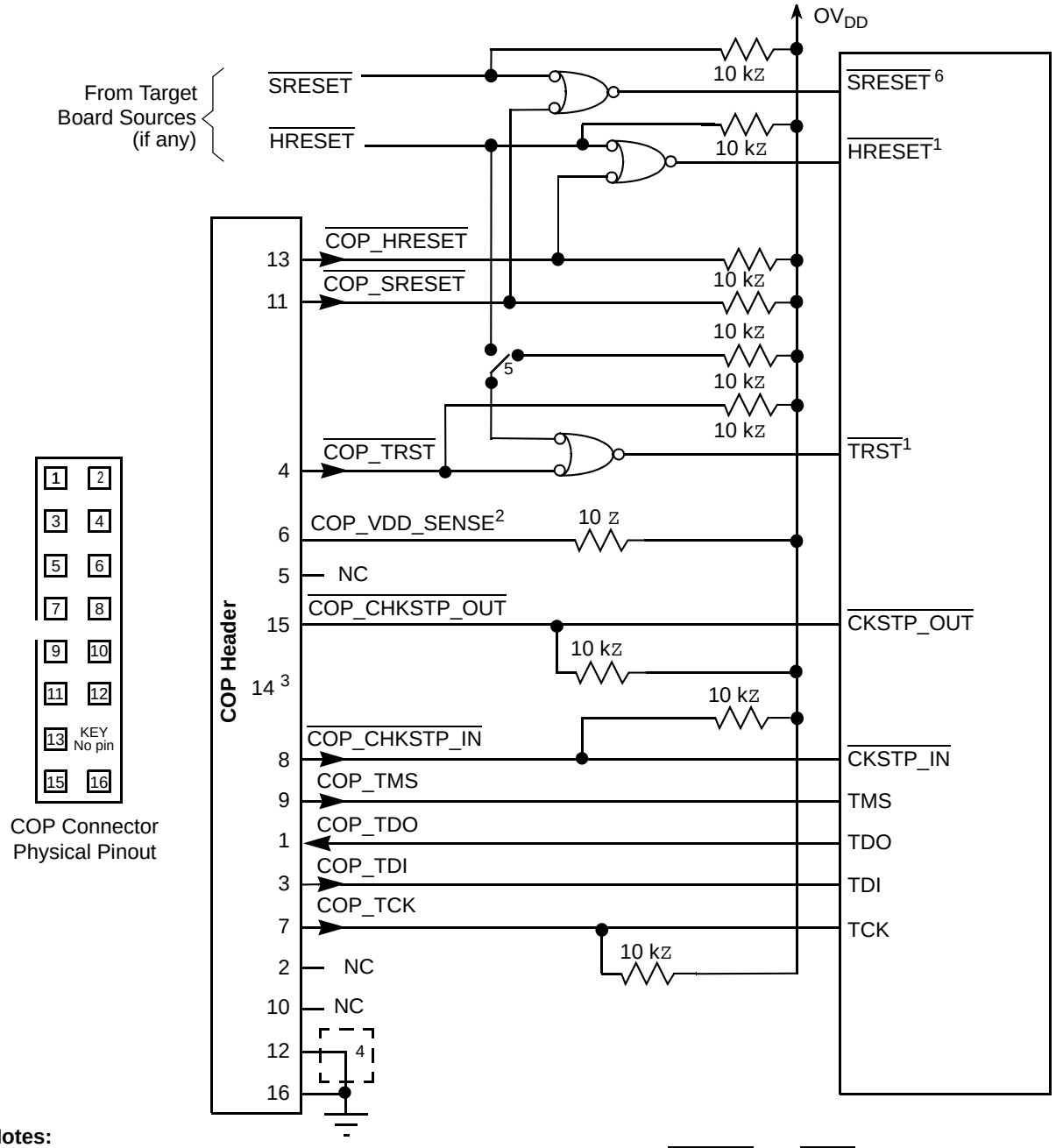
This signal is not used for MII mode. When any other mode is used in the TSEC interface, the gigabit transmit 125 MHz reference clock EC_GTX_CLK125 must be supplied. This signal must be generated externally with a crystal or oscillator, or it can sometimes be provided by the PHY. In GMII, RGMII, RTBI or TBI mode, EC_GTX_CLK125 is a 125 MHz input into the TSEC and is used to generate all 125-MHz-related signals and clocks.

4 Debug

This section describes the PowerQUICC III reset sequence and recommendations for the system.

4.1 TRST

$\overline{\text{TRST}}$ is the reset pin for the JTAG/COP interface. It must be held at a low level during the assertion of $\overline{\text{HRESET}}$ to reset all logic completely on the PowerQUICC III. For compatibility with third-party tools, $\overline{\text{TRST}}$ and $\overline{\text{HRESET}}$ must be able to assert independently (see the example in Figure 3).



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be open during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed or removed.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 3. COP Connections to PowerQUICC III

The COP header is fully described in Figure 4 and Table 6.

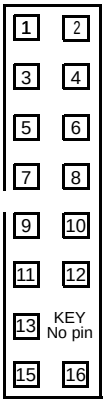


Figure 4. COP Header Pinout

Table 6. COP Header Definition

Header Position	Name	Description
1	COP_TDO	Test Data Output
2	NC	
3	COP_TDI	Test Data Input
4	TRST	Test Reset
5	Not implemented. Connect to OV_{DD} with a 10KΩ resistor.	
6	COP_VDDS	VDD Sense
7	COP_TCK	Test Clock
8	COP_CHKSTP_IN	Checkstop In
9	COP_TMS	Test Mode Select
10	NC	
11	$\overline{\text{COP\_SREST}}$	Soft Reset
12	NC	
13	$\overline{\text{COP\_HRESET}}$	Hard Reset
14	KEY	
15	COP_CHKSTP	Checkstop Out
16	GND	Ground

4.2 Termination of Unused Signals

If the JTAG interface and COP header are not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during

the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 3. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ if a JTAG interface needs to be wired onto the system in future debug situations.

- Tie TCK to OV_{DD} through a 10 kΩ resistor to prevent TCK from changing state and reading incorrect data into the device.
- No connection is required for TDI, TMS, or TDO.

4.3 Recommended Test Points

For easier debug, it is recommended that the test points on the board include the following pins:

- CLK_OUT (This helps to verify the CCB clock)
- TRIG_OUT (This helps to verify the end of the reset sequence)
- ASLEEP (This helps to verify the end of the reset sequence)
- SENSEVDD (This helps to verify power plane V_{DD})
- SENSEVSS (This helps to verify ground plane V_{SS})
- HRESET_REQ (This helps to verify proper boot sequencer functions and reset requests)

5 Power-On Reset/Reset Configurations

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{HRESET}}$. These inputs are either pulled high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{HRESET}}$ is asserted. $\overline{\text{HRESET}}$ must be asserted for a minimum of 100µs. When $\overline{\text{HRESET}}$ negates, the configuration pins are sampled and latched into registers and the pins then take on their normal output circuit characteristic from an input circuit during $\overline{\text{HRESET}}$.

All configuration pins have an internally gated 20 KΩ pull-up resistor, enabled only during $\overline{\text{HRESET}}$. For configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7 KΩ pull-down resistor is recommended to pull the configuration pin to a valid logic-low level. If a configuration pin has no default, 4.7 KΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin. Table 7 summarizes all the power-on reset configurations possible on the device.

Table 7. Power-On Reset Configurations

Type of Configuration	Configuration Pins	Default State
CCB Clock PLL Ratio	LA[28:31]	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
e500 Core PLL Ratio	LALE, LGPL2	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
Boot ROM Location	$\overline{\text{LGPL0}}$, LGPL1, $\overline{\text{LWE}}$[3]	Local Bus GPCM, 32-bit ROM
Host/Agent	$\overline{\text{LWE}}$[2]	Device acts as the host on processor for PCI 1
CPU Boot	LA27	The core is allowed to boot without waiting for configuration from any external master
Boot Sequencer	LGPL3, LGPL5	Boot sequencer is disabled
TSEC Width	EC_MDC	Ethernet interfaces operate in standard GMII or TBI modes

Table 7. Power-On Reset Configurations (continued)

Type of Configuration	Configuration Pins	Default State
TSEC1 Protocol	TSEC2_TXD[3]	TSEC1 operates using the TBI (or RTBI) protocol
TSEC2 Protocol	TSEC2_TXD[2]	TSEC2 operates using the TBI (or RTBI) protocol
PCI1 Clock Select	TSEC2_TXD[1]	SYSCLK is used as default clock for PCI1
PCI2 Clock Select	TSEC2_TXD[0]	SYSCLK is used as default clock for PCI2
PCI 32bit configuration	PCI2_FRAME	PCI interface operates as two 32-bit interface
PCI1 I/O Impedance	PCI1_GNT1	42Z drivers are used on the PCI1 interface
PCI2 I/O Impedance	PCI2_GNT1	42Z drivers are used on the PCI1 interface
PCI1 Arbiter	PCI1_GNT2	PCI1 Arbiter enabled
PCI2 Arbiter	PCI2_GNT2	PCI2 Arbiter enabled
PCI Debug	PCI1_GNT3	PCI operates in normal mode
Memory Debug	MSRCID0	DDR debug information is driven on MSRCID and MDVAL
DDR Debug	MSRCID1	No debug information is driven on the ECC pins
PCI1 Output Hold	PCI1_GNT4	PCI1: Two added buffer delays to meet 2ns hold time (In 64bit PCI mode applies to lower 32bit)
PCI2 Output Hold	PCI2_GNT4	PCI2: Two added buffer delays to meet 2ns hold time (In 64bit PCI mode applies to upper 32bit)
Local Bus Output Hold	$\overline{\text{LWE}}$[0:1]	One added buffer delay
General Purpose POR	LAD[0:31]	No default state; pins must be configured at HRESET if GPPORCR is intended to be accessed by a user system

An alternative to pull-up and pull-down resistors to configure the POR pins is to use a PLD, DIP switch, or similar device to drive the configuration signals when $\overline{\text{HRESET}}$ is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the negation of $\overline{\text{HRESET}}$ (PLL configuration inputs must meet a 100 ms set-up time to $\overline{\text{HRESET}}$), hold their values for at least 2 SYSCLK cycles after the negation of $\overline{\text{HRESET}}$, and tri-state the pins afterwards for normal device operation. For details on the power-on reset configurations and their definitions, refer to the *MPC8555E/MPC8541E PowerQUICC™ III Integrated Communications Processor Reference Manual* (MPC8555ERM).

5.1 Useful System POR Debug Registers

The POR configuration settings can be read in the POR PLL status register (PORPLLSR), the POR boot mode status register (PORBMSR), the POR I/O impedance status and control register (PORIMPSCR), the POR device status register (PORDEVSR), the POR debug mode status register (PODBGMSR), and the general-purpose POR configuration register (GPPORCR). See the MPC8555ERM for details on these registers, which are all read-only registers except for PORIMPSCR.

GPPORCR can be used to pass any information on the local bus address/data pins LAD[0:31] to software. For example, we can pass information about a circuit board revision number to software by driving the pins in any order. The information is automatically sampled from LAD[0:31] during POR. Then software

can read this register at any time and process the data accordingly. There are no default settings for this register. If this feature is not used, it is not necessary to drive the pins high or low.

5.2 Internal Manufacturing Test Modes

A few pins on the PowerQUICC III device have a secondary function of enabling internal manufacturing test modes (see Table 8). These modes are enabled during the HRESET sequence by driving the respective pin to a logic-zero state.

NOTE

If any of these modes are enabled during normal device operation, the device does not come out of reset, and the system hangs.

To avoid accidentally enabling these internal test modes, take care to ensure that these pins are either floating (as they implement an internal weak pull-up resistor) or are pulled high during the reset sequence if they are connected to a device that pulls these pins low. Additional test pins must be pulled up by a resistor connected to OV_{DD} during normal device operation. If any of these pins are pulled low, the system may hang. (Consult the MPC8555EEC or the MPC8541EEC).

Table 8. Internal Test Mode and Debug Pins

Pin	Pin Type	Comment
ASLEEP	Internal test mode	Pull up or leave floating during reset only
L1_TSTCLK	Internal debug	Pull up to OV_{DD}
L2_TSTCLK	Internal debug	Pull up to OV_{DD}
LBCTL	Internal test mode	Pull up or leave floating during reset only
$\overline{\text{LSSD\_MODE}}$	Internal debug	Pull up to OV_{DD}
TRIG_OUT/READY	Internal test mode	Pull up or leave floating during reset only
TSEC1_TXD[0:3]	Internal test mode	Pull up or leave floating during reset only
$\overline{\text{HRESET\_REQ}}$	Internal test mode	Pull up or leave floating during reset only

5.3 Boot Sequencer

The boot sequencer allows configuration of any memory-mapped register before the boot-up code runs. When enabled, it loads code from an EEPROM on the I^2C bus. This code can be used to configure the port interface registers if the device is booting from PCI. The boot sequencer is enabled during power-on reset by the [LGPL3, LGPL5] pins. These two signals can also enable extended boot sequencer mode. Refer to the MPC8555ERM for the complete data format for programming the I^2C EEPROM.

The boot sequencer contains a basic level of error detection. If a preamble or CRC fail is detected, the external HRESET_REQ asserts. The I^2C pins continue to be pulled low during a fail until a hard reset occurs.

The CRC algorithm used by the boot sequencer is as follows:

$$1 + x^1 + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$$

The start value is 0xFFFFFFFF. The final XOR value is 0x00000000.

5.4 Boot Hold-off Mode

The PowerQUICC III can be put into slave mode in a system. An external master on the PCI bus must configure the device. Boot hold-off mode, when enabled during power-on reset, allows any external master on these buses to configure the PowerQUICC III slave device. To enable this mode during power-on reset, use the LA27 pin. During this mode, the core is suspended from fetching boot code. To exit this mode, the EEBPCR[CPU_EN] bit must be set.

6 Functional Blocks

The following sections discuss the recommendations and guidelines for designing with the various functional blocks on PowerQUICC III.

6.1 Global Utilities

The PowerQUICC III provides a global utilities block which controls power management, I/O device enabling, power-on reset configuration monitoring, and other debug functions. Refer to Section 4, “Debug.” The following subsections present information on the device disable register (DEVDISR) and low-power modes.

6.1.1 Device Disable Register (DEVDISR)

After the PowerQUICC III comes out of reset, all functional blocks are enabled. However, if all interfaces of the PowerQUICC III are not used, it would be more power efficient to disable these interfaces. The device disable register (DEVDISR) contains disable bits for the PCI1, PCI2, LBC, SEC, L2, DDR, e500, Time Base, CPM, DMA, TSEC1, TSEC2, I2C, and DUART interface. If desired, the core or an external master can disable these blocks by setting these bits.

When a block is disabled with this register, all clocks are disabled to the block, thereby saving power. However, a result of not having clocks to an interface is that the interface does not respond to any interrupts or accesses. A programming error occurs when the user tries to access configuration or status registers of a block while disabled.

These interfaces cannot be re-enabled without asserting $\overline{\text{HRESET}}$, or the results are be undefined. Disabling the e500 core through this register is equivalent to “nap mode.” This is not recommended since any interface disabled through DEVDISR requires an $\overline{\text{HRESET}}$ to re-enable it. Use the low-power “nap mode” instead.

6.1.2 Low Power Modes

In addition to the device disable register, the PowerQUICC III further allows the user to reduce the power consumption through the low-power modes. There are three low-power modes: doze, nap, and sleep. For details on these modes, consult the relevant device manual. Putting the device into nap mode is equivalent to disabling the e500 core through DEVDISR. However, because you cannot wake up the device using DEVDISR, except through an $\overline{\text{HRESET}}$, it is recommended that nap mode be used instead.

6.2 Core

Multiprocessor functionality is not implemented in the PowerQUICC III e500 core:

- There are no shared (S) states in the L1 or L2 cache.
- The memory coherence bit, M, controlled through MAS2[M] / MAS4[MD] and MAS2[SHAREN] /MAS4[SHAREND], has no effect.
- HID1[MSHARS] and HID1[SSHAR] are not implemented.
- HID1[ABE] is only used to ensure (when set) that cache and TLB management instructions operate properly with respect to the L2 cache.
- There is no dynamic bus snooping. If the PowerQUICC III is in a nap or sleep state, then the core is not wakened to snoop global transactions.

The PowerQUICC III does not implement a double-precision floating point. If this is needed, it can be emulated through software. The PowerQUICC III supports single-precision scalar and single-precision vector floating point only through various APUs on-chip. In addition, 64-bit operands are not supported because the e500 is a 32-bit implementation of Book-E.

The SPE, and SPFP APUs functionality will not be implemented in the next generation of PowerQUICC devices. Freescale strongly recommends that use of these instructions be confined to libraries and device drivers. Customer software that uses SPE or SPFP APU instructions at the assembly level or that uses SPE intrinsics will require rewriting for upward compatibility with next generation PowerQUICC devices. Freescale offers a lib_moto_e500 library that uses SPE and SPFP APU instructions. Freescale will also provide future libraries to support next generation PowerQUICC devices.

6.3 DDR SDRAM

Please refer to the following application notes for detailed information on layout consideration and DDR programming guidelines:

- AN2582*: Hardware and Layout Design Considerations for DDR Memory Interfaces* for details on signal integrity and layout considerations.
- AN2583*: Programming the PowerQUICC III™ DDR SDRAM Controller* on DDR programming guidelines.

The DDR bus should not be configured during use. Rather, it should be configured by executing code from another interface (i.e., Local Bus).

NOTE

- In the DDR controller of the MPC8555E and MPC8541, only the source synchronous mode is supported. For proper operation, the external signals MSYNC_IN and MSYNC_OUT should be connected to each other.
- The source synchronous mode bit field must be set during initilization: DDR_SDRAM_CLK_CNTL[SS_EN] = 1

6.3.1 Termination of DDR Signals During Normal Operation

Parallel termination is optional for DDR signals and should be simulated to verify necessity. Differential termination is included on DIMM. It is required only for discrete memory applications. For details on termination schemes, see application note *Hardware and Layout Design Considerations for DDR Memory Interfaces* (AN2582). It is strongly recommended that with any termination scheme, signal integrity analysis be performed using the respective device IBIS model.

6.3.2 Termination of Unused DDR Signals

Termination is not needed on output signals. For I/Os, tie signals high or low through a resistor. Recommended resistor values are 2–10 kΩ. For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low. Recommended resistor values are 2–10 kΩ.

6.4 I^2C Unit

6.4.1 Termination of Signals during Normal Operation

Tie both SDA and SCL high through a 1 kΩ resistor.

6.4.2 Termination of Unused Signals

When this interface is not used, you should individually tie the signals high through a resistor. Recommended resistor values are 2–10 kΩ.

6.5 Local Bus Interface Unit

The local bus frequency can be adjusted through the LCRR[CLKDIV] bit. If modified, the DLL requires a re-lock time prior to use. The lock time can vary between ~7680 to 122880 CCB clock cycles. It is a ratio between the LBC clock and the CCB clock. The 2:1 ratio corresponds to the minimum lock time and the 8:1 ratio corresponds to the maximum lock time.

The PowerQUICC III features adjustable drive strengths for the local bus. The PORIMPSCR register configures most local bus signals to either 25 or 42 Ω. This configurable drive strength can help improve signal integrity by helping match the load on the I/O. For applications with heavy loading on the bus, we recommend the stronger drive strength of 25 Ω 1If there is light loading on the bus, we recommend the weaker drive strength of 42 Ω. A driver/I/O impedance mismatch can cause noise issues on the signal. The decision of which driver to use should be based on signal integrity analysis with the available IBIS models.

The local bus clock should not be reconfigured while executing from the local bus, but rather by executing code from another interface such as DDR. The PowerQUICC III local bus features a multiplexed address and data bus, LAD[0:31]. An external latch is required to de-multiplex these signals to the connecting device.

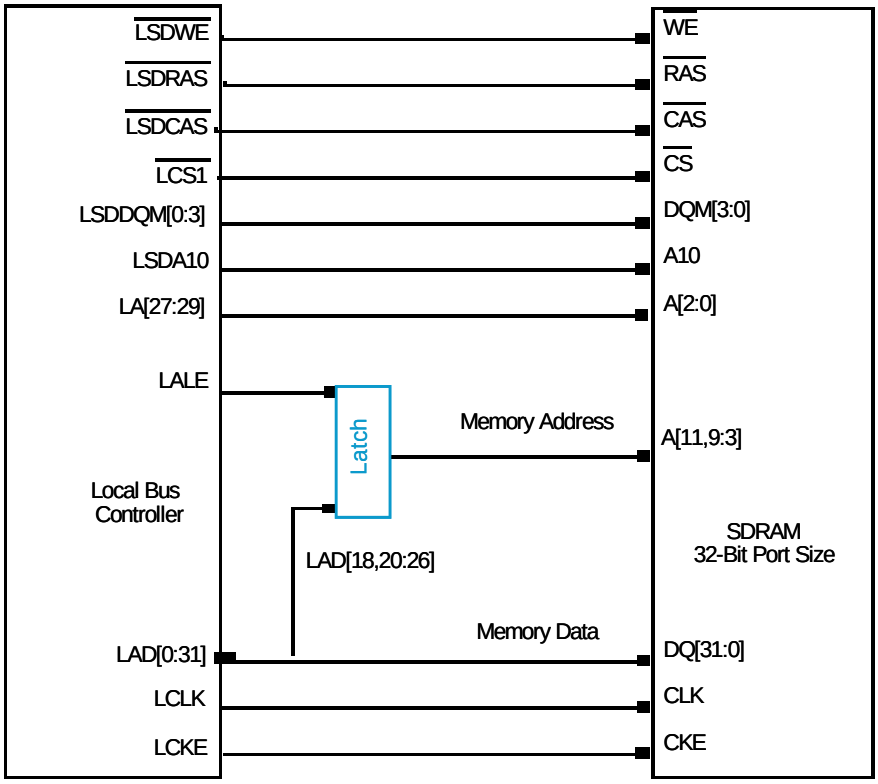


Figure 5. Local Bus Connection to SDRAM

6.5.1 Termination of Signals During Normal Operation

You should verify signal integrity by simulating with the current IBIS model. A weak pull-up (2–10 KΩ) is required on /LGTA signal.

6.5.2 Termination of Unused Signals

Termination is not needed on output signals. For bidirectional I/Os, tie signals high or low though a resistor. Recommended resistor values are 2–10 KΩ. For inputs, tie signals to their inactive state through a resistor. Recommended resistor values are 2–10 KΩ.

6.5.3 Timing

Local bus output valid, hold, and tri-state timings can be adjusted at reset by the POR pins TSEC2_TXD[6:5]. These pins directly affect local bus AC-timing by adding up to three buffer delays to the output path. The default configuration is a single buffer delay. Fewer buffer delays are needed in cases where the connection is to a faster external device.

For address latch hold time t_{LBOTOT}, the LBCR[AHD] bit is used to further adjust t_{LBOTOT}. It removes part of the hold time for LAD with respect to LALE to lengthen the LALE pulse. It can remove either a half or a full CCB clock period. Table 9 shows how t_{LBOTOT} is programmed.

Table 9. Programming t_{LBOTOT}

LBCR[AHD]	TSEC2_TXD[6:5]	t_{LBOTOT}
0	00	CCBCLK
0	01	CCBCLK + 3BDs
0	10	CCBCLK + 2BDs
0	11	CCBCLK + 1BD
1	00	CCBCLK/2
1	01	CCBCLK/2 + 3BDs
1	10	CCBCLK/2 + 2BDs
1	11	CCBCLK/2 + 1BD

6.6 PCI

6.6.1 Termination of Signals during Normal Operation

You should verify signal integrity by simulating with the current IBIS model. For standard operation of the PCI port, pull-ups are necessary to guarantee the state of control signals when no agent is driving the bus. The *PCI Local Bus Specification* requires a pull-up on the PCI1_FRAME, PCI1_TRDY, PCI1_IRDY, PCI2_TRDY, PCI2_IRDY, PCI1_DEVSEL, PCI1_STOP, PCI1_SERR, PCI1_PERR, PCI2_STOP, PCI2_SERR, PCI2_PERR,PCI1_REQ64, and PCI1_ACK64 pins. Weak pull-ups of 2–10 KΩ are recommended for these pins.

When in 32-bit PCI mode, the PowerQUICC III enables weak internal pull-ups on PCI1_AD[63:32], PCI_C_BE[7:4], and PCI1_PAR64. These internal pull-ups are not enabled in 64-bit mode. If there is concern that in 32-bit mode these inputs may see noise that would cause unwanted power consumption, then external pull-up resistors can be placed on them to further guarantee their logic-one state when in 32-bit mode.

The PCI1_REQ64 pin functionally requires a pull-up resistor per the *PCI Local Bus Specification*; however, during reset it is a configuration input for PowerQUICC III that determines 32- or 64-bit PCI operation. If the PowerQUICC III is to be configured as a 64-bit PCI device, it must be actively driven low during reset by reset logic. Because PowerQUICC III does not implement an override to this specified protocol for selecting 64-bit operation, the signal would have to be driven low with a tri-stateable driver or similar logic during reset and then released to select 64-bit PCI operation.

If the PowerQUICC III is the host that initiates PCI transactions, you should pull the IDSEL pin low to guard against the PowerQUICC III replying to one of its own bus transactions.

6.6.2 Termination of Unused Signals

Termination is not needed on output signals. For bidirectional I/Os, tie signals high or low though a resistor. Recommended resistor values are 2–10 KΩ. If the PCI arbiter is disabled by the power-on reset configuration settings, these signals can be tied together to a common resistor. If the PCI interface is used in 32-bit mode, PCI1_AD[63:32] should be left floating. No termination is needed.

For inputs, tie signals to their inactive state through a resistor. Recommended resistor values are 2–10 KΩ.

6.6.3 Specific Pin Usage

The PowerQUICC III does not implement for the PCI interface specific CLK and $\overline{\text{RST}}$ pins separately from the rest of the device pins. Instead, the PCI CLK is realized on the SYSCLK input, and the PCI $\overline{\text{RST}}$ is realized on the $\overline{\text{HRESET}}$ input.

6.7 Three Speed Ethernet Controller (TSEC)

The TSEC has one management interface that controls all external PHYs. The management interface of TSEC1 controls the TBI PHY from TSEC1 as well as all external PHYs. The management interface of TSEC2, shown in Figure 6, controls the TBI PHY from TSEC2 only.

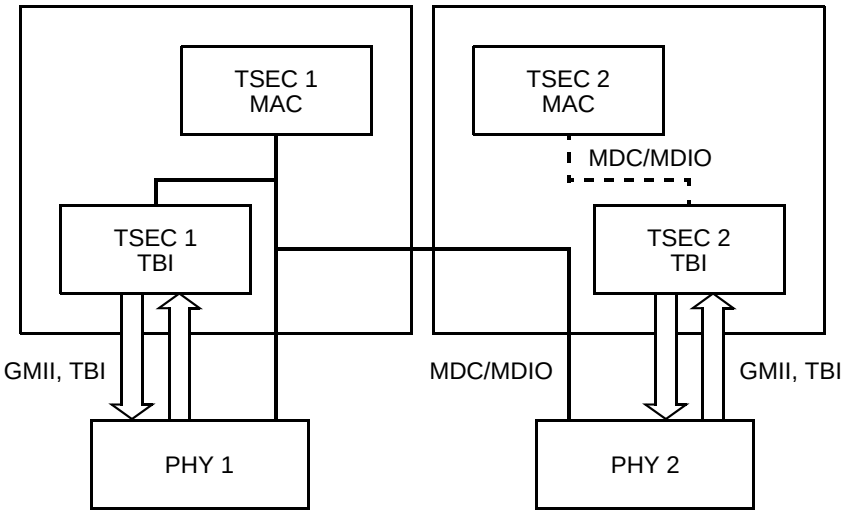


Figure 6. TSEC Management Interface

6.7.1 Graceful Stop

The TSEC interfaces must be properly stopped by the graceful stop mechanism. Stopping the transmit and receive buffers without using graceful stop can yield unpredictable results. The processor must first gracefully stop the transmitter by setting the DMACTL[GTS] bit and confirming that it has completed by polling the IEVENT [GTSC] bit. Only then should the transmitter be disabled by clearing the MACCFG1[TxEN] bit.

For the TSEC receive, first turn off the receiver to prevent any additional data from coming in. Then the graceful stop should be enabled by setting the DMACTL[GRS] bit. Wait for confirmation by polling the IEVENT[GRSC] bit.

6.7.2 Termination of TSEC Signals During Normal Operation

It is recommended that the signal integrity be verify by simulating with the current IBIS model.

6.7.3 Termination of Unused TSEC Signals

Termination is not needed on output signals. For I/Os, tie signals high or low through a resistor. Recommended resistor values are 2–10 KΩ. For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low. Recommended resistor values are 2–10 KΩ.

6.8 Termination Summary for Unused Signals

Table 10 summarizes the recommended terminations for unused interfaces or unused pins. Termination is not needed on outputs, only inputs. Suggested resistor values are between 2–10 KΩ. In general, inputs can be tied together to a single resistor. I/Os must be tied off with a single resistor per I/O except on the PCI interface (see Section 6.6, “PCI”).

Note that if you are not using the local bus or the TSEC, must still configure the appropriate power-on reset signals for these interfaces. However, these particular power-on reset pull-ups and pull-downs can be left alone during normal operation because the interfaces are not used.

Table 10. Termination of Unused Signals Summary

Block	Termination Needed on Unused Inputs	Exceptions
CPM	If Port A-D pins are not re-programmed as outputs, then: • Tie I/Os high or low through resistor • Tie inputs to inactive state through resistor	—
DDR	Tie pins high or low through resistor	—
I^2C	Tie pins high through resistor	—
PCI	Tie I/Os high or low through resistor Tie inputs to inactive state through resistor	POR pins $\overline{\text{PCI1\_GNT[1:4]}}$, $\overline{\text{PCI2\_GNT[1:4]}}$ and $\overline{\text{PCI1\_REQ64}}$
TSEC	Tie I/Oshigh or low through resistor Tie inputs to inactive state through resistor	POR pins TSEC1_TXD[4:7], TSEC2_TXD[2:7]; manufacturing test pins TSEC1_TXD[0:3]
Local Bus	Tie I/Os high or low through resistor Tie inputs to inactive state through resistor	POR pins LA[27:31], LALE, LGPL[0:3], LGPL5, LWE[0:3]

7 Revision History

Table 11 provides a revision history for this application note.

Table 11. Document Revision History

Rev. Number	Date	Changes
5	05/2013	Changed “.....minimum of 100ms” to “.....minimum of 100µs” in Section 5, “Power-On Reset/Reset Configurations
4	06/2010	Added a NOTE to Section 2.3, “Power Sequencing.”
3	11/2006	Made updates to bring this application note in line with the hardware specification updates. Changes are summarized as follows: • Section 4.1, “TRST, “ replaced Figure 3 and added section on Section 4.2, “Termination of Unused Signals. • Modified Section 2.3, “Power Sequencing.” • Modified signal names in Table 6.
2	6/2006	Updates are as follows: • Modified note in Section 6.3, “DDR SDRAM” to clarify that while MSYNC_IN mube connected to MSYNC_OUT, the length of this trace need not be matched to anything because the operating mode is Source Synchrounous mode. • Section 2.2, removed Table 2. • Section 3.1. Removed the current Figure 2 and replaced it with Figure 4-6 from the MPC8555E reference manual. • Section 6.3. Added a bullet to the note section. • Section 6.5.1. Added the following line: “A weak pull-up (2–10 K Z) is required on the LGTA signal. • Removed and replaced Figure 3 with the MPC8560EC hardware specification Figure 59.
0.1	12/2004	Deleted sentence from Section 6.5.1
0	10/2004	Initial Release

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