Application Note

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Configuring the System and Peripheral Clocks in the MC9S08GB/GT

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Introduction

This application note addresses the features and usage of the internal clock generator (ICG) module residing in the MC9S08GB/GT Family of microcontrollers. It will describe initialization and usage in its various modes of operation and address clock configurations for the MCU peripherals.

Features of the ICG Module

The ICG module provides the system clock to the MC9S08GB/GT microcontroller. **Figure 1** is a block diagram showing a functional view of the ICG module. This module provides multiple selections for system clock sources, allowing the user to choose among system cost, precision, and performance needs. The module consists of four major functional blocks:

- Oscillator block
- Internal reference generator (IRG)
- Frequency-locked loop (FLL)
- Clock select block

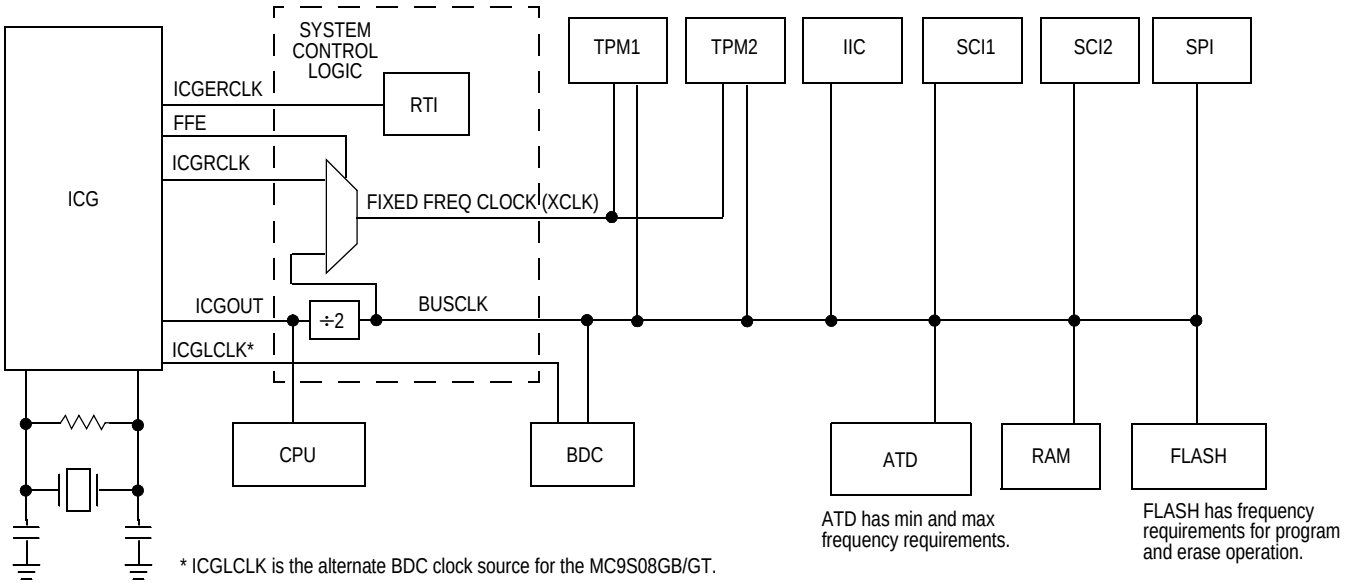


Figure 1. System Clocks Block Diagram

The ICG provides three separate clock output signals:

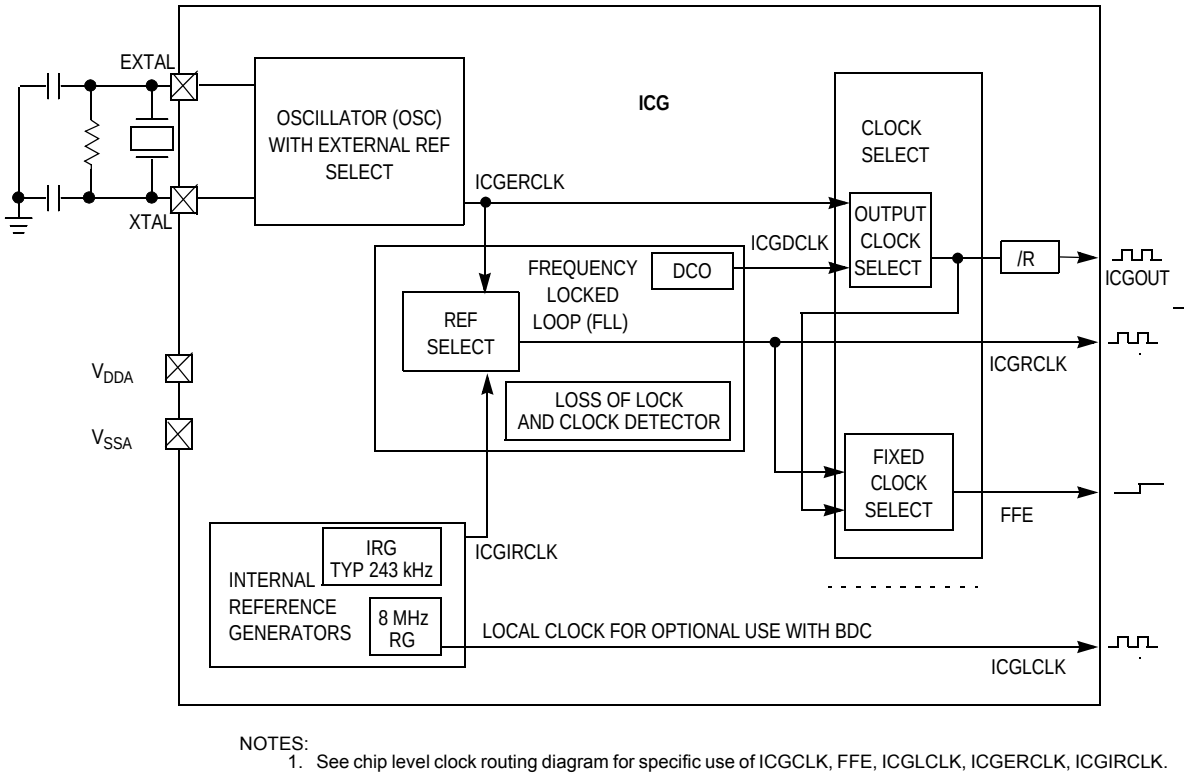
- ICGOUT — The main CPU clock which is divided by 2 to create the bus clock
- ICGRCLK — The reference clock for the FLL; is available for use with certain peripherals under certain conditions
- ICGLCLK — An optional clock source for the background debug controller (BDC); is fixed at 8 MHz, ±30%

Modes of the ICG

The ICG has five modes of operation

- Off
- Self-clocked mode (SCM)
- FLL engaged-internal reference (FEI)
- FLL bypassed-external reference (FBE)
- FLL engaged-external reference (FEE)

Figure 2 is a top-level diagram that shows the functional organization of the internal clock generation (ICG) module.



NOTES:
1. See chip level clock routing diagram for specific use of ICGCLK, FFE, ICGLCLK, ICGERCLK, ICGIRCLK.

Figure 2. ICG Block Diagram

Mode 1: Off

Mode 1, off, is the powered-down state of the ICG. The output clock, ICGOUT, is held in a static or stopped state. This mode is entered when a STOP instruction is executed, and it is exited upon waking up from stop. **Figure 3** shows the stop mode recovery states of the ICG.

In the case of stop1 and stop2 modes, off mode is exited directly into SCM. In the case of stop3, if a reset is used to exit stop, SCM is entered. If an interrupt is used to exit stop3, SCM is entered unless FBE mode was selected prior to entering stop mode. If FBE was selected, the ICG module will hold ICGOUT static until the external clock source is stable. If FEI or FEE was selected upon entering stop3, then SCM is entered with the frequency retained from the pre-stop settings. Then the desired mode is entered when the FLL is stable.

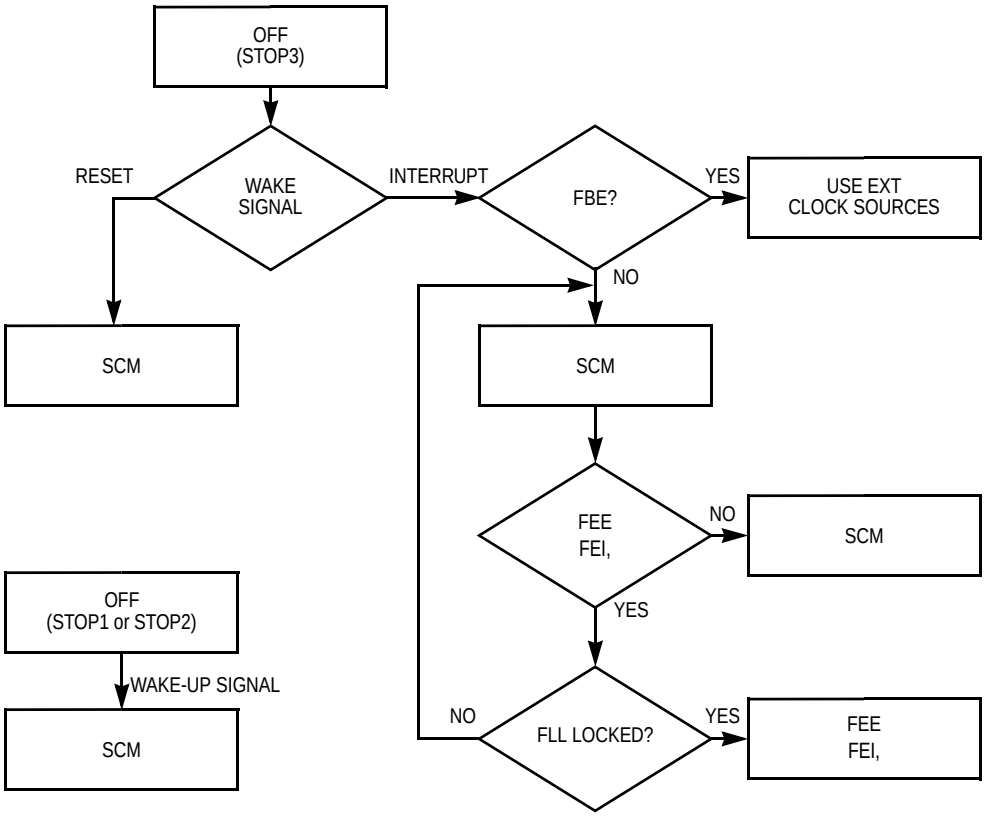


Figure 3. Stop Mode Recovery

Mode 2: Self-Clocked Mode (SCM)

Mode 2, SCM, is the self-clocked default mode. In this mode, the FLL loop is opened and the digitally controlled oscillator (DCO) is used as a stand-alone clock source. ICGOUT will be clocked at approximately 8 MHz, yielding a bus clock of approximately 4 MHz. No external oscillator components are required for this mode.

SCM is the ICG default mode of operation from reset. This mode requires no software intervention or external components to control the ICG. It enables the normal use of I/O port G bits 1 and 2, as there is no requirement for connections to XTAL or EXTAL. Use of this mode is limited to systems where timing requirements are very flexible.

SCM is entered when any of the following four conditions occur:

- After any reset.
- Exiting stop mode if CLKS bits in the ICG control register are not equal to 10. If CLKS bits = x1, the ICG will temporarily enter this state until the DCO becomes stable.
- CLKS bits are written from x1 to 00.
- CLKS bits = x1 and the external reference clock is not detected (ICGERCLK). In other words, the external reference clock is not stable or its frequency is too low and the external clock is lost.

The frequency of the ICG will be approximately 8 MHz. This ICGOUT frequency can be varied from 8 MHz to 40 MHz by writing a new value into the ICG filter registers (ICGFLTU:ICGFLTL). The value and frequency are related in direct proportion to each other. Only during SCM can the filter registers be written. In all other modes, the filter registers are read-only.

Mode 3: FLL Engaged-Internal Reference (FEI)

Mode 3, FEI, is used to provide MCU frequencies that are programmable multiples of the 243-kHz internal reference clock (ICGIRCLK). No external oscillator components are required for this mode.

To construct an inexpensive, but very functional, system from an ICG point of view, the designer can elect to use mode 3, internal self-clocked mode. There are advantages and disadvantages when using this mode of operation.

The main advantage of this mode is that the system requires no external oscillator components. Also, using mode 3 frees the XTAL and EXTAL pins normally associated with the external oscillator to be used as general-purpose I/O. Another advantage of using this internal oscillator is that it starts up very quickly at power-up time or upon recovery from a STOP instruction. Mode 3 uses the FLL to create frequencies programmable in multiples of the internal 243-kHz reference clock.

The disadvantage of using this mode is the initial accuracy of the internal reference generator. It can vary as much as ±25%, however it can be trimmed by user software. When using the ICG in untrimmed self-clocked mode, the MCU is limited to 75% of the maximum 20 MHz bus frequency. This is because at the worst case untrimmed internal reference, you would not want to clock the MCU faster than the maximum specified bus frequency.

Trimming the internal reference generator is beyond the scope of this document and will be discussed in another application note, Freescale document number AN2496/D: *Calibrating the MC9S08GB/GT Internal Clock Generator (ICG)*. Suffice to say, the internal oscillator can be trimmed to ±25% by writing an 8-bit value to the ICG trim register. By using a known timing reference input to the microcontroller and user software, the internal reference oscillator can be accurately calibrated with a resolution of approximately 0.2%.

Trimming the internal reference generator has two major advantages. First, it allows the system to be clocked at its maximum bus rate. Second, it enables an accurate system clock for timer usage as well as an accurate bit-rate generator for the MCU's serial communications interface.

Mode 4: FLL Bypassed-External Reference (FBE)

Mode 4, FBE, uses the external clock source (crystal/resonator/square wave) directly as the MCU clock source. The FLL is powered off in this mode.

Modes 4 and 5 require either a crystal/resonator or an external square wave as the clock source. If the system uses a crystal/resonator, the configuration will be as shown in **Figure 4**. If the system uses an external square wave clock source, input to the ICG is only through the EXTAL pin. In this configuration, a square wave clock will free the XTAL pin for general-purpose I/O use.

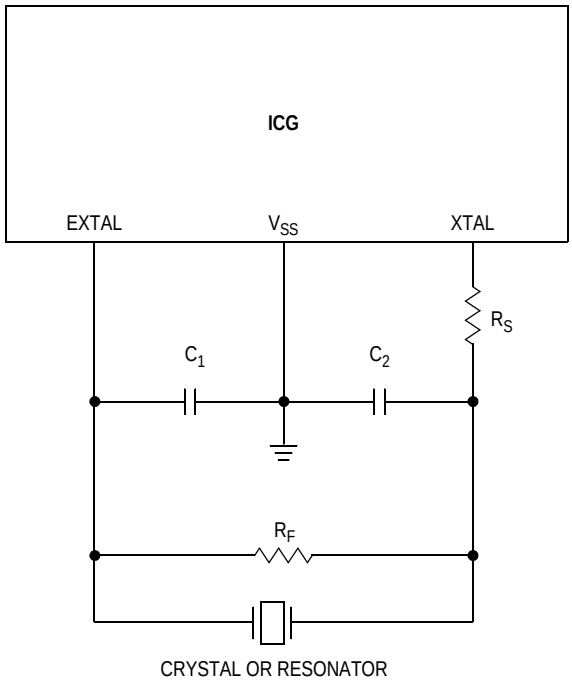


Figure 4. Crystal/Resonator Connections

Mode 5: FLL Engaged-External Reference (FEE)

In mode 5, FEE, the FLL is used to generate MCU frequencies that are programmable multiples of the external clock reference (crystal/resonator/square wave). An external clock source must be present as described in FBE mode.

One advantage of using mode 5 is having a very accurate reference clock source and still having the flexibility of a programmable FLL. Another

advantage is that during a stop recovery event, the ICG will run in SCM until the external reference is stable. This provides a quick wakeup from stop.

The disadvantages of using mode 5 are the added expense of external components and that two I/O port pins are lost to the external clock circuit.

Software Configuration

This section will discuss in detail initialization of the ICG in its various modes of operation. There is commonality in the requirements for software initialization in modes 3, 4, and 5. In the discussion of these modes, there will be some duplication of text, but each explanation will stand on its own to eliminate reading several sections to use any given mode.

Configuring Off Mode (Mode 1)

Off mode is a special case, as it deals with stop mode. With two exceptions, all ICG clock activity will cease during this mode. The exceptions where clock activity continues during stop are:

- When the background debug controller (BDC) is active, the ICG will continue to run as it was before the STOP instruction was executed. This allows access to memory and registers through the BDC.
- If the oscillator is enabled in stop mode (OSCSTEN = 1 in the ICG control register 1). In this case, the external oscillator continues to run, but the clock that was fed to the MCU is turned off. These options are provided to avoid long external oscillator start-up times when the system requires a quick wakeup from stop3 mode.

Another special case is recovery from stop mode. There are two ways to exit stop mode:

- If stop3 mode is exited due to an interrupt, the control bits for the ICG will be valid as they were before entering stop3. System clock feed will resume. If the FFL engaged-external (FEE, mode 5) is selected, the ICG will source the internal reference clock at the pre-stop frequency until the external clock is stable. If the FFL bypassed-external (FBE, mode 4) is selected, the ICG will wait until the external clock is stable before enabling CLKOUT.
- If stop mode is exited due to a reset, previous control bits will be ignored and default reset values will be applied to the ICG control registers. The ICG will exit stop mode in SCM (mode 2), with a bus clock at approximately 4 MHz.

Configuring SCM (Mode 2)

SCM (mode 2) is the default operating mode at system reset and requires no software intervention. In SCM, the FLL is opened and the clock is provided directly by the DCO. The frequency can be modified through software from approximately 8 MHz up to approximately 40 MHz by writing a new FLT value to the ICG filter registers (ICGFLTU, ICGFLTL), which are writable only while in SCM. Writing a higher value will result in a higher frequency.

In addition to the FLT value, the frequency can be modified by the reduced frequency divider (RFD) value in the ICG control 2 register (ICGC2). This 3-bit value divides the ICG output by a factor equal to 2^{RFD}.

The ICG trim register has no effect in this mode. The multiplication factor also has no effect. Therefore the ICGOUT frequency will be:

$$f_{ICGOUT} = f_{ICGDCLK} \div 2^{RFD}$$

Where $f_{ICGDCLK}$ is the output of the DCO.

The bus clock will be the ICGOUT frequency divided by 2.

This ability to write a new FLT value can be useful when recovering from stop2 mode when using FEI or FEE modes. Since stop2 automatically recovers into SCM, if the FLT value is read and saved into RAM before entering stop2, then when the MCU wakes from stop2 and begins code execution in SCM, the user can write the saved value of FLT from RAM back into the ICGFLTx registers. This should result in a faster FLL lock time.

Configuring FEI Mode (Mode 3)

FLL engaged-internal clock mode uses the internal 243-kHz oscillator as a reference and multiplies it with the frequency-locked loop (FLL) to create the MCU's bus clock. The bus clock will be a programmable multiple of the internal 243-kHz reference oscillator. No external oscillator components are required for this mode, freeing port bits 1 and 2 for general-purpose I/O use.

Recall, the bus clock will be the ICGOUT frequency divided by 2.

See **Configuring FEE Mode (Mode 5)** for complete FLL programming guidelines.

Configuring FBE Mode (Mode 4)

FLL bypassed-external clock mode uses the external clock (crystal/resonator/square wave) as the MCU's clock source. If a square wave input is used as the clock source, it can run at any frequency from dc to 40 MHz. If a crystal or ceramic resonator is used as the clock source, it must either be in the low range (32 kHz to 100 kHz) or the high range (1 MHz to 16 MHz).

FBE mode does not use the frequency-locked loop. The frequency can still be modified by the reduced frequency divider (RFD) value in the ICG control 2 register (ICGC2). This 3-bit value divides the ICG output by a factor equal to 2^{RFD}.

The ICG trim register has no effect in this mode. The multiplication factor also has no effect.

Therefore the ICGOUT frequency will be:

$f_{ICGOUT} = f_{EXTCLK} \div 2^{RFD}$

Where f_{EXTCLK} is the frequency of the external clock source.

Recall, the bus clock will be the ICGOUT frequency divided by 2.

Configuring FEE Mode (Mode 5)

FLL engaged-external clock mode uses an external clock (crystal/resonator/square wave) as the MCU's reference clock source. FEE mode uses the frequency-locked loop to multiply the reference clock source to a desired value selected by the MFD and RFD bits in the ICGC2 register. To use FEE mode, there must be an external clock source in the 32 kHz to 100 kHz range or the 2 MHz to 10 MHz range.

When using an IGC mode in which the FLL is engaged (modes 3 and 5), the bus frequency will be some multiple of the reference clock. The reference clock can be the internal 243-kHz reference, an external crystal, resonator, or square wave.

In mode 3, the reference clock is the internal 243-kHz reference. The bus frequency will follow the formula:

$$f_{IRG} = 243 \text{ kHz}$$

$$N = 4, 6, 8, 10, 12, 14, 16, \text{ or } 18$$

$$R = 1, 2, 4, 8, 16, 32, 64, \text{ or } 128$$

$$\text{Bus frequency} = ((f_{IRG} \div 7) \times 64 \times N \div R) \div 2$$

An example for mode 3 (with a desired a bus frequency of 8.8869 MHz) that solves the formula for mode 3 and chooses from the available N and R constants, we would use N = 16 and R = 2.

$$\text{Bus frequency} = 8.8869 \text{ MHz} = ((243 \text{ kHz} \div 7) \times 64 \times 16 \div 2) \div 2$$

In mode 5, the reference clock will be a crystal/resonator/square wave. The bus frequency will follow one of two formulas, depending on the frequency of the reference. Note, when using low-frequency crystals, the RANGE bit in ICGC1 must be set to 0. If the applied reference frequency is between 32 kHz and 100 kHz, the following formula applies:

$$f_{ext} \text{ 32 kHz to 100 kHz}$$

$$N = 4, 6, 8, 10, 12, 14, 16, \text{ or } 18$$

$$R = 1, 2, 4, 8, 16, 32, 64, \text{ or } 128$$

P = 64

Bus frequency = ($f_{IRG} \times P \times N \div R$) ÷ 2

For example, for mode 5, using a 32.768-kHz external reference frequency, if we desire a bus frequency of 8.3886 MHz, solving the formula for mode 5, choosing from the available N and R constants, we would use N = 18 and R = 2.

Bus frequency = 8.3886 MHz = (32.768 kHz * 64 * 16 / 2) / 2

The second formula for mode 5 is based on an external reference frequency in the range of 2 MHz to 10 MHz. Note, when using higher-frequency crystals, the RANGE bit in ICGC1 must be set to 1. The following formula applies:

f_{ext} 2 MHz to 10 MHz

N = 4, 6, 8, 10, 12, 14, 16, or 18

R = 1, 2, 4, 8, 16, 32, 64, or 128

P = 1

Bus frequency = ($f_{IRG} \times P \times N \div R$) ÷ 2

An example for mode 5, using a 4.00 MHz external reference frequency, if we desire a bus frequency of 20.0 MHz, solving the formula for mode 5, choosing from the available N and R constants, we would use N = 10 and R = 1.

Bus frequency = 20.00 MHz = (4.00 MHz × 1 × 10 ÷ 1) ÷ 2

The data sheet for the MC9S08GB/GT devices has some excellent examples for setting the various control registers in the ICG section.

Table 1 illustrates various bus frequencies available when using the internal 243-kHz, external 32.768-kHz, 4.00-MHz, and 8.00-MHz reference frequencies as examples. Note that there are frequency entries listed as out of spec. The output frequency of the DCO is limited to 40 MHz. Therefore, the product of the reference frequency times the multiplier (MFD) must be limited to less than or equal to 40 MHz.

As an example from Table 1, for a 4.00-MHz reference frequency with a multiplier of 12 (MFD = 100), the resulting DCO frequency will be (4.00 MHz × 12) 48 MHz, which exceeds the 40-MHz DCO specification.

Table 1. Bus Frequency Examples (Sheet 1 of 3)

								FEI	FEE		
								CLKS1 = 0	= 1	= 1	= 1
								CLKS0 = 1	= 1	= 1	= 1
MFD			RFD			MFD	RFD	Range = X	= 0	= 1	= 1
2	1	0	2	1	0	Multiplier (N)	Divisor (R)	243 kHz	32.768 kHz	4.00 MHz	8.00 MHz
0	0	0	1	1	1	4	128	0.03 MHz	0.03 MHz	0.06 MHz	0.13 MHz
0	0	1	1	1	1	6	128	0.05 MHz	0.05 MHz	0.09 MHz	Out of spec
0	0	0	1	1	0	4	64	0.07 MHz	0.07 MHz	0.13 MHz	0.25 MHz
0	1	0	1	1	1	8	128	0.07 MHz	0.07 MHz	0.13 MHz	Out of spec
0	1	1	1	1	1	10	128	0.09 MHz	0.08 MHz	0.16 MHz	Out of spec
0	0	1	1	1	0	6	64	0.10 MHz	0.10 MHz	0.19 MHz	Out of spec
1	0	0	1	1	1	12	128	0.10 MHz	0.10 MHz	Out of spec	Out of spec
1	0	1	1	1	1	14	128	0.12 MHz	0.11 MHz	Out of spec	Out of spec
0	0	0	1	0	1	4	32	0.14 MHz	0.13 MHz	0.25 MHz	0.50 MHz
0	1	0	1	1	0	8	64	0.14 MHz	0.13 MHz	0.25 MHz	Out of spec
1	1	0	1	1	1	16	128	0.14 MHz	0.13 MHz	Out of spec	Out of spec
1	1	1	1	1	1	18	128	0.16 MHz	0.15 MHz	Out of spec	Out of spec
0	1	1	1	1	0	10	64	0.17 MHz	0.16 MHz	0.31 MHz	Out of spec
0	0	1	1	0	1	6	32	0.21 MHz	0.20 MHz	0.38 MHz	Out of spec
1	0	0	1	1	0	12	64	0.21 MHz	0.20 MHz	Out of spec	Out of spec
1	0	1	1	1	0	14	64	0.24 MHz	0.23 MHz	Out of spec	Out of spec
0	0	0	1	0	0	4	16	0.28 MHz	0.26 MHz	0.50 MHz	1.00 MHz
0	1	0	1	0	1	8	32	0.28 MHz	0.26 MHz	0.50 MHz	Out of spec
1	1	0	1	1	0	16	64	0.28 MHz	0.26 MHz	Out of spec	Out of spec
1	1	1	1	1	0	18	64	0.31 MHz	0.29 MHz	Out of spec	Out of spec
0	1	1	1	0	1	10	32	0.35 MHz	0.33 MHz	0.63 MHz	Out of spec
0	0	1	1	0	0	6	16	0.42 MHz	0.39 MHz	0.75 MHz	Out of spec
1	0	0	1	0	1	12	32	0.42 MHz	0.39 MHz	Out of spec	Out of spec
1	0	1	1	0	1	14	32	0.49 MHz	0.46 MHz	Out of spec	Out of spec

Table 1. Bus Frequency Examples (Sheet 2 of 3)

								FEI	FEE		
								CLKS1 = 0	= 1	= 1	= 1
								CLKS0 = 1	= 1	= 1	= 1
MFD			RFD			MFD	RFD	Range = X	= 0	= 1	= 1
2	1	0	2	1	0	Multiplier (N)	Divisor (R)	243 kHz	32.768 kHz	4.00 MHz	8.00 MHz
0	0	0	0	1	1	4	8	0.56 MHz	0.52 MHz	1.00 MHz	2.00 MHz
0	1	0	1	0	0	8	16	0.56 MHz	0.52 MHz	1.00 MHz	Out of spec
1	1	0	1	0	1	16	32	0.56 MHz	0.52 MHz	Out of spec	Out of spec
1	1	1	1	0	1	18	32	0.62 MHz	0.59 MHz	Out of spec	Out of spec
0	1	1	1	0	0	10	16	0.69 MHz	0.66 MHz	1.25 MHz	Out of spec
0	0	1	0	1	1	6	8	0.83 MHz	0.79 MHz	1.50 MHz	Out of spec
1	0	0	1	0	0	12	16	0.83 MHz	0.79 MHz	Out of spec	Out of spec
1	0	1	1	0	0	14	16	0.97 MHz	0.92 MHz	Out of spec	Out of spec
0	0	0	0	1	0	4	4	1.11 MHz	1.05 MHz	2.00 MHz	4.00 MHz
0	1	0	0	1	1	8	8	1.11 MHz	1.05 MHz	2.00 MHz	Out of spec
1	1	0	1	0	0	16	16	1.11 MHz	1.05 MHz	Out of spec	Out of spec
1	1	1	1	0	0	18	16	1.25 MHz	1.18 MHz	Out of spec	Out of spec
0	1	1	0	1	1	10	8	1.39 MHz	1.31 MHz	2.50 MHz	Out of spec
0	0	1	0	1	0	6	4	1.67 MHz	1.57 MHz	3.00 MHz	Out of spec
1	0	0	0	1	1	12	8	1.67 MHz	1.57 MHz	Out of spec	Out of spec
1	0	1	0	1	1	14	8	1.94 MHz	1.84 MHz	Out of spec	Out of spec
0	0	0	0	0	1	4	2	2.22 MHz	2.10 MHz	4.00 MHz	8.00 MHz
0	1	0	0	1	0	8	4	2.22 MHz	2.10 MHz	4.00 MHz	Out of spec
1	1	0	0	1	1	16	8	2.22 MHz	2.10 MHz	Out of spec	Out of spec
1	1	1	0	1	1	18	8	2.50 MHz	2.36 MHz	Out of spec	Out of spec
0	1	1	0	1	0	10	4	2.78 MHz	2.62 MHz	5.00 MHz	Out of spec
0	0	1	0	0	1	6	2	3.33 MHz	3.15 MHz	6.00 MHz	Out of spec
1	0	0	0	1	0	12	4	3.33 MHz	3.15 MHz	Out of spec	Out of spec
1	0	1	0	1	0	14	4	3.89 MHz	3.67 MHz	Out of spec	Out of spec

Table 1. Bus Frequency Examples (Sheet 3 of 3)

								FEI	FEE		
								CLKS1 = 0	= 1	= 1	= 1
								CLKS0 = 1	= 1	= 1	= 1
MFD			RFD			MFD	RFD	Range = X	= 0	= 1	= 1
2	1	0	2	1	0	Multiplier (N)	Divisor (R)	243 kHz	32.768 kHz	4.00 MHz	8.00 MHz
0	0	0	0	0	0	4	1	4.44 MHz	4.19 MHz	8.00 MHz	16.00 MHz
0	1	0	0	0	1	8	2	4.44 MHz	4.19 MHz	8.00 MHz	Out of spec
1	1	0	0	1	0	16	4	4.44 MHz	4.19 MHz	Out of spec	Out of spec
1	1	1	0	1	0	18	4	5.00 MHz	4.72 MHz	Out of spec	Out of spec
0	1	1	0	0	1	10	2	5.55 MHz	5.24 MHz	10.00 MHz	Out of spec
0	0	1	0	0	0	6	1	6.67 MHz	6.29 MHz	12.00 MHz	Out of spec
1	0	0	0	0	1	12	2	6.67 MHz	6.29 MHz	Out of spec	Out of spec
1	0	1	0	0	1	14	2	7.78 MHz	7.34 MHz	Out of spec	Out of spec
0	1	0	0	0	0	8	1	8.89 MHz	8.39 MHz	16.00 MHz	Out of spec
1	1	0	0	0	1	16	2	8.89 MHz	8.39 MHz	Out of spec	Out of spec
1	1	1	0	0	1	18	2	10.00 MHz	9.44 MHz	Out of spec	Out of spec
0	1	1	0	0	0	10	1	11.11 MHz	10.49 MHz	20.00 MHz	Out of spec
1	0	0	0	0	0	12	1	13.33 MHz	12.58 MHz	Out of spec	Out of spec
1	0	1	0	0	0	14	1	15.55 MHz	14.68 MHz	Out of spec	Out of spec
1	1	0	0	0	0	16	1	17.77 MHz	16.78 MHz	Out of spec	Out of spec
1	1	1	0	0	0	18	1	20.00 MHz	18.87 MHz	Out of spec	Out of spec

Software Configurations for Other Module Clocks

ATD Clock

The only clock source for the analog-to-digital (ATD) module is the bus clock. Depending on the power supply voltage applied to the analog-to-digital converter, the ATD clock should be in the range from 0.5 MHz to 2 MHz. The ATD control register's (ATDC) lower four bits, referred to as the prescaler rate select (PRS), determine the bus clock prescale factor for the ATD conversion clock. These sixteen prescale values can divide the bus clock in even integer values between 2 and 32. Based on the selected bus clock frequency and required system conversion times, the user must choose the prescale value to achieve the required ATD conversion rate — keeping in mind the minimum and maximum ATD clock range. The equation for determining the ATD clock frequency (f_{ATDCLK}) is:

$$f_{ATDCLK} = f_{Bus} \div\div [([PRS3:PRS0] +1) \times 2]$$

Therefore, the minimum bus frequency at which the ATD can be used is 1 MHz, in which case the ATD clock frequency would be:

$$f_{ATDCLK} = 1 \text{ MHz} \div\div [([\$0]+1) \times 2] = 500 \text{ kHz}$$

FLASH Clock

In order to perform FLASH program or erase operations, the internal FLASH clock must be configured to run between 150 kHz and 200 kHz. The bus clock is the reference clock source for the FLASH clock, and it is configured by two values in the FLASH clock divider register (FCDIV). The first value is PRDIV8, a 1-bit prescaler that either divides the bus clock by 8 or leaves it as is. The second is DIV5:DIV0, a 6-bit value that generates a divisor from 1 to 64 ([DIV5:DIV0]+1). The resulting equations for the FLASH clock frequency (f_{FCLK}) are:

$$\text{if PRDIV8 = 0, then } f_{FCLK} = f_{Bus} \div ([DIV5:DIV0] +1),$$

$$\text{else if PRDIV8 = 1, then } f_{FCLK} = f_{Bus} \div (8 \times\times [DIV5:DIV0] +1).$$

RTI Clock

The real-time interrupt function (RTI) has two clock sources to choose from, either the external reference clock (if available) or an internal, completely independent 1-kHz clock source, selectable by the RTICLKS bit in the system real-time interrupt status and control register (SRTISC). The internal clock reference in the ICG module cannot be used as a clock source for this module.

The RTI module has seven selectable prescaler values ranging from 256 to 32,768, selectable by the three bits, RTIS2:RTIS0 also in SRTISC. When these three bits are set to 0:0:0, the RTI function is disabled. When used with the

1-kHz reference, the timeout periods range from 8 ms to 1.024 s. The tolerance of the internal 1-kHz reference is approximately ±30%.

When the RTI is used to wake the MCU up from stop3 mode, both clock options are available. However, if the RTI is used to wake from stop2 mode, only the internal 1-kHz clock can be used as a reference because stop2 powers down the ICG module. If the RTI is used in run or wait modes, only the external clock option is available.

SPI Clock

The only clock source for the SPI module is the bus clock. The SPI has a 3-bit prescaler value that divides the bus by a value between 1 and 8, set by bits SPPR2:SPPR0 in the SPI baud rate register (SPIBR). In addition, another 3-bit value selects one of eight additional divide factors between 2 and 256, set by bits SPR2:SPR0 also in SPIBR. Therefore, the SPI baud rate is computed by the following equation:

$$\text{SPI baud rate} = f_{Bus} \div [(\text{SPPR}+1) \times 2^{(\text{SPR}+1)}]$$

The potential baud rates range from (bus clock ÷ 2) to [bus clock ÷ (8 × 256)].

SCI Clock

The only clock source for the SCI modules is the bus clock. The SCI has a 13-bit prescaler value that can be set in the SCI baud rate registers (SCIxBDH and SCIxBDL). The prescaler factor is simply the value of this 13-bit number and is referred to collectively as BR. BR can be set to any value from 0 to 8191. When BR = 0, the SCI baud rate generator is disabled to reduce system current consumption. For all other values,

$$\text{SCI baud rate} = f_{Bus} \div (16 \times \text{BR})$$

IIC Clock

The only clock source for the IIC module is the bus clock. The IIC baud rate is a function of the bus clock divided by the product of a multiplier and SCL divider. The IIC frequency divider register (IICF) is partitioned into two sections. The MULT portion provides for a multiplication factor (mul) of 1, 2, or 4. The remainder of the IICF register contains the ICR bits and provides for 64 SCL divider values ranging from 20 to 3840. The IIC baud rate is computed by the following formula:

$$\text{IIC baud rate} = f_{Bus} \div (\text{mul} \times \text{SCL divider})$$

TPM clock

The clock source for each of the two TPMs can be independently selected to be the bus clock, the fixed system clock (XCLK), or an external input fed into the TPMxCH0 pin. The maximum frequency allowed for the external clock fed into the TPMxCH0 pin option is one-fourth the bus rate.

The XCLK frequency is normally equal to the ICG's reference clock (ICGRCLK) divided by 2. Therefore, the XCLK frequency is dependent on the configuration of the ICG:

- In SCM and FEI modes, XCLK is the internal reference clock (ICGIRCLK) divided by 2, or 121.5 kHz when ICGIRCLK is trimmed.
- In FBE mode, XCLK is always equal to the bus clock.
- In FEE, XCLK is the external reference source (ICGERCLK) (e.g., the crystal oscillator) divided by 2.

In all cases, if the bus clock frequency is not at least four times the XCLK frequency, then XCLK is set equal to the bus clock.

Once the clock source has been selected, the TPM counter frequency can be divided by a prescaler determined by the 3-bit value PS2:PS0 in the timer x status and control register (TPMxSC). The prescaler is equal to 2^{PS}. Therefore, the equation for the frequency of the TPM counter is:

$$f_{TPM\ counter} = f_{clock\ source} \div\div 2^{PS}$$

MC9S08GB60 Clock Setup Helper

In conjunction with this application note, a Microsoft Excel workbook containing worksheets used to help configure the ICG, IIC, TPM, SCI, SPI, RTI, ATD, FLASH, and BDM can be downloaded. This resource, *MC9S08GB60 Clock Usage Worksheet* (contained in AN2494SW.zip), also contains a summary sheet that collects all the resulting frequencies, baud rates, timeouts, etc., on one page with the register settings to achieve these values. An instruction page is also provided for detailed instructions on how to use the workbook.

Conclusion

The internal clock generator is a new, highly flexible, module on the HCS08 Family of microcontrollers. It provides multiple options for MCU clock sources. These choices offer users flexibility when making system trade-offs among cost, precision, and performance.

The ICG has the advantage of requiring no external components or using valuable pins on the device when the internal reference generator is used. The characteristics of this oscillator make it accurate over temperature and voltage variations once it has been trimmed. The IRG is an ideal clock source for low-cost systems.

Because of the FLL, designers have great flexibility when choosing crystals and resonators for their system. Inexpensive crystals and resonators can be used and yet a very wide variety of system frequencies can still be obtained.

The flexibility of the ICG also makes setting up the MCU's peripherals much simpler. Bus frequencies can more easily be tailored for optimum performance of a specific module and can even be modified when a particular module is not in use.

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