# AN1997

FM/IF systems for SMSK/GFSK receivers Rev. 2 — 13 August 2014

**Application note** 

#### **Document information**

Info	Content		
Keywords	GMSK/GFSK modulation, BER, Gaussian LPF		
Abstract	To assist NXP Semiconductors customers in digital cellular and wireless/PCS system design, an NXP FM/IF system-based GMSK/GFSK demoboard has been developed based on CT-2 specifications. This application note presents a detailed description of this board including circuits, design information, and measured BER performance. The circuit diagram, component list, and board layout are also included.		



### **Revision history**

Rev	Date	Description		
2.0	20140813	Application note; second release.		
Modifications:		<ul> <li>The format of this application note has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> </ul>		
		<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Updated Figure 10.</li> </ul>		
1.0	19970820	Application note; initial release.		

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## 1. Introduction

In order to meet the rapidly increasing demand for mobile radio and wireless/PCS services, digital cellular and digital wireless systems have become the new generation of mobile communications for higher capacity. It is a new challenge for engineers to find IC solutions for these digital wireless applications.

In worldwide digital cellular, wireless/PCS standards, GMSK/GFSK modulation techniques have been widely employed as illustrated in <u>Table 1</u>. In order to assist the applications of NXP ICs in these digital systems, an NXP FM/IF system-based GMSK/GFSK demoboard has been developed. This application note provides a detailed description of this board to help customers achieve the best performance using the SA636, and also to provide suggestions for the applications of other NXP FM/IF systems.

Standard	Access	Modulation	Bit rate	Channel spacing
IS-54	TDMA	π/4-DQPSK	48 kbit/s	30 kHz
GSM	TDMA	GMSK	270 kbit/s	200 kHz
CT-2	TDMA	GFSK	72 kbit/s	100 kHz
DECT	TDMA	GFSK	1.152 Mbit/s	1.728 MHz

#### Table 1. Summary of digital cellular and cordless standards

The application note is organized as follows:

- Introduction.
- Review of GMSK/GFSK modulation: advantages of GMSK/GFSK modulation techniques and implementation methods.
- Overview of the demoboard: general block diagram and detailed description of each part of the board.
- BER measurements: measurement set-up, procedures, and measured results.
- Questions and Answers.

# 2. Review of GMSK/GFSK modulation

GMSK (Gaussian Minimum Shift Keying) is a premodulation Gaussian filtered binary digital frequency modulation scheme with modulation index of 0.5. The following features make GMSK very suitable for digital cellular and wireless applications.

- Constant envelope: this allows the operation of Class-C RF power amplifiers to achieve higher system power efficiency.
- Narrow power spectrum: narrow main lobe and low spectral tails keep the adjacent channel interference to low levels and achieve higher spectral efficiency.
- Coherent/non-coherent detection capabilities.
- Good BER performance.

GMSK modulation can be implemented in two ways. The most straightforward way is to transmit the data stream through a Gaussian low-pass filter and apply the resultant wave form to a voltage controlled oscillator (VCO) as shown in <u>Figure 1</u>. The output of the VCO is then a frequency modulated signal with a Gaussian response. The advantage of this

scheme is the simplicity, but it is difficult to keep an exact modulation index of 0.5 with this scheme. Therefore, VCO implemented GMSK is usually used in non-coherent detection systems such as DECT and CT-2.



GMSK signals can also be generated using a quadrature modulation structure. Consider the phase modulated signal given by:

$$s(t) = \cos[\omega_c t + \phi(t)] \tag{1}$$

This can be expanded into its in-phase and quadrature components,

$$s(t) = \cos[\phi(t)] \cos(\omega_c t) - \sin[\phi(t)] \sin(\omega_c t)$$
(2)

The quadrature modulator is based on Equation 2. The implementation of such a GMSK modulator is shown in Figure 2. The incoming data is used to address two separate ROMs which contain the sampled versions of all possible phase trajectories within a given interval. After D/A conversion, the output of each ROM is applied to the I/Q modulator. The output is the GMSK modulated signal. This implementation scheme provides an exact modulation index of 0.5, which allows coherent detection.

GFSK (Gaussian Frequency Shift Keying) is also a premodulation Gaussian filtered digital FM scheme, but without the restriction of modulation index to be 0.5. The block diagram of GFSK modulator is the same as shown in <u>Figure 1</u>, but the modulation index can be specified according to the applications.



GMSK signals can be demodulated in three ways: FM discriminator detection, differential detection, and coherent detection. The coherent detection scheme has the best BER performance, but is only suitable for I/Q structure based GMSK systems (Ref. 6). The differential detection method has BER degradation even with complex implementation (Ref. 7). The limit/frequency discriminator structure is the simplest scheme suitable for both GMSK and GFSK applications. Therefore, the FM discriminator technique is widely used for GMSK/GFSK demodulation in digital cellular/PCS applications. Figure 3 presents the block diagram of an FM discriminator GMSK/GFSK demodulator.



# 3. Overview of the GMSK/GFSK demoboard

Figure 4 is the block diagram of a VCO/FM discriminator based GMSK/GFSK modem (modulator/demodulator), which also illustrates the structure of the NXP GMSK/GFSK demoboard. The demoboard contains the entire demodulator as well as the Gaussian low-pass filter (LPF) for the modulator. The input data stream is first premodulation filtered by the Gaussian LPF, then the filtered baseband waveform is applied to an FM signal generator with specific modulation index. The output is then the GMSK/GFSK modulated signal. After the limit/frequency discriminator detection, a Gaussian LPF is employed to eliminate noise. The output of the threshold detector is the regenerated binary data, which can be sent to a data error analyzer to evaluate the BER performance.



### 3.1 Gaussian LPF

On the demoboard, a fourth-order Gaussian LPF is implemented for both pre-modulation filtering and post-demodulation filtering. The response function of this fourth-order filter can be expressed as (Ref. 4):

$$H(s) = \frac{\omega_1^2}{S^2 + 2\zeta_1 \omega_1 S + \omega_1^2} \cdot \frac{\omega_2^2}{S^2 + 2\zeta_2 \omega_2 S + \omega_2^2}$$
(3)

By looking up the Gaussian LPF poles table[4], with 3 dB bandwidth normalized to unity, we have:

$$\omega_1 = 1.9086$$
  
 $\zeta_1 = 0.7441$   
 $\omega_2 = 1.6768$   
 $\zeta_2 = 0.9720$ 

This fourth-order Gaussian LPF is implemented with switched capacitor filters. The reason for using this scheme is that the LPF 3 dB bandwidth can be controlled by an external clock which allows generating GMSK signals with different  $BT_b$ . To realize a fourth-order LPF, two stages of LMF100 are cascaded and operated at Mode-3[5]. Figure 5 shows the circuit diagram for this mode.



For Mode-3 LPF applications, the following formulas can be used to calculate the resistor values [5]:

$$H_{LP}(s) = \frac{H_{OLP}\omega_0}{S^2 + (S\omega_0/Q) + \omega_0}$$
(4)

where:

$$H_{OLP} = -\frac{R_4}{R_1}$$
$$\omega_0 = \left(\frac{f_{clk}}{100}\right) \cdot \sqrt{\frac{R_2}{R_4}}$$
$$Q = \left(\frac{R_3}{R_2}\right) \cdot \frac{\sqrt{R_2}}{R_4}$$

### 3.1.1 Example

- Step 1Decide the gain and choose R value:<br/>For unity gain, we have  $H_{OLP} = -R_4/R_1 = -1$ , that is,  $R_4 = R_1$ .<br/>For the first stage, we choose a convenient value for input resistance:<br/> $R_{14} = R_{11} = 22 \ k\Omega$
- Step 2 Calculate R<sub>12</sub>: Compare <u>Equation 3</u> with <u>Equation 4</u>, we have:

$$\omega_1 = \left(\frac{f_{clk}}{100}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}}$$

By choosing  $f_{clk}$  = 100 times the 3 dB bandwidth, we have:

$$\omega_1 = \sqrt{\frac{R_{12}}{R_{14}}} \rightarrow R_{12} = 80.14 \ k\Omega$$

Step 3 Calculate R<sub>13</sub>: From the comparison of <u>Equation 3</u> and <u>Equation 4</u>, we also have:

$$Q_1 = \frac{1}{(2\zeta_1)} = \left(\frac{R_{13}}{R_{14}}\right) \cdot \sqrt{\frac{R_{12}}{R_{14}}} = \frac{1}{(2 \cdot 0.7441)}$$

For the second stage, the resistor values can be calculated by the same procedures. For this example, they are:

$$R_{24} = R_{21} = 22 \text{ k}\Omega$$
  
 $R_{22} = 61.86 \text{ k}\Omega$   
 $R_{23} = 18.98 \text{ k}\Omega$ 

To obtain a good Gaussian LPF, the resistor values have to be adjusted with all input/output circuits connected. Baseband eye-diagrams and modulated power spectrum could be the references for the adjustment.

### 3.2 FM/IF system

The NXP low-voltage high-performance monolithic FM/IF system, SA636, is employed for demodulation on the GMSK/GFSK demoboard. SA636 was designed specially for wide bandwidth portable communications applications, incorporating with a mixer/oscillator, two limiting intermediate frequency amplifiers, quadrature detector, and audio and RSSI op amps. The RF section is similar to the famous SA605. The audio and RSSI outputs have amplifiers.

With Power-down mode, SA636 will function down to 2.7 V. Figure 6 is the block diagram of SA636. Detailed information can be found in the data sheet (Ref. 3) and associated application notes (Ref. 1, Ref. 2).



The GMSK/GFSK demoboard is designed for an RF frequency of 45 MHz, LO frequency of 55.7 MHz, and intermediate frequency of 10.7 MHz. For different RF frequency applications, the step-by-step matching circuits design procedure is presented in Ref. 1.

Although this demoboard is designed with SA636 based on CT-2 specifications, NXP also provides FM/IF solutions for many other GMSK/GFSK systems. SA636 is specially designed for wide bandwidth applications. For lower data rate applications such as CDPD (19.2 kbit/s), SA605 family is recommended. For DECT and other high data rate applications, SA636 and SA639 are the recommended solutions. Data (audio) output bandwidth is the main limiting factor for high data rate applications. <u>Table 2</u> presents a summary of the major characteristics of NXP FM/IF systems. The suggested maximum

data rate for each part is an approximation based on the baseband eye pattern. Higher data rate could be operated with some modifications or if more BER degradation is allowed.

Table 2. Major characteristics of the FM/IF systems

Characteristic/ feature	SA602A/SA604A	SA605	SA636	SA639
V <sub>CC</sub>	4.5 V to 8 V	4.5 V to 8 V	2.7 V to 5.5 V	2.7 V to 5.5 V
I <sub>CC</sub>	2.4/3.3 mA at 6 V	5.7 mA at 6 V	6.5 mA at 3 V	8.3 mA at 3 V
SINAD	–120 dBm/0.22 μV	–120 dBm/0.22 μV	–111 dBm/0.54 μV	–111 dBm/0.54 μV
	RF: 45 MHz	RF: 45 MHz	RF: 240 MHz	RF: 240 MHz
	IF: 455 kHz, 1 kHz tone, 8 kHz deviation	IF: 455 kHz, 1 kHz tone, 8 kHz deviation	IF: 10.7 MHz, 1 kHz tone, 125 kHz deviation	IF: 10.7 MHz, 576 kHz tone, 288 kHz deviation
Features	Audio and data pins	Audio and data pins	Power-down mode	Power-down mode
	IF bandwidth of 25 MHz	IF bandwidth of 25 MHz	Low-voltage	Low-voltage
	Matching for standard	Matching for 455 kHz IF filters	Fast RSSI	Fast RSSI
	455 kHz IF filters		IF bandwidth of 25 MHz	IF bandwidth of 25 MHz
			Internal RSSI op amp	Internal RSSI op amp
			Wideband data out	Wideband data out
			Matching for 10.7 MHz	Post detection amp
			IF filters	Matching for 10.7 MHz IF filters
Data rate <sup>[1]</sup>	100 kbit/s	100 kbit/s	1.5 Mbit/s	2 Mbit/s

[1] Approximated maximum data rate. With some modifications, higher data rate might be operated.

### 3.3 Threshold detector and data regeneration

A 2-level threshold detector with sampling time adjustment circuits is implemented for data regeneration as shown in the circuit diagram. The output base band signal (eye-diagrams) from SA636 is first fed into a comparator (LM311) to generate a TTL logic signal which is then sampled with the data clock at the transmitting bit rate. The phase of the data clock can be adjusted manually through a monostable multivibrator (74HC123) to achieve the optimal sampling time. The demoboard is initially adjusted for a bit rate of 72 kbit/s. If a different data rate is used, the sampling time has to be re-adjusted.

The Symbol Timing Recovery (STR) circuit is not implemented on this demoboard. The transmitting data clock should be either hardwire connected from the transmitter, or obtained from a separate STR circuit for operation. The measured performance presented in this paper is conducted with hard-wire connected data clock. However, BER degradation caused by STR should be no more than 1 dB (<u>Ref. 8</u>).

## 4. Performance measurements

The performance of this GMSK/GFSK demoboard including receiver sensitivity and BER is experimentally evaluated. BER performance is evaluated based on CT-2 specifications. Measurement procedures and the measured results are presented in this section.

### 4.1 Measurement setup

<u>Figure 7</u> illustrates the measurement setup with the GMSK/GFSK demoboard. A data error analyzer is employed to generate a Pseudo Random Binary Sequence (PRBS) with length of  $10^9 - 1$  at a data rate of 72 kbit/s. This data sequence is sent to the Gaussian LPF on the board for premodulation filtering. The output Gaussian filtered baseband signal is then applied to an FM signal generator as the modulating signal. To generate a GMSK modulated signal (modulation index = 0.5) at a bit rate of 72 kbit/s, frequency deviation of the FM signal generator needs to be set at 18 kHz. The output from the generator is then a GMSK modulated signal (at 45 MHz). Another signal generator is employed to provide an LO signal at 55.7 MHz for the FM/IF system detection.



After FM discriminator detection, the output base band signal is fed into another Gaussian LPF on the board to eliminate noise. The 3 dB bandwidth of both Gaussian LPFs is controlled by an external clock. This clock should be a square-wave signal with TTL level. By controlling the frequency of this clock, different BT<sub>b</sub> can be achieved for certain bit rate. To have BT<sub>b</sub> equal 0.5 with bit rate of 72 kbit/s, the clock signal is set at 3.6 MHz (100 times the required 3 dB bandwidth). The output from the LPF is then sent to the threshold detector for data regeneration. The data clock signal is taken directly from the data error analyzer. The sampling time can be controlled by adjusting VR2 in the circuit diagram. The recovered data sequence is fed back to the Data Error Analyzer for BER measurement.

### 4.2 Measurement procedure and results

- Measure SINAD at the audio output of SA636: use the same setup as described above, but set RF = 45 MHz, fm = 1 kHz, Df = 8 kHz; LO = 55.7 MHz, -10 dBm; the measured typical sensitivity for 12 dB SINAD should be about -110 dBm. (See <u>Ref. 1</u> for detailed SINAD measurement.)
- 2. Check 'LPF clock input': this clock should be a TTL level signal with the frequency of 100 times the desired 3 dB bandwidth of the LPF. For the data rate of 72 kbit/s and  $BT_b = 0.5$  LPF, the clock frequency is 3.6 MHz (100 × 36 kHz).
- 3. Check 'Tx data input': 72 kbit/s baseband NRZ signal.
- Measure 'Tx data output': Gaussian low-pass filtered baseband eye-diagram as shown in <u>Figure 8</u>.
- 5. Check 'data clock input': 72 kHz clock signal.
- Adjust sampling position: by adjusting VR2, set the rising edge of the clock at Pin 11 of Unit 4 (74HC74) to be at the center of the eye-diagram at Pin 2 of Unit 6 (LM311) in the circuit diagram.
- 7. **Measure BER with high RF level:** set RF input signal level at -80 dBm and -90 dBm, LO signal level at -10 dBm: error free.
- Measure BER versus RF input level curve: RF level: -94 dBm ~ -104 dBm, LO level: -10 dBm, at each point, at least 100 errors have to be measured. Figure 9 presents the measured BER as a reference.





# 5. Questions and answers

Question	For the SINAD measurement, is it necessary to connect the whole system?
Answer	Even though only part of the system is used to measure SINAD, it is recommended to connect the whole system because the RF part should be tested under the operating conditions.
Question	Why is the DC current ( $I_{CC}$ ) very large when I measure the SINAD on SA636?
Answer	Check the power supplies. Make sure both +5 V and $-5$ V are connected all the time, even though only +5 V is needed for SA636.
Question	Is it possible that SINAD is good, but BER is not good?
Answer	Yes, because there are other factors affecting BER.
Question	What are the main factors affecting BER?
Answer • • •	They are: Tx LPF FM deviation and RF signal level RF part sensitivity Rx LPF Threshold detector Sampling time
Question	There are two 'Rx Data Output' ports. Which one should be used?
Answer	Two 'Rx Data Output' ports are designed to provide convenience for different measurement conditions. Either one can be used if the BER analyzer has the $Q/\overline{Q}$ detection capability.
Question	What needs to be done for higher RF frequency applications?
Answer	First, RF and LO input matching circuits have to be redesigned at the desired frequency. Second, the layout of RF and LO input circuits might also need to be re-designed. The inputs should be further away from each other and in different directions (not in parallel with each other) to provide better isolation.



Application note

Rev. 2 — 13 August 2014

**NXP Semiconductors** 

FM/IF systems for SMSK/GFSK receivers



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Qty.	Value	Voltage	Component reference	Part description	Vendor	Mfg.	Part number
Surfac	Surface mount capacitors						
1	4.7 pF	50 V	C8	Cap. cer. 1206 NPO ±0.25 pF	Garrett	Rohm	MCH315A4R7CK
1	39 pF	50 V	C7	Cap. cer. 1206 NPO ±5 %	Garrett	Rohm	MCH315A390JK
1	47 pF	50 V	C25	Cap. cer. 1206 NPO ±5 %	Garrett	Rohm	MCH315A470JK
1	100 pF	50 V	C23	Cer. chip cap. 1206 NPO $\pm 5$ %	Garrett	Philips	1206CG101J9BB0
1	120 pF	50 V	C10	Cer. chip cap. 1206 NPO $\pm$ 5 %	Garrett	Philips	1206CG121J9BB0
1	150 pF	50 V	C14	Cer. chip cap. 1206 NPO $\pm$ 5 %	Garrett	Philips	1206CG151J9BB0
2	330 pF	50 V	C11, C15	Cer. chip cap. 1206 NPO $\pm$ 5 %	Garrett	Philips	1206CG331J9BB0
8	0.1 μF	50 V	C4, C5, C6, C9, C12, C13, C18, C20	Cer. chip cap. 1206 X7R ±10 %	Garrett	Philips	1206R104K9BB0
1	0.47 μF	35 V	C22	Tant. chip cap B 3528 $\pm 10$ %	Garrett	Philips	49MC474B035KOAS
3	4.7 μF	10 V	C16, C21, C24	Tant. chip cap B 3528 $\pm$ 10 %	Garrett	Philips	49MC475B010KOAS
3	10 μF	10 V	C3, C17, C19	Tant. chip cap B 3528 $\pm$ 10 %	Jaco	AVX	TAJB106K016R
	option		C26, C27, C28, C29				
Surfac	ce mount v	ariable ca	pacitors				
2	5 pF to 30 pF		C1, C2	Trimmer capacitor	Kent Elect.	Kyocera	CTZ3S-30C-W1
Surfac	ce mount r	esistors					
1	0 Ω		R2	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW000E
1	82 Ω		R21	Res. chip 1206 1/8 W $\pm$ 5 %	Garrett	Rohm	MCR18JW820E
3	180 Ω		R17, R26, R30	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW181E
1	330 Ω		R18	Res. chip 1206 1/8 W $\pm$ 5 %	Garrett	Rohm	MCR18JW331E
2	560 Ω		R7, R16	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW561E
2	620 Ω		R24, R28	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW621E
2	1.3 kΩ		R12, R22	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW132E
1	1.5 kΩ		R19	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW152E
3	15 kΩ		R5, R14, R20	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW153E
2	18 kΩ		R27, R31	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW183E
1	20 kΩ		R1	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW203E
7	22 kΩ		R3, R4, R6, R8, R10, R13, R15	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW223E
2	33 kΩ		R23, R29	Res. chip 1206 1/8 W $\pm$ 5 %	Garrett	Rohm	MCR18JW333E
1	56 kΩ		R9	Res. chip 1206 1/8 W $\pm$ 5 %	Garrett	Rohm	MCR18JW563E
1	68 kΩ		R11, 25	Res. chip 1206 1/8 W $\pm 5$ %	Garrett	Rohm	MCR18JW683E
Surfac	ce mount v	ariable re	sistors				
1	5 kΩ		VR1	SM Res. Trim, 1 TRN ±20 <sup>°</sup> % J-H	Garrett	Philips	ST-4TA502
1	500 kΩ		VR2	SM Res. Trim, 1 TRN ±20 % J-H	Garrett	Philips	ST-4TA504

### Table 3. Customer application component list for GMSK/GFSK demoboard

Qty.	Value	Voltage	Component reference	Part description	Vendor	Mfg.	Part number
Surfa	ce mount i	nductors					
2	0.39 μH		L2, L3	Chip inductors - 1800CS series	Coilcraft	Coilcraft	1800CS-391
Surfa	ce mount v	variable in	ductors				
1	5.6 μΗ		L1	Adjustable SM inductor 5CCD type	Digikey	ТОКО	TKS2251
Filters	S						
2	10.7 MHz		FLT1, FLT2	10.7 MHz IF filter, 110 kHz ± 30 kHz	Murata	Murata	SFE10.7MHY-A
Surfa	ce mount i	ntegrated	circuits		1		
2			U1, U3	Switched capacitor filter	Hamilton	National	LMF100CIWM
1			U2	Low voltage high performance mixer FM IF system with high-speed RSSI	NXP	NXP	SA636DK/01
1			U4	Dual D-type flip-flop with set and reset; positive edge-trigger	NXP	NXP	74HC74
1			U5	Dual re-triggerable monostable multivibrator with reset	NXP	NXP	74HC123
1			U6	Voltage comparator	Philips	Philips	LM311
Misce	llaneous					÷	
8			J1, J2, J3, J4, J5, J6, J7, J8	SMA gold connector	Newark	EF Johnson	142-0701-801
1			JP1	6-pin header, straight	Mouser	Molex- Waldem	558-22-05-2061
1				Printed circuit board	Philips	Philips	GMSK/DC#10626

### Table 3. Customer application component list for GMSK/GFSK demoboard ...continued

# 7. Abbreviations

Table 4. Abbre	eviations
Acronym	Description
BER	Bit Error Rate
CT-2	Cordless Telephone 2
D/A	Digital-to-Analog
DECT	Digital European Cordless Telephone
DQPSK	Differential Quadrature Phase Shift Keying
FM	Frequency Modulation
GFSK	Gaussian Frequency Shift Keying
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile
IC	Integrated Circuit
IF	Intermediate Frequency
LPF	Low-Pass Filter
NRZ	Non-Return-to-Zero
PCS	Personal Communications Service
	Physical Coding Sublayer
ROM	Read-Only Memory
STR	Symbol Timing Recovery
TDMA	Time Division Multiple Access
TTL	Transistor-Transistor Logic
VCO	Voltage Controlled Oscillator

## 8. References

- [1] AN1994, "Reviewing key areas when designing with the SA605" application note; NXP Semiconductors; www.nxp.com/documents/application\_note/AN1994.pdf
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