AN14520

General MCU PWM DAC Application

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Document information

Information	Content
Keywords	AN14520, PWM DAC
Abstract	This application note introduces how to set low-cost DAC using the PWM output.

1 Introduction

This application note introduces how to set the low-cost Digital-to-Analog Converter (DAC) using the PWM output. The main application is household electrical and industry appliances, which need a low cost and accurate DAC without a high-bandwidth requirement. This application note includes two main parts:

- The principle of PWM DAC
- The features and using FTM from Kinetis E Series MCU and CTimer from MCX Series MCU to implement the DAC function

2 Implementation principle of PWMDAC

This article uses frequency domain analysis to perform Fourier transform on periodic rectangular pulse signals (as shown in Figure 1):

$$f(t) = \frac{A\tau}{T}\sum_{-\infty}^{\infty}\frac{\sin(n\omega\tau/2)}{n\omega\tau/2}\cos(n\omega t) \quad (1)$$

Among them, ω is the fundamental frequency. The amplitude of the n^{th} harmonic of the signal is:

$$A_n = \frac{2A\tau}{T}\left|\frac{\sin(n\pi\tau/2)}{n\pi\tau/2}\right| \quad (2)$$

From this equation, the DC component of its voltage is obtained $\frac{A\tau}{T}$, where A is the amplitude of the original rectangular pulse (as shown in Figure 1) $\frac{\tau}{T}$. Therefore, the DC component of the voltage is only related to the duty cycle. If using a filter to filter out harmonic components, we can obtain a DC output voltage that is linearly related to the duty cycle. The goal of changing the output voltage by changing the duty cycle is achieved.

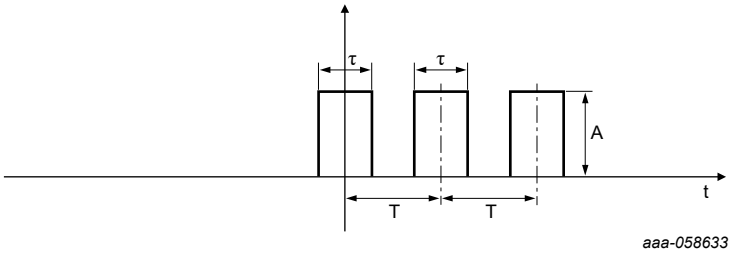

Figure 1. Time domain waveform of PWM wave

2.1 Influence and selection of various parameters in RC low-pass filter in the design of PWMDAC

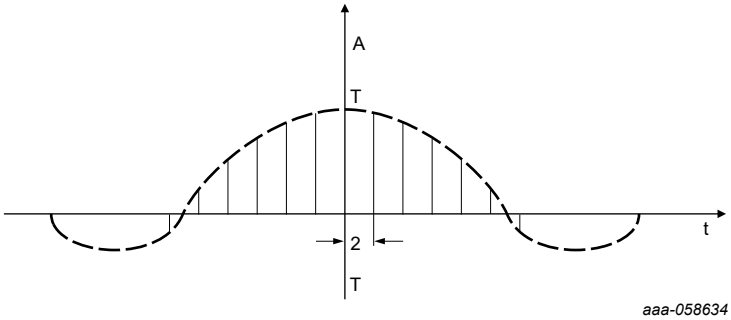

Figure 2. Frequency domain waveform of PWM wave

As the PWM wave is a periodic signal, its frequency spectrum is discrete (as shown in Figure 2). The frequency domain interval between the DC component and the first harmonic is $\frac{2\pi}{T}$ and the cut-off frequency of the RC filter is $\omega = \frac{1}{RC}$.

To ensure the complete filtering of the first harmonic, the *f* frequency of the PWM wave is taken $\omega \leq \frac{1}{10} \cdot \frac{2\pi}{T}$ as in engineering.

Because the transfer function of the RC filter is $\alpha = \frac{1}{RC}$ $|H(jw)| = \frac{\alpha}{jw+\alpha}$, its frequency domain amplitude characteristic is monotonically decreasing. It can be observed that the faster the amplitude decreases when *RC* is larger, the lower the cutoff frequency, and the better harmonic filtering. However, the response speed of the system to reach stability slows down, and the output lag increases. So, it's not the *RC* bigger the better. If the design requires a delay of milliseconds, the subsequent amplification circuit must choose devices with good switching characteristics to reduce the distortion of the PWM output waveform. Assuming that the frequency of the PWM wave is 40 kHz, R = 4.7 K, and C = 100 nF, the output of simulation result for the PWM DAC is as shown in Figure 3, and the time for the output voltage to rise and stabilize is about 2.86 ms,

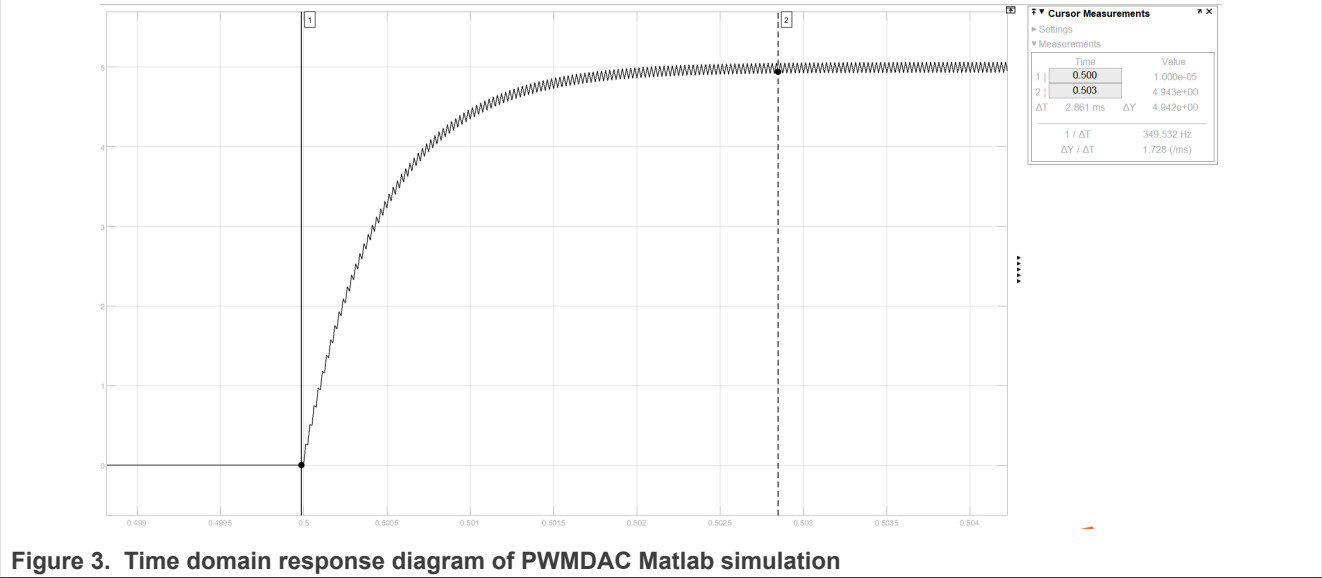

Figure 3. Time domain response diagram of PWMDAC Matlab simulation

Let's take care of the τ influence of PWM wave pulse width again. Assuming that the frequency of the PWM wave remains constant, the frequency domain interval between the first harmonic and the DC component is still $\frac{2\pi}{T}$, and the spectral envelope is horizontally stretched or compressed with the change of pulse width, the frequency domain interval between each harmonic remains unchanged. So, *RC* does not affect the selection of filter parameters.

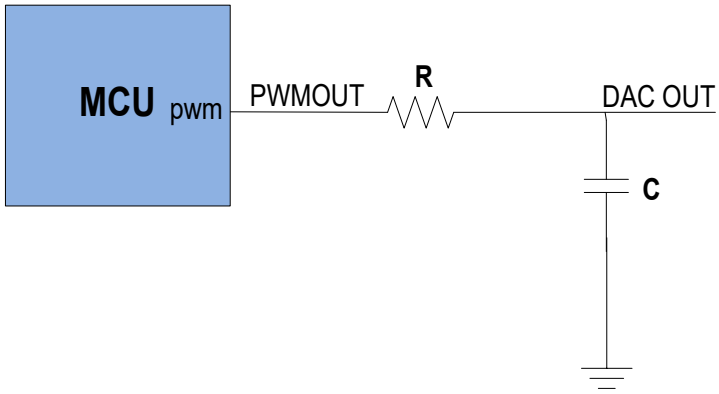

Figure 4. RC filtering circuit

According to the DC component of Equation 1, the DAC voltage output can only vary between 0 V and 3.3 V, and the accuracy is difficult to guarantee as the load current and ambient temperature change. Due to the low precision of the changing parts of the circuit, there is no need to use high-resolution PWM output. In addition, the load capacity of the DAC output in Figure 4 is relatively poor and is only suitable for connecting with subsequent circuits with high input impedance. Therefore, in situations where high precision and load capacity are required, it is necessary to add a conditioning amplifier circuit to the circuit in Figure 4.

2.2 Parameters design

To replace the original DAC chip, the DAC parameters of the original DAC chip were consulted and a 10-bit DAC chip with a resolution of 1/1024 is found. Based on this result, a PWM wave period count value must be more than 1024 was selected, if the counter counting clock was predetermined to be 72 MHz (KE17z). Therefore, the carrier frequency of PWM is 40 kHz.

To achieve a good ripple suppression effect, according to the formula $\frac{1}{RC} \le \frac{1}{100} \cdot 2\pi f$, $f = 40\ KHz$:

$$RC \ge \frac{1}{8\pi} \times 10^{-2} \approx 4 \times 10^{-4}$$

According to the parameter selection method, the parameters for the RC filtering circuit are selected as R = 4.7 K and C = 0.1 µF:

$$RC = 4.7 \times 10^{-4} > 4 \times 10^{-4}$$

Figure 5 shows the recommended circuit for PWM DAC using CTimer. For Kinetis series MCU which has high driver pins, if using these pins, buffer gate chips may not be a must.

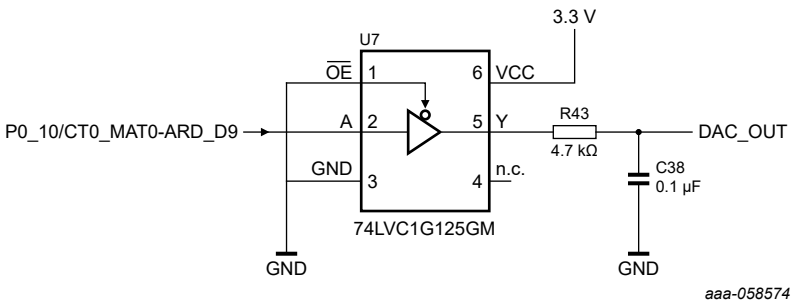

Figure 5. PWM DAC recommended circuit

2.3 PWM DAC using CTimer

Each CTimer has up to four capture and four match registers with corresponding inputs and outputs. Configure the CTimer to the PWM mode and use it as the PWM output. In this use case, four match registers can be used in this application. After configuring as PWM Mode, one channel is occupied to the server as the Period register. Each CTimer can generate three PWM outputs.

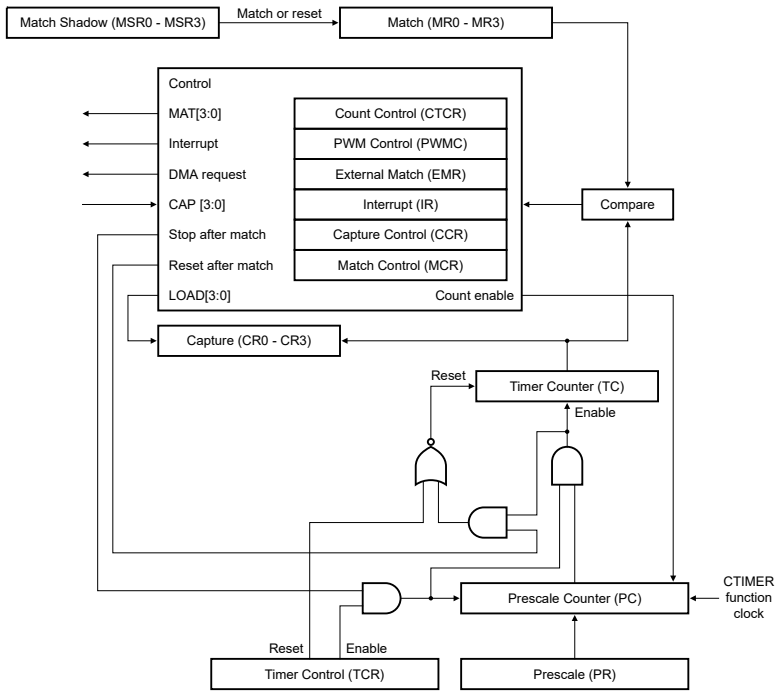

Figure 6. CTimer block diagram

For each timer, you can select a maximum of three single-edge controlled PWM outputs on the `MATn[2:0]` outputs. One additional match register (see **Match (MR0 - MR3)**) determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to **high**. The match register resets the timer that you can configure to set the PWM cycle length. When the timer is reset to zero, all currently high match outputs configured as PWM outputs are cleared.

For more details, see AN14520SW.

2.4 PWM DAC using FTM

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

The PWM synchronization provides an opportunity to update the MOD, HCR, CNTIN, CnV, OUTMASK, INVCTRL, and SWOCTRL registers with their buffered value and force the FTM counter to the CNTIN register value use the hardware trigger to synchronize. In this use case, we use a hardware trigger to synchronize CnV to modify the duty Cycle of PWM for reducing CPU over ahead. The external trigger is caused by the event which is generated when the FTM counter matches the CnV register. And the signal can be routed to any of the three hardware trigger inputs of FTM by TRGMUX module. Then, it controls the output voltage of PWM DAC.

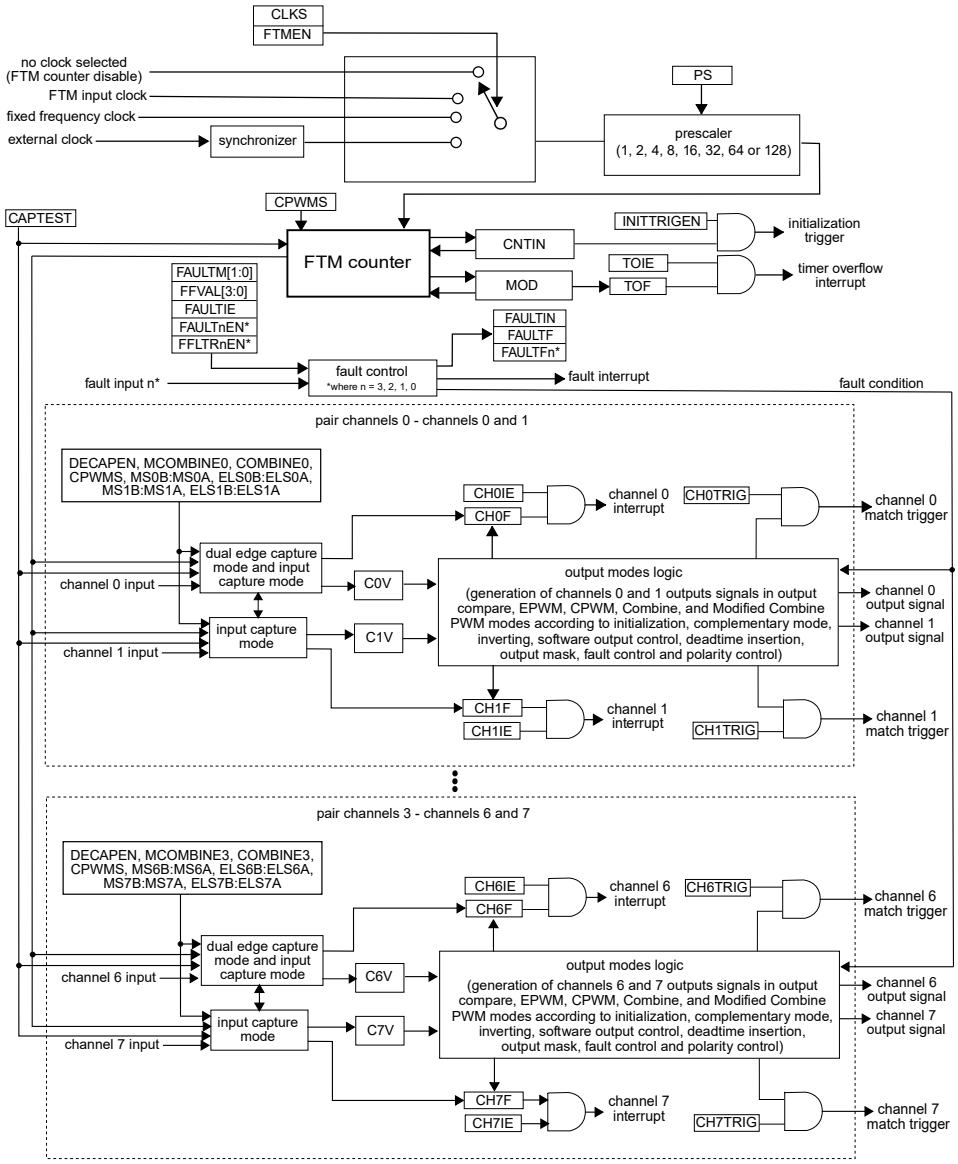

Figure 7. FTM block diagram

For more details, see AN14520SW.

3 Performance test

Now, we use the FRDM-KE17Z to test the performance of PWM DAC, using PTB12 to generate PWM waveform.

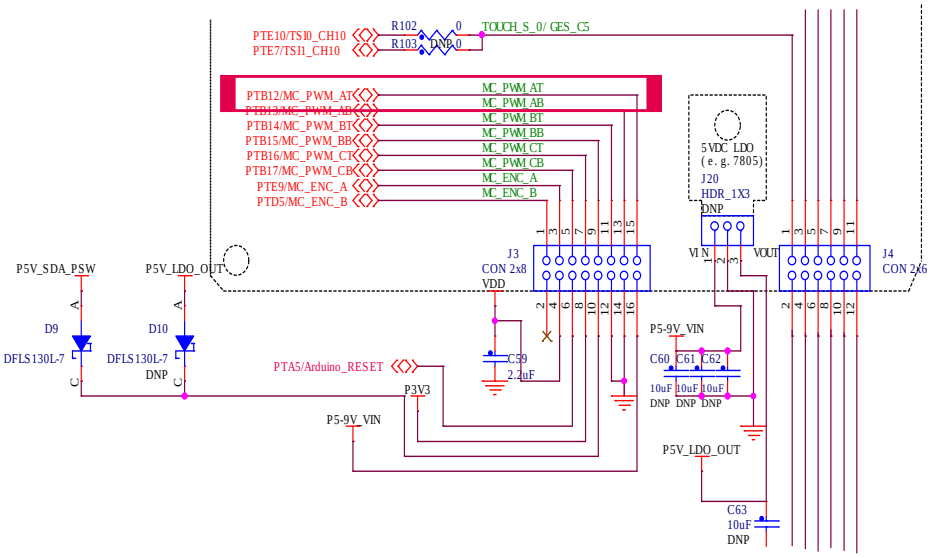

Figure 8. PWM PIN

Table 1. PWM waveform

Refer Voltage mV	Output Voltage mV	Error ΔU mV
0	0.9	0.9
2	2.7	0.7
5	4.5	-0.5
10	10.1	0.1
20	19.2	-0.8
50	50.4	0.4
100	99.9	-0.1
200	200.7	0.7
500	499.7	-0.3
1000	1000.3	0.3
1200	1200.2	0.2
1500	1498.8	-1.2
2000	1999.2	-0.8
2200	2198	-2
2500	2496	-4
3000	2996	-4
3200	3194	-6
3250	3244	-6
3290	3285	-5

Table 1. PWM waveform*...continued*

Refer Voltage mV	Output Voltage mV	Error ΔU mV
3295	3290	-5
3300	3298	-2

As shown in Table 1, we can see:

1. The linearity of the output voltage of the PWM DAC is good.
2. The resolution reaches 2 mV, which can meet the needs.
3. VDD is high-precision. In this test, the VDD is 3298 mV.

Note: *If the VDD is inaccuracy, we can sample the VDD voltage to compensate duty cycle of PWM output to achieve high-precision DAC or do Linear Calibration for output.*

3.1 Output waveforms and time response

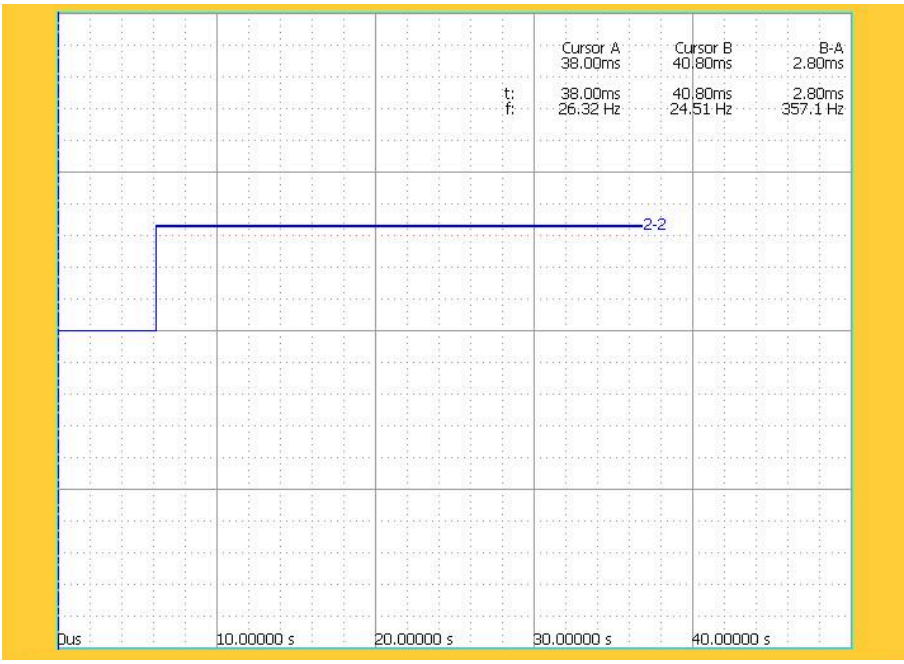

Figure 9. Output test results of PWMDAC

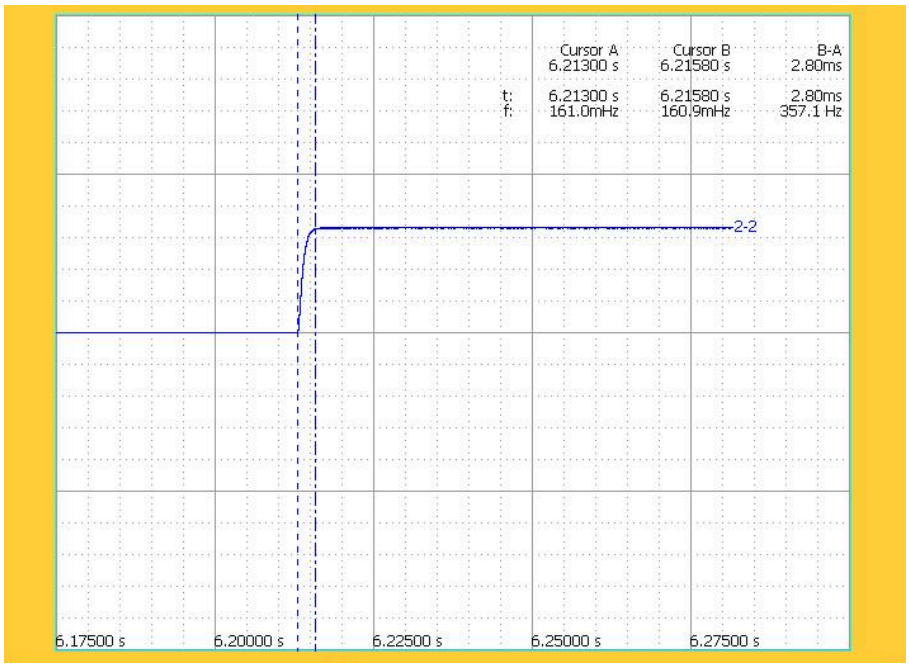

Figure 10. Time domain amplified test results of PWM DAC output

Figure 9 and Figure 10 show the same output waveform. Figure 10 shows the time-domain amplified output test results. As shown in Figure 10, the DAC output reaches stability in approximately 2.8 ms, which meets the performance requirements.

4 Conclusion

Based on the theoretical analysis of PWM waveform composition, this article proposes that to save cost, demodulate the DAC modulation signal in PWM through a low-pass filter to achieve DAC. This article analyzes the principle of PWM DAC and the selection of RC parameters. The test result is nearly the same with simulation. This circuit is highly suitable for the application.

5 Revision history

Table 2 summarizes the revisions to this document.

Table 2. Revision history

Document ID	Release date	Description
AN14520 v.1,0	16 December 2024	Initial public release

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