AN14518

Crystal Oscillator Design Guide

Rev. 1.0 — 29 November 2024 Application note

Document information

Information	Content
Keywords	Pierce oscillator, crystal oscillator, XTAL, negative resistance, loading capacitors, drive level, XTAL start-up
Abstract	This document covers the design process for the XTAL oscillator in NFC Reader circuits. In this context, design means the selection of the correct XTAL unit and its implementation into the customer design.

1 Introduction

This document explains what considerations need to be made when designing and tuning the **crystal oscillator** (referred to as "**XTAL**") for NFC Design. It also provides instructions on how to check all important parameters which may influence the XTAL start-up and stability. The document also includes a list of recommended XTALs for each NXP product.

Note that choosing the correct XTAL is only one part to be considered. For proper functionality, the PCB layout and other factors such as load capacitance and drive level also have to be considered.

Note: *In this document, the acronym **NFCC** (NFC Controller) is used to refer to an NFC Integrated Circuit (for example: PN7642).*

2 XTAL design - flowchart

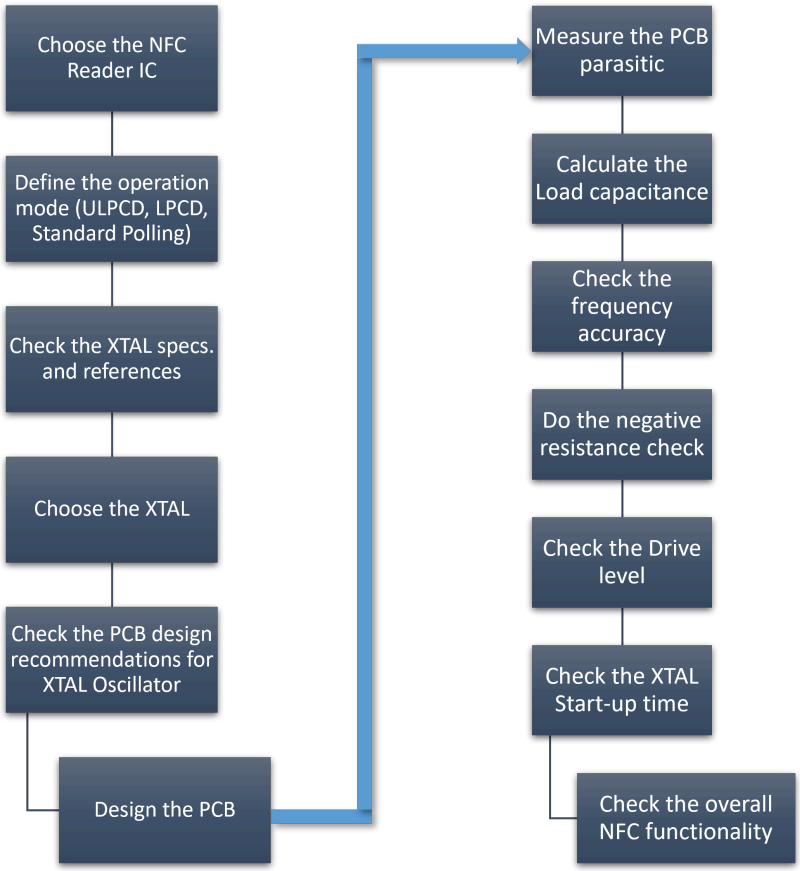

Figure 1. Simplified design flowchart

3 XTAL oscillator - theory

NXP NFC Controllers/Frontends use a Pierce oscillator structure which consists of two parts: An active part which is inside the NFCC and a passive part which is connected externally. The active part is an inverter amplifier which is represented as transconductance "*gm*". The passive part consists of an XTAL oscillator (XTAL) and two loading capacitors (CL1 and CL2). Find the basic structure in Figure 2.

As shown in Figure 2, there are also parasitic capacitances which have to be considered during the PCB design and the load capacitance calculation (see Section 4 and Section 9).

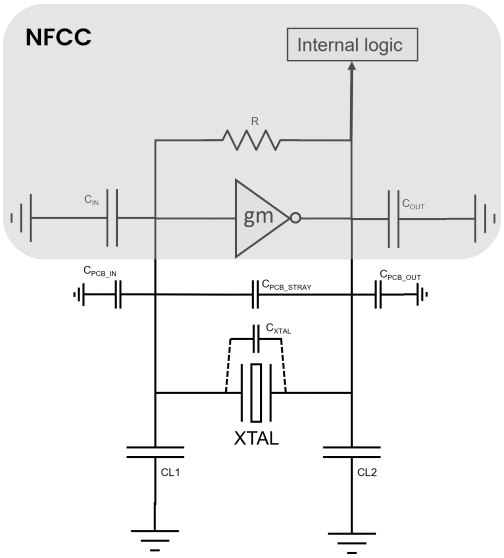

Figure 2. Pierce oscillator in NFC Controller

The crucial part of the Pierce oscillator is a quartz oscillator (XTAL) which contains a crystal element enabling oscillation at certain frequency. For NFC, the frequency is typically **27.12MHz.** The electrical model of the XTAL is shown in Figure 3:

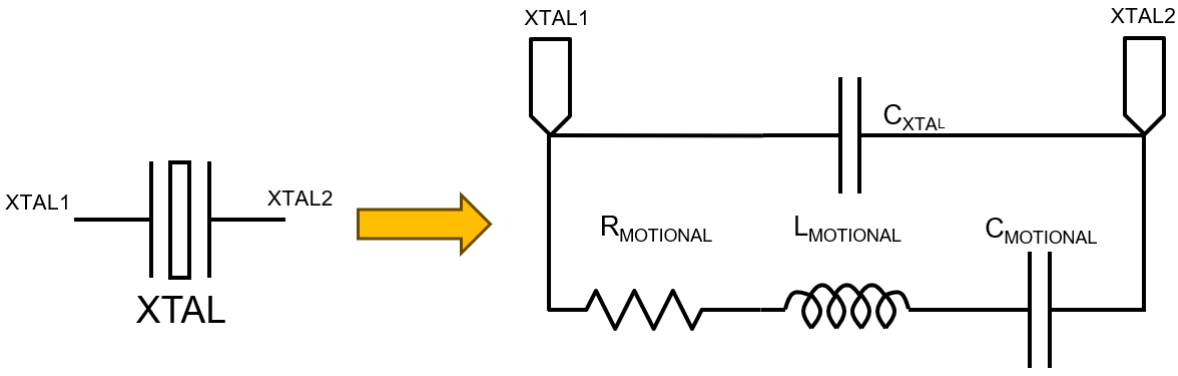

Figure 3. XTAL Model

- $R_{MOTIONAL}$ → Motional Resistance of the XTAL (Equivalent Series Resistance known as **ESR**)
- $L_{MOTIONAL}$ → Motional Inductance of the XTAL
- $C_{MOTIONAL}$ → Motional Capacitance of the XTAL
- C_{XTAL} → Shunt Capacitance of the XTAL

4 XTAL oscillator - load capacitance

The XTAL load capacitance is one of the crucial parameters in the oscillator design which defines the oscillation frequency. The goal is to match the overall capacitance of the design (including external load capacitors and all parasitic capacitances) to the nominal load capacitance defined by the XTAL manufacturer.

For example, if the nominal load capacitance of the XTAL defined by the manufacturer is 10 pF, then the PCB design and the selection of all external components should ideally be done in such way that the overall capacitance connected to the XTAL equals 10 pF.

See the “capacitive” Pierce oscillator model in Figure 4. This model includes all parasitics that might influence the final load capacitance connected to the XTAL.

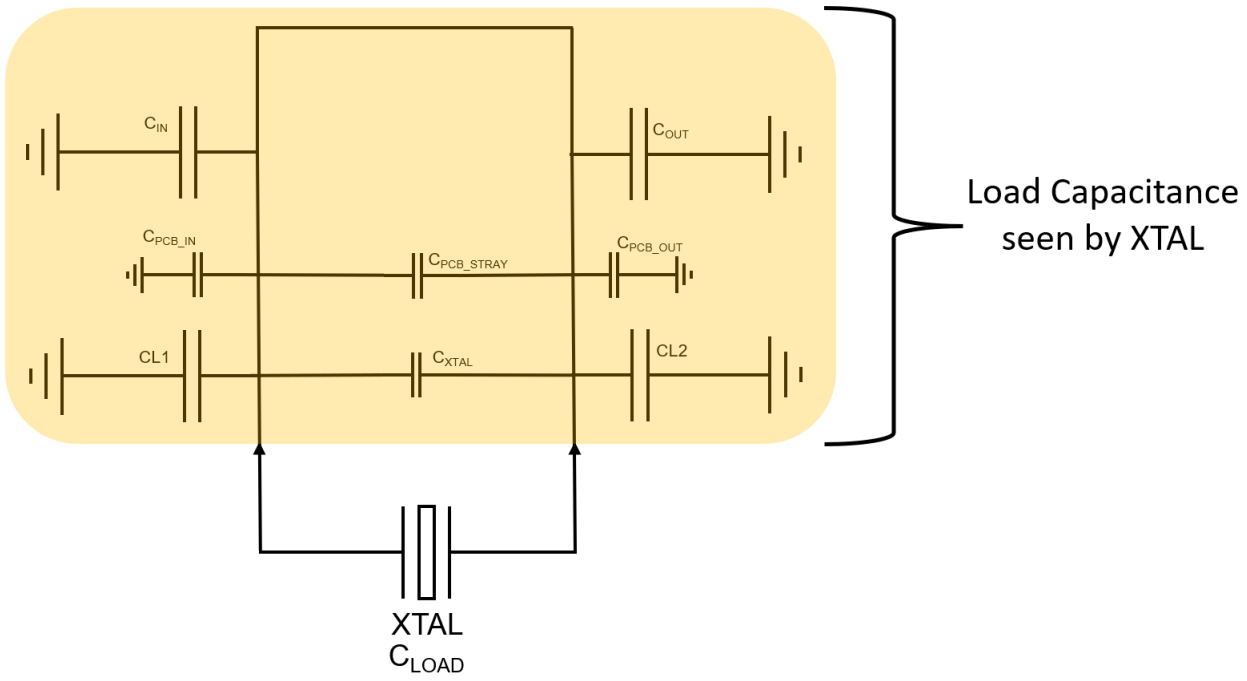

Figure 4. XTAL Load Capacitance model

- C_{LOAD} → Nominal Load Capacitance given by the XTAL manufacturer
- C_{L1} and C_{L2} → External loading capacitors
- C_{XTAL} → XTAL Shunt capacitance
- C_{PCB_STRAY} → Stray capacitance of the PCB
- C_{PCB_IN} and C_{PCB_OUT} → Parasitic capacitance of the input and output PCB traces
- C_{IN} and C_{OUT} → Capacitance of the PN7160 XTAL input and output pins

4.1 XTAL external load capacitors

For the adjustment of the load capacitance connected to XTAL, there are two external capacitors used, C_{L1} and C_{L2}. Their values can be calculated using the following formula:

$$C_{LOAD} = \frac{(C_{IN}+C_{PCB\_IN}+C_{L1})*(C_{OUT}+C_{PCB\_OUT}+C_{L2})}{(C_{IN}+C_{PCB\_IN}+C_{L1})+(C_{OUT}+C_{PCB\_OUT}+C_{L2})} + (C_{PCB\_STRAY} + C_{XTAL})\ (pF)$$

Figure 5. External load capacitance - formula

The C_{LOAD} and C_{XTAL} can be extracted from the XTAL data sheet.

It is recommended to measure the remaining capicitance using a Vector Network Analyzer directly on the PCB. Find recommendations for the VNA settings below:

- Set the center frequency 27.12 MHz
- Set the span frequency 100kHz
- Use, for example, the "pin header" probe and calibration kit as shown in Figure 6.
  Note: *Do not touch the PCB and the GND of coax during the measurement.*

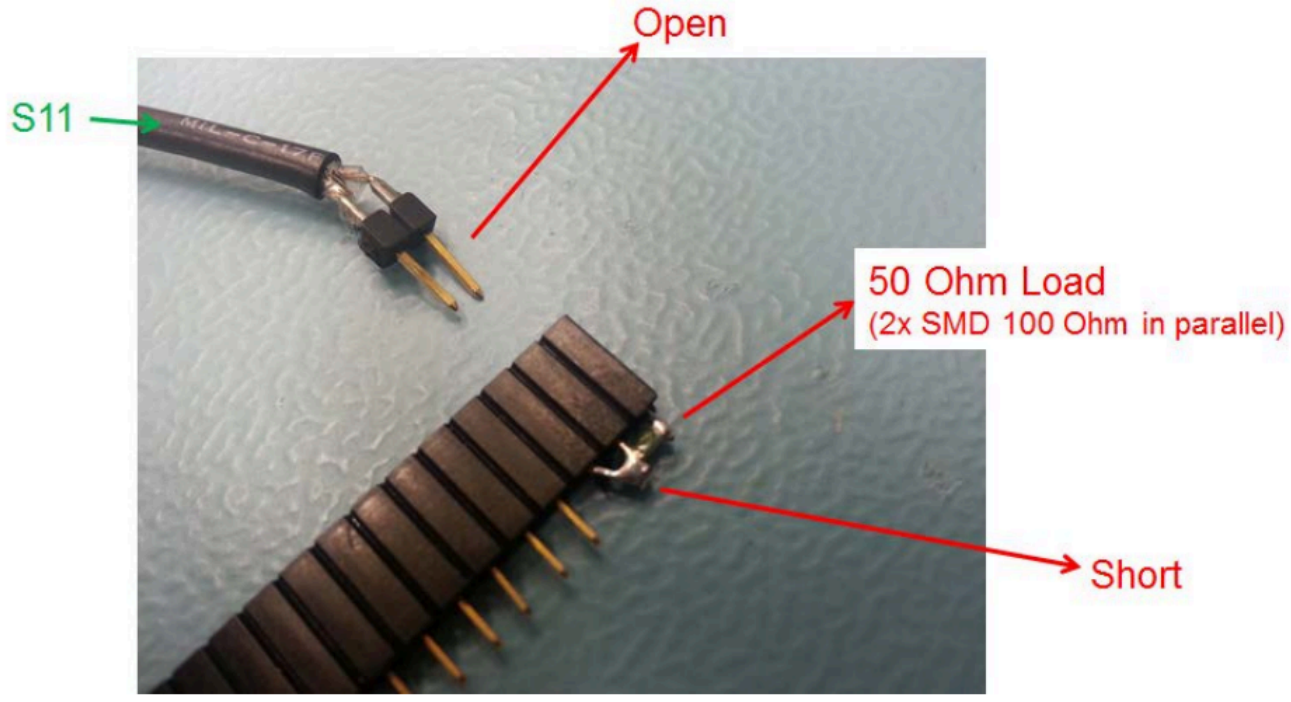

Figure 6. "Pin header" probe + calibration kit

- Measure the parasitic capacitance on the PCB as shown in Figure 7. For optimal measurement results, place the probes as close as possible to the XTAL pads.
- Based on the obtained results, the following parameters can be defined.
  - XTAL_CLK1 to GND → $C_{IN} + C_{PCB\_IN}$
  - XTAL_CLK2 to GND → $C_{OUT} + C_{PCB\_OUT}$
  - XTAL_CLK1 to XTAL_CLK2 → C_{PCB_STRAY}

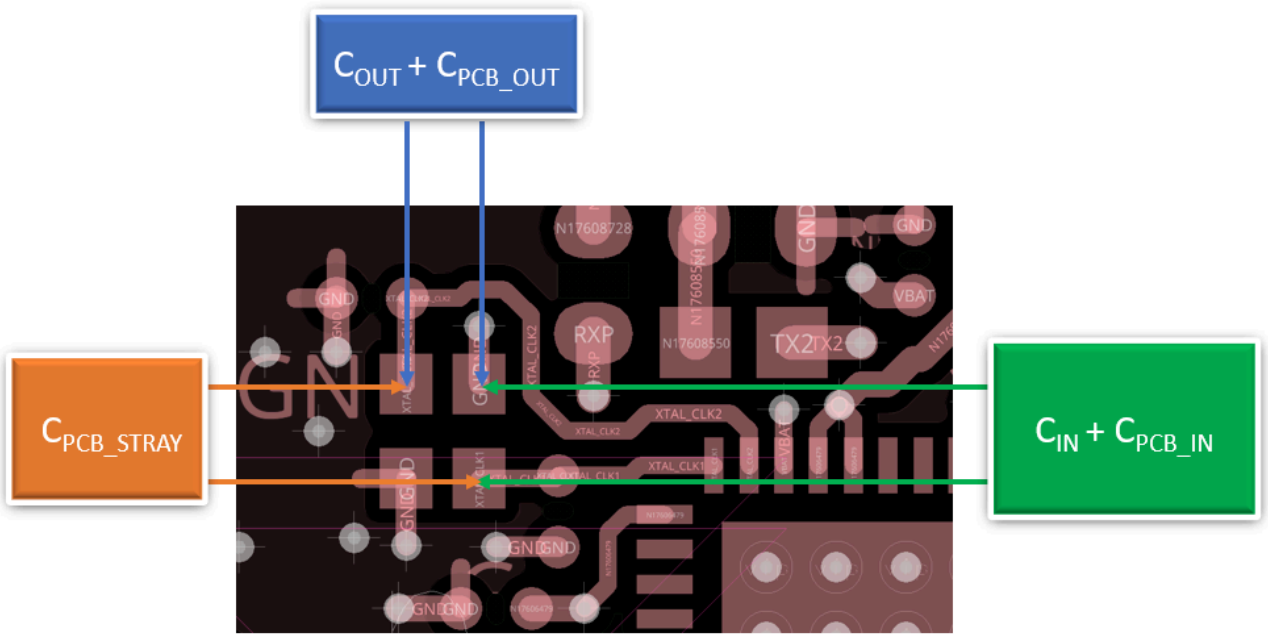

Figure 7. Parasitic capacitance measurement

For this measurement, the XTAL and external load capacitors have to be removed from the PCB. The NFC Controller stays assembled but it is not powered.

5 XTAL oscillator - frequency accuracy

In NFC systems, the carrier frequency is 13.56 MHz. The carrier frequency is based on the clock signal generated by the XTAL oscillator. Therefore, If the carrier frequency is **13.56 MHz**, the XTAL oscillator should generate exactly **27.12 MHz**. The signal is then divided by two and directly used for the carrier wave generation of the NFCC TX driver.

As the XTAL is a sensitive component, its output frequency can be influenced by temperature changes and the tolerances of every component in the PCB design. Therefore, regulatory authorities such as the FCC, ETSI, KCC, and ISO, allow an offset to the carrier frequency in *ppm* (parts per million). Find some examples below:

- FCC → ± 100ppm
- KCC → ± 100ppm
- ISO 14443 → ± 516 ppm
- FeliCa global → ± 50 ppm

Note: *Always check with a standardization expert for the actual limits.*

5.1 Frequency accuracy - check

The frequency accuracy (pullability) is given in ppm. Ideally, if the capacitance connected to the XTAL matches with the nominal XTAL capacitance, the ppm value is 0.

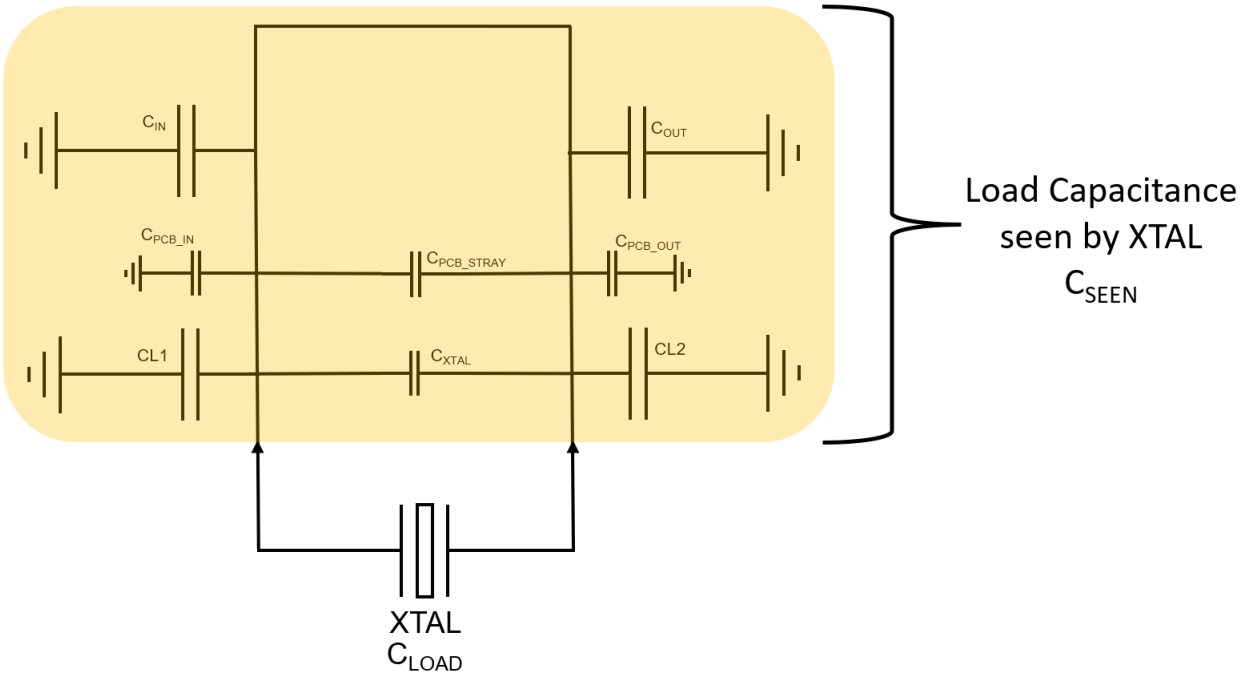

Figure 8. Load capacitance connected to the XTAL

The target is $\mathbf{C_{LOAD} = C_{SEEN}}$, but sometimes, for example, due to faster start-up time or an increase of the negative resistance absolute value, it can be necessary to slightly detune the XTAL,

The pullability can be calculated with the following formula:

$$ppm = \frac{C_m*(C_{LOAD}-C_{SEEN})}{2*C_{LOAD}*C_{SEEN}} * 10^6$$

Figure 9. XTAL pullability - formula

See an example of the ppm and loading capacitance connected to the XTAL in Figure 10. The calculation has performed for an XTAL with nominal C_{LOAD} = 10 pF.

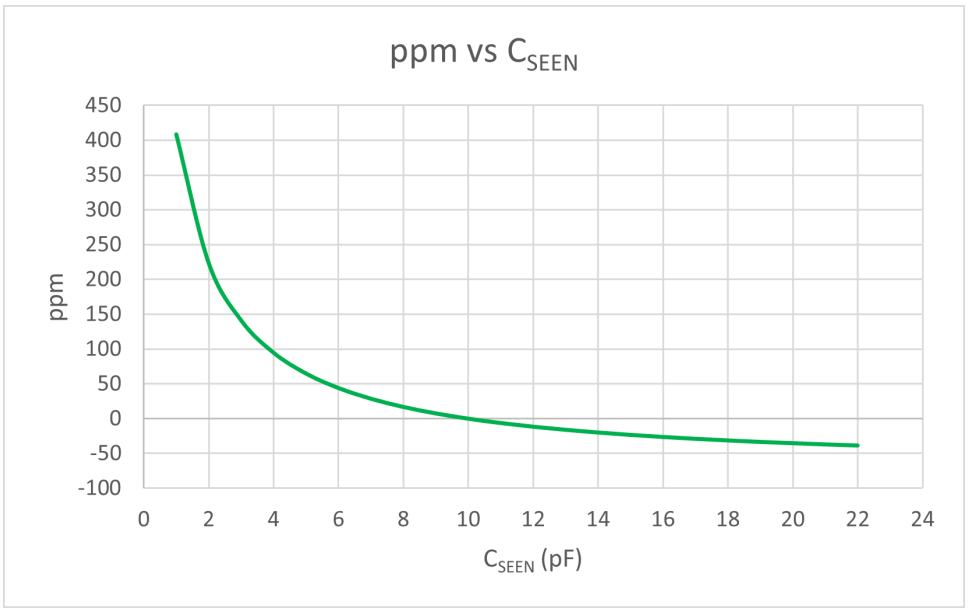

Figure 10. ppm over loading capacitance connected to the XTAL

The direct measurement of the XTAL frequency might not be accurate when a probe of a scope or spectrum analyzer is connected to the oscillator circuit as it adds an additional load. To minimize the inaccuracy of the measurement, an "indirect" measurement approach can be used for the RF carrier frequency .

Theoretically, the **frequency of the RF Carrier wave is half of the XTAL Oscillator loaded frequency** → 2 * f_c = f_{xtal}. Therefore, users can perform a simple test with a scope or spectrum analyzer to check the RF Field and its frequency. The carrier frequency shall be within in the limits and tolerances described in Section 5.

The measurement can be peformed with either:

- a suitable scope with a high sample rate and FFT support, or
- a spectrum analyzer.

Find the measurement setup in Figure 11.

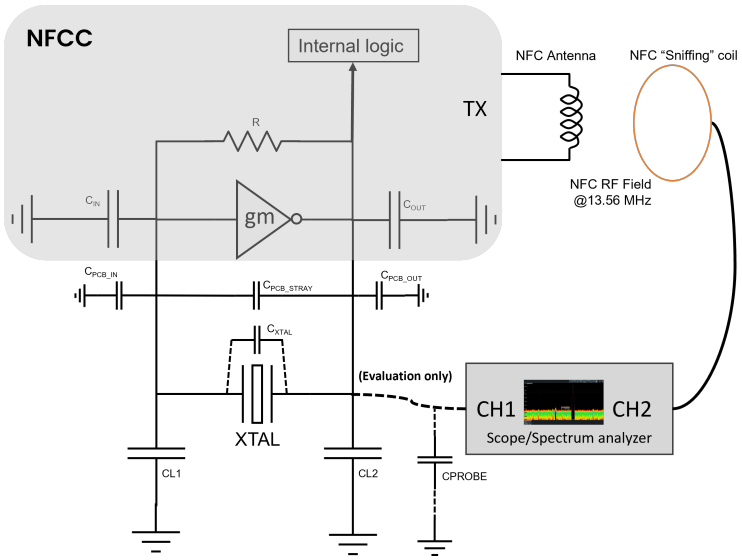

Figure 11. Measurement setup - Block diagram

Note: *For the final measurement, the CH1 must be disconnected.*

For the RF signal sniffing, a basic loop from the scope probe can be used as shown in Figure 12.

Figure 12. Measurement setup

The measurement is performed with a continous RF_ON signal. The frequency of the radiated carrier frequency is measured.

See an example of the measurement in Figure 13, the following FFT settings were used:

- Center frequency → 13.56 MHz
- Frequency span → 50 kHz
- Resolution BW → 500 Hz
- Window type → Blackman Harris

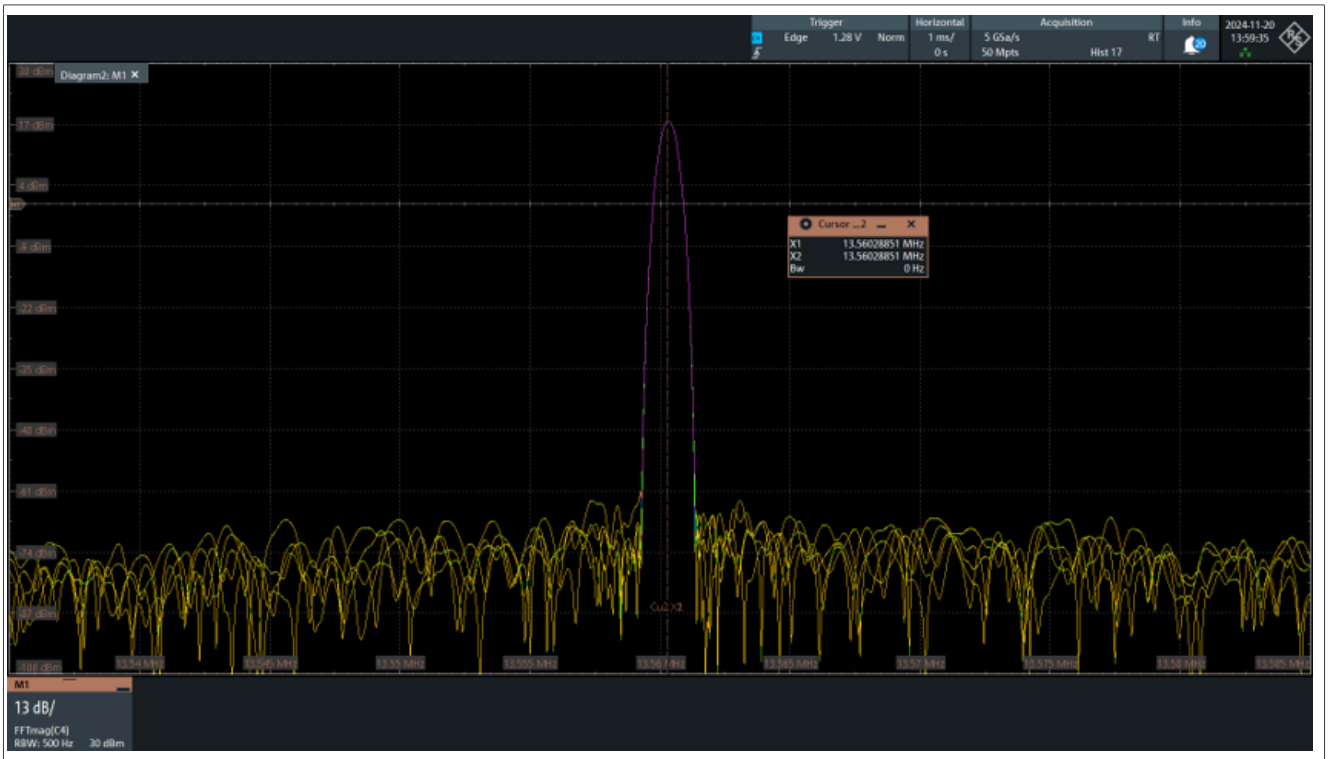

Figure 13. CL1 & CL2 = 10 pF

Find results in the table below.

Table 1. Measurement results for different load capacitances

CL1 and CL2 (pF)	Measured frequency (Hz)	Offset from 13.56 MHz (ppm)
10	13 560 289	+21
12	13 560 136	+10
15	13 559 983	-1.25

If the frequency offset is too high, the load capacitors must be adjusted accordingly.

6 XTAL oscillator - negative resistance

Negative resistance of the oscillator (**-R**) is an important parameter which defines the oscillation stability and reliable start of the oscillator. The negative resistance "compensates" the losses in the oscillator circuit caused by XTAL Equivalent Series Resistance (**ESR**).

The theoretical condition for XTAL oscillation is $|-R|$ **= ESR**. There is no margin for this condition, and even a small change in the circuit (for example, due to the component tolerances, changes in temperature or humidity), the XTAL might not perform properly. Therefore, it is recommended to have the negative resistance 5 times higher than the ESR of the XTAL to allow for all operating conditions.

$$|-R|*5 = \mathbf{ESR}$$

The negative resistance is defined by the following parameters:

- **gm** → Transconductance of the inverter amplifier
- $\mathbf{C_{L1}}$ and $\mathbf{C_{L2}}$ → External loading capacitors
- $\mathbf{C_{XTAL}}$ → XTAL Shunt capacitance
- $\mathbf{C_{PCB\_STRAY}}$ → Stray capacitance of the PCB
- $\mathbf{C_{PCB\_IN}}$ and $\mathbf{C_{PCB\_OUT}}$ → Parasitic capacitance of the input and output PCB traces
- $\mathbf{C_{IN}}$ and $\mathbf{C_{OUT}}$ → Capacitance of the XTAL input and output pins

The applied negative resistance against the ESR of the XTAL can be calculated using the following formula:

$$Re(Z) = \frac{-\{g_m*(C_{L1}+C_{IN}+C_{PCB\_IN})*(C_{L2}+C_{OUT}+C_{PCB\_OUT})\}}{\left\{\omega^2*\left[(C_{L1}+C_{IN}+C_{PCB_{IN}})*(C_{L2}+C_{OUT}+C_{PCB_{OUT}})+(C_{L1}+C_{IN}+C_{PCB_{IN}})*(C_{XTAL}+C_{PCB_{STRAY}})+(C_{L2}+C_{OUT}+C_{PCB_{OUT}})*(C_{XTAL}+C_{PCB_{STRAY}})\right]^2+\left[g_m*(C_{XTAL}+C_{PCB_{STRAY}})\right]^2\right\}} \ (\Omega)$$

Figure 14. Applied negative resistance formula

See examples of the negative resistance and load capacitances for different oscillator parameters below.

Figure 15 shows the influence of the PCB stray capacitance on the negative resistance value applied against the ESR of the XTAL. As shown in the figure, lower PCB stray capacitance leads to higher achievable absolute negative resistance.

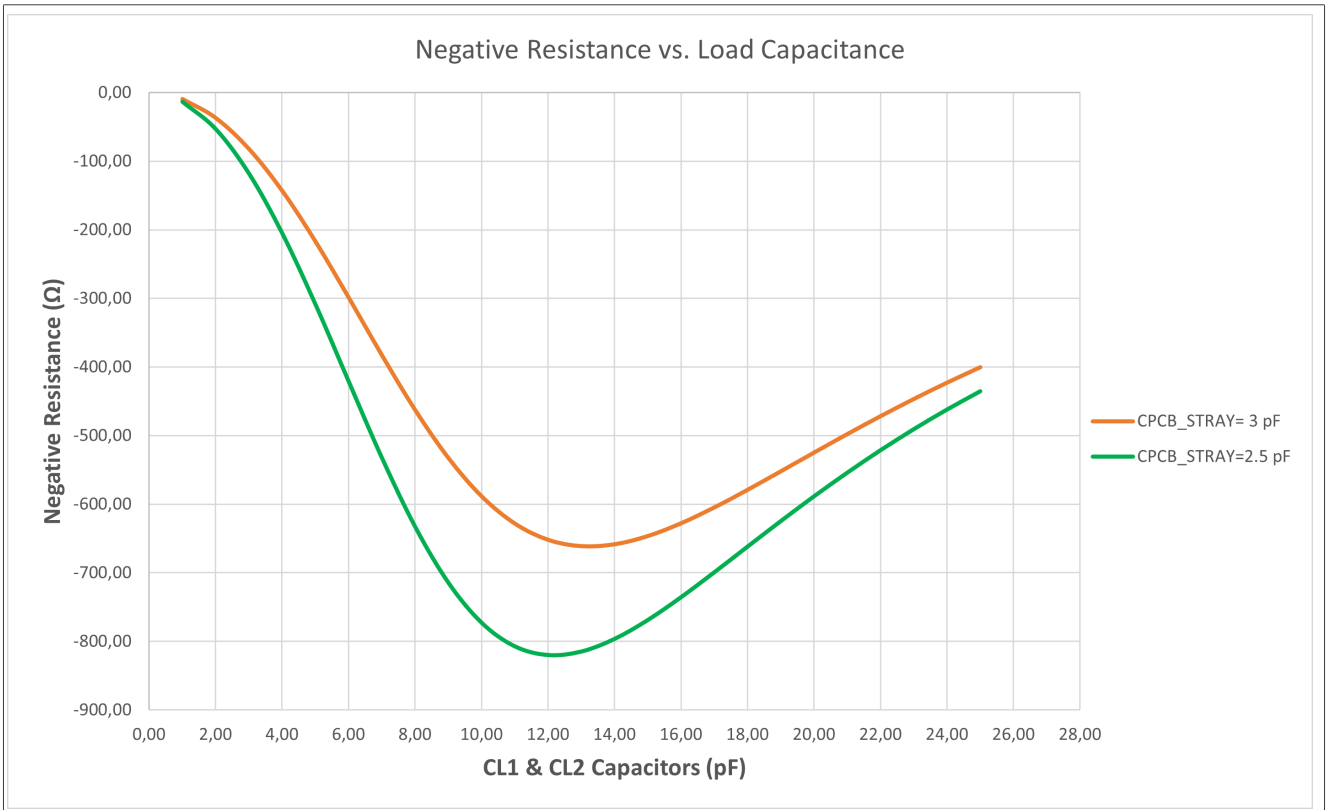

Figure 15. Negative Resistance vs. Load Capacitance, different C_{PCB_STRAY}

The same applies for the C_{XTAL} (XTAL Shunt capacitance) shown in Figure 16. Lower XTAL stray capacitance leads to higher achievable absolute negative resistance.

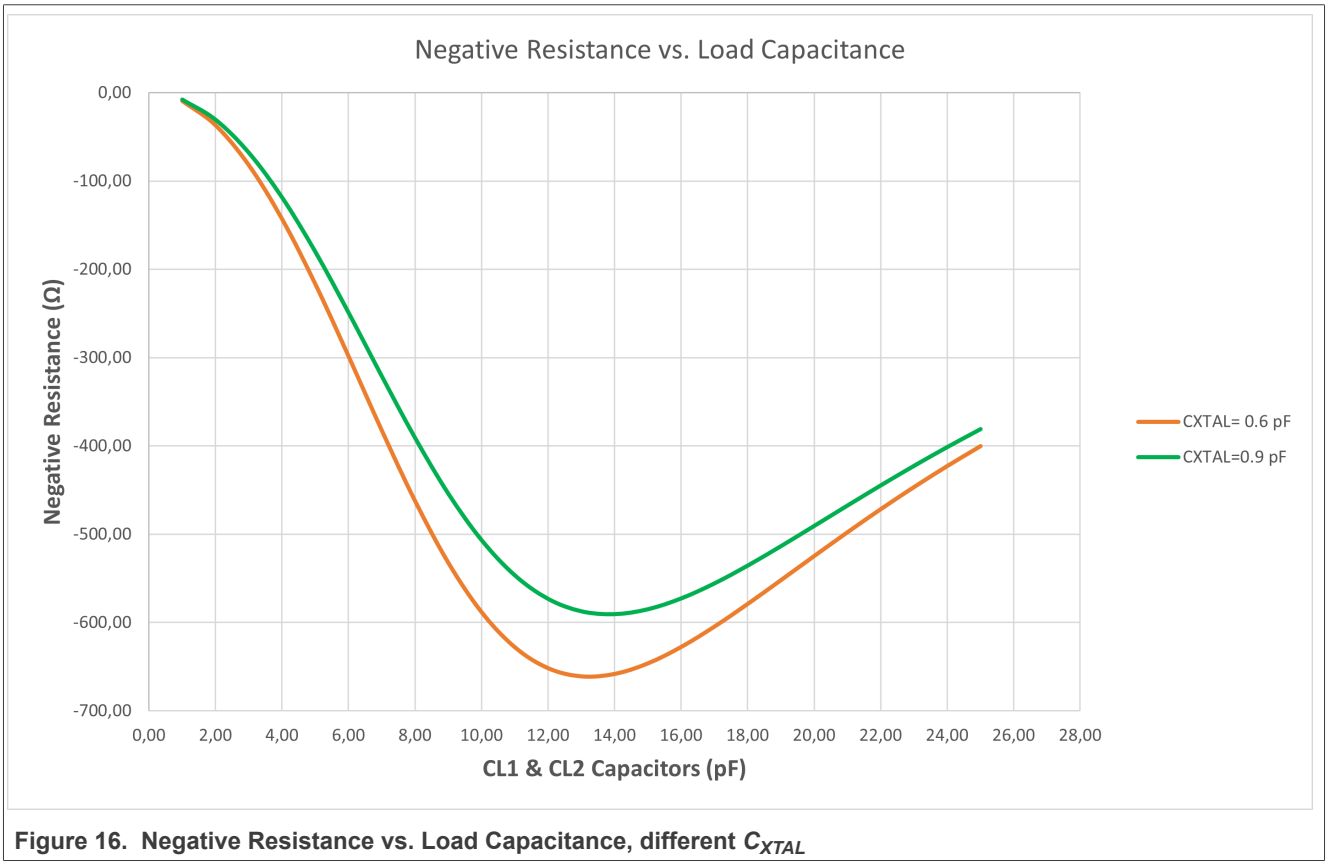

Figure 16. Negative Resistance vs. Load Capacitance, different C_{XTAL}

Figure 17 shows the behavior of the negative resistance over load capacitance for different values of the inverter transconductance "*gm*". The transconductance depends on the type of the inverter used (for example, a different NFC controller) and its supply voltage. The value may slightly vary for different ambient temperatures.

Figure 17. Negative Resistance vs. Load Capacitance, different *gm*

6.1 Negative resistance - check

For a quick check if the design has enough negative resistance compared to the ESR of the XTAL in use, a simple test can be performed. Follow the steps below:

- Check the ESR_{max} of the used XTAL in the data sheet
- Connect a resistor R_{TEST} which is approximately 5 times higher than ESR_{max}
  - for example, If ESR_{max} = 100 Ω, then R_{TEST} = 510 Ω
- Check if the XTAL starts to oscillate
  - Check for the minimum and maximum required operating temperature
  - Check for a different ICs

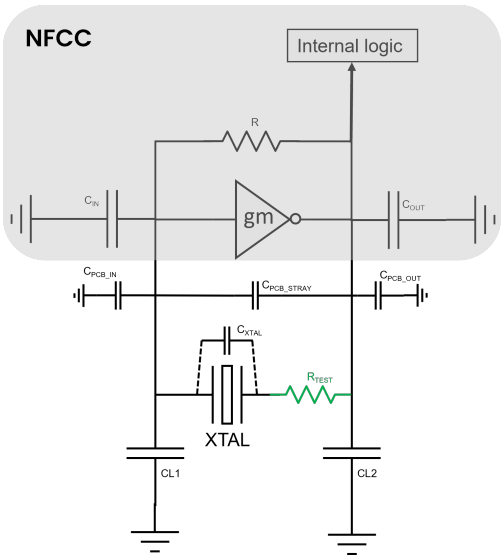

Figure 18. Negative resistance test

If the XTAL does not start to oscillate or the oscillation is not stable enough, the following measures have to be considered:

- Increasing the "*gm*" value of the NFCC inverter block
- Using a different XTAL with a lower ESR
- Adjusting the CL1 and CL2 capacitors (typically, increasing their value)
  - This might be at the cost of frequency accuracy.
- Reducing the C_{PCB_STRAY} capacitance of the PCB
  - Lower C_{PCB_STRAY} leads to higher negative resistance absolute value.

7 XTAL drive Level

XTAL drive level (**DL**) defines the power dissipation of the XTAL unit. This value is typically in the range of tens to hundreds of µW and is defined by the XTAL manufacturer in the data sheet.

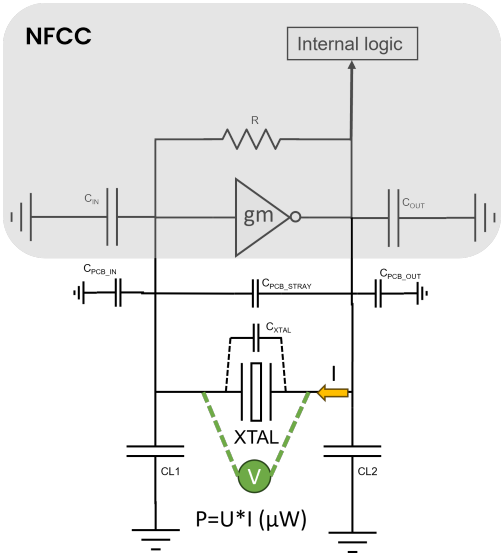

Figure 19. XTAL drive level

It is important to check the XTAL drivel level during oscillation. Make sure that the value is under the maximum value specified in the XTAL data sheet.

7.1 Drive level - check

The most reliable way to check the drive level of the XTAL is to measure voltage and current direcly on the XTAL. Then, calculate the resulting power as shown in Figure 20. This measurement requires a current probe which might no always be available.

However, if the resistance (ESR) of the XTAL is known, the voltage can be measured and the drive level calculated accordingly.

For the voltage measurement, it is recommended to use a Differential Active Probe with low capacitance (max.1pF).

The drive level can be calculated using the following formula:

$$Drive\ Level\ (DL) = \mathrm{ESR} * \left(\pi * f * \frac{V_{pp}}{\sqrt{2}} * (C_{LOAD} + C_{PROBE})\right)^2$$

Figure 20. Drive level - Formula

where:

- **ESR** - Equivalent Series Resistance of the XTAL
- **Vpp** - Measured peak-to-peak voltage
- **C_{LOAD}** - XTAL load capacitance → Figure 5
- **C_{PROBE}** - Parasitic capacitance of the scope probe
- **f** - Oscillation frequency

If the resulting drive level is too high, a damping resistor ($R_{DAMPING}$) can be used to reduce the drive power (see Figure 21).

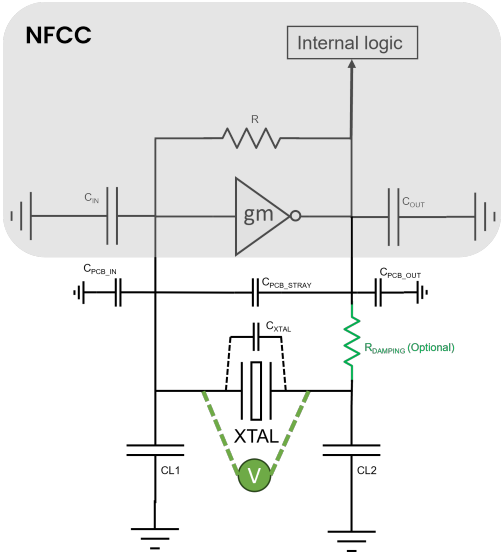

Figure 21. ($R_{DAMPING}$ in placement

Note: *As the ESR value of the XTAL might have a large range (for example, Min. = 15 Ω, Nom. = 25 Ω, and Max. = 100 Ω), it is recommended to cooperate with the XTAL vendor/manufacturer.*

8 XTAL start-up

Start-up time is the time between an oscillator being first turned on and the NFC controller detecting the clock signal using its "clock detection" mechanism.

The required time can differ depending on the NFC controller and the detection mechanism in use (ULPCD, LPCD, Standard "digital" Polling).

- For the PN7160, the XTAL start-up time is maximum **3 ms**, typically around **1 ms**.
- For the PN5190/PN7642/PN7220, the XTAL start-up time is typically **1 ms** for normal operation and **400 µs** for Ultra Low Power Card Detection (ULPCD)

See the typical XTAL start-up sequence for standard digital polling in Figure 22.

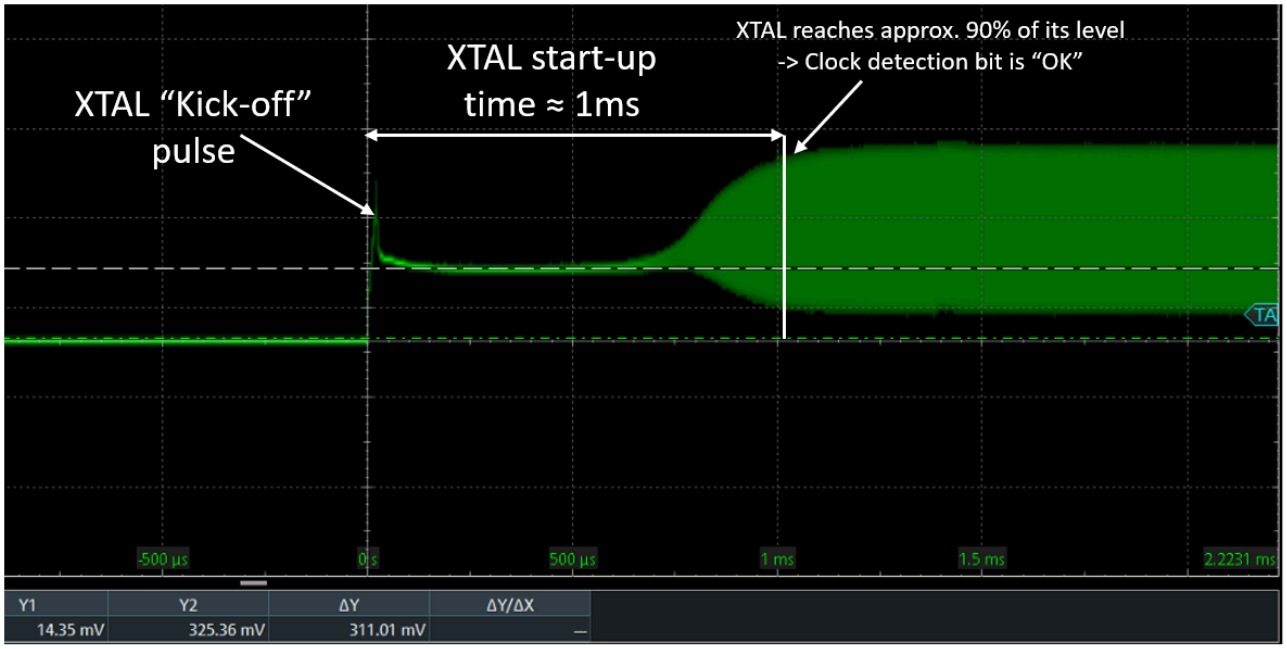

Figure 22. XTAL start-up

The start-up time is influenced by multiple factors:. For example, it can be reduced by:

- XTAL Parameters
  - Low C_{XTAL} Shunt capacitance
  - High $C_{MOTIONAL}$
  - Low C_{LOAD}
- PCB Parameters
  - Low C_{PCB_STRAY}
- NFC controller Parameters:
  - High "**gm**" Transdocuntance of the internal inverted block

The effect of each parameter listed above has been simulated and compared. See the results in Section 11.

8.1 XTAL start-up - check

The XTAL start-up can be measured directly by probing the XTAL2 pin (XTAL oscillator output) and sniffing the generated RF Field as shown in Figure 23. For this measurement, it is recommended to use an active low capacitance probe (max. 1pF) to minimize the measurement uncertainties as much as possible.

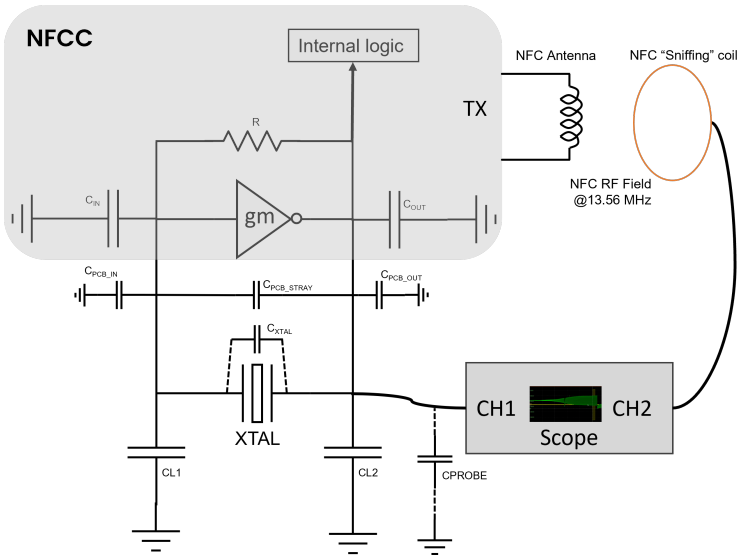

Figure 23. XTAL Start-up measurement - direct method

Note: *The scope probe adds an extra capacitance to the oscillator circuit. Thus, the real start-up time is slightly lower than the one measured.*

Find an example of the XTAL start-up sequence in Ultra Lower Power Card Detection mode in Figure 24.

Figure 24. XTAL Start-up in ULPCD mode

Green signal → XTAL2

Yellow signal → RF Field

9 XTAL layout recommendations

The PCB introduces some parasitics, which must be considered and minimized during the PCB design. The stray capacitance of the PCB (C_{PCB_STRAY}) might influence the XTAL start-up significantly. Find a simplified illustration showing most of the PCB parasitics in Figure 25. In general, the XTAL must be connected as close as possible to the CLK1 and CLK2 pins from the NFCC to achieve the best performance possible. Find more design recommendations below:

- As the XTAL is sensitive to parasitic capacitance and noise, it is advised to:
  - place the XTAL far from other signals (especially other CLK lines or signals with frequent switching);
  - place the XTAL far from heat sources;
  - limit the crosstalk between CLK lines and other signals.
- Load capacitor connections:
  - Choose a capacitor with a good temperature stability such as COG/NP0 and a maximum tolerance of 2%.
  - Place the capacitors close to each other and to the XTAL.
  - Avoid connecting them to dirty ground.
- PCB layout (see an example in Figure 28):
  - XTAL1 and XTAL2 traces should be as short as possible to reduce C_{PCB_IN} / C_{PCB_OUT} parasitic capacitance.
  - Increase the spacing ("*d*") between XTAL1 and XTAL2 to reduce the C_{PCB_STRAY}.
  - If possible, route the XTAL1 and XTAL2 traces symmetrically (same length).
  - Do not use vias for XTAL1 and XTAL2 traces.
  - Use a “keep-out” area around the crystal unit. The GND connection should use vias to the next GND layer. .

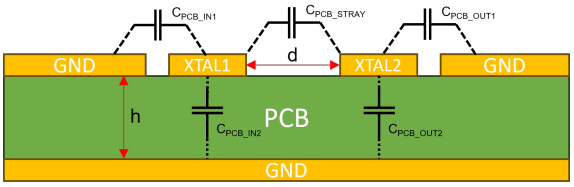

Figure 25. Illustration of the PCB Parasitics

The stray and parasitic capacitances can be estimated using the formulas described in Figure 26.

$$C_{PCB\_STRAY} = \frac{\varepsilon_{free\_space} * \varepsilon_{r-air} * l * w}{d} \text{ (pF)}$$

Figure 26. PCB Stray capacitance calculation

$$C_{PCB\_IN2}/C_{PCB\_OUT2} = \frac{\varepsilon_{free\_space} * l * w * \varepsilon_{r-pcb}}{h} \text{ (pF)}$$

Figure 27. Parasitic capacitance calculation

- $\varepsilon_{r\text{-free air}}$ - vacuum permittivity
- $\varepsilon_{r\text{-PCB}}$ - relative permittivity of the PCB
- l - length of the trace
- w- width of the trace
- d - distance between traces
- h - height of the PCB

Find an example of PCB layout in Figure 28.

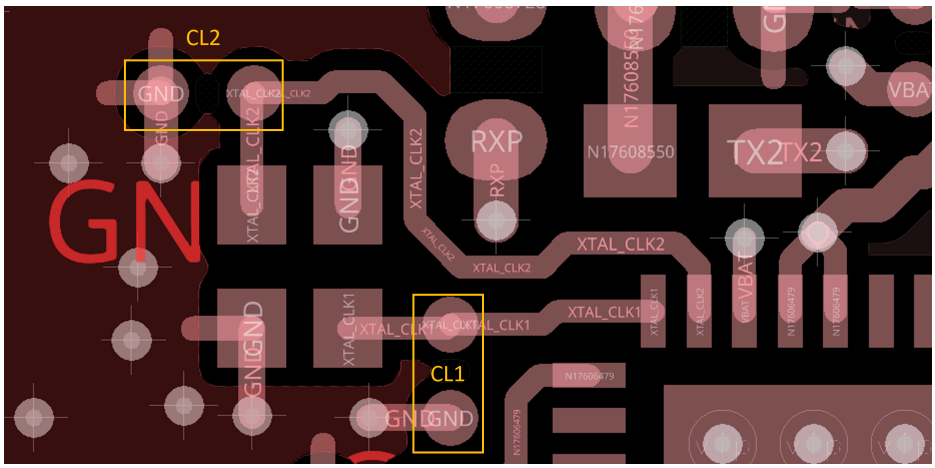

Figure 28. XTAL PCB layout example

10 XTAL references

Each NFCC from the NXP portfolio may require an XTAL with differing parameters due to different clock block implementations and/or requirements for start-up timing (ULPCD, LPCD, or Standard digital polling).

NFCC clock interfaces with XTAL oscillators have been verified with several references as shown in Section 10. Other crystal units might be suitable for the specified usage, but only those discussed within this document have been validated by NXP.

When using a different XTAL, frequency accuracy, drive level, nominal load capacitance, and ESR must be carefully selected according to the specification provided in each product data sheet.

10.1 XTAL references - PN5190/PN7642/PN7220

The recommended XTAL specifications are provided in the PN5190B1, PN5190B2, PN7642 and PN7220 product data sheets.

See the list of XTAL References in Table 2.

Table 2. XTAL references - PN5190/PN7642/PN7220

XTAL Manufacturer	XTAL Part Number	Note
TXC	8J27170001	Supports also ULPCD
EPSON	FA-118T 27.1200MD50Z-K3	Only for LPCD and Standard polling
NDK	NX2016SA 27.12 MHz EXS00A-CS06346	Only for LPCD and Standard polling

10.2 XTAL references - PN7160/PN7161

The recommended XTAL specification is provided in the PN7160 product data sheet.

See the list of XTAL References in Table 3.

Table 3. XTAL references - PN7160

XTAL Manufacturer	XTAL Part Number	Note
NDK	NX2016SA 27.12 MHz EXS00A-CS06346	-
NDK	NX2016HA 27.12 MHz EXS00A-CH00075	-
MURATA	XRCGB27M120F3M10R	-

Note: *For PN7160, it is important to use a crystal with* ***nominal load capacitance 10pF****. Lower value might lead to low negative resistance and then issues with the XTAL start-up. If a crystal with lower nominal capacitance is used, e.g, 8pF, the customer would need to increase the load capacitance seen by XTAL (mainly by CL1 and CL2) at the cost of frequency accuracy. See Section 5.1.*

10.3 XTAL references - CLRC663 plus Family

The recommended XTAL specification is provided in the CLRC663 plus Family product data sheet.

See the list of XTAL References in Table 4.

Table 4. XTAL references - CLRC663 plus Family

XTAL Manufacturer	XTAL Part Number	Note
MURATA	XRCGB27M120F3M10R0	-

10.4 XTAL references - PN5180

The recommended XTAL specification is provided in the PN5180 product data sheet.

See the list of XTAL References in Table 5.

Table 5. XTAL references - PN5180

XTAL Manufacturer	XTAL Part Number	Note
TXC	7M-27.120MEEQ-T	-

10.5 XTAL references - PN7462 Family

The recommended XTAL specification is provided in the PN7462 Family product data sheet.

See the list of XTAL References in Table 6.

Table 6. XTAL references - PN7462 Family

XTAL Manufacturer	XTAL Part Number	Note
EPSON	Q22FA12800034	-

11 Annex 1: XTAL start-Uup time simulations

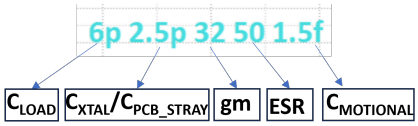

Figure 29. XTAL Start-Up - Legend

11.1 Different C_{LOAD}

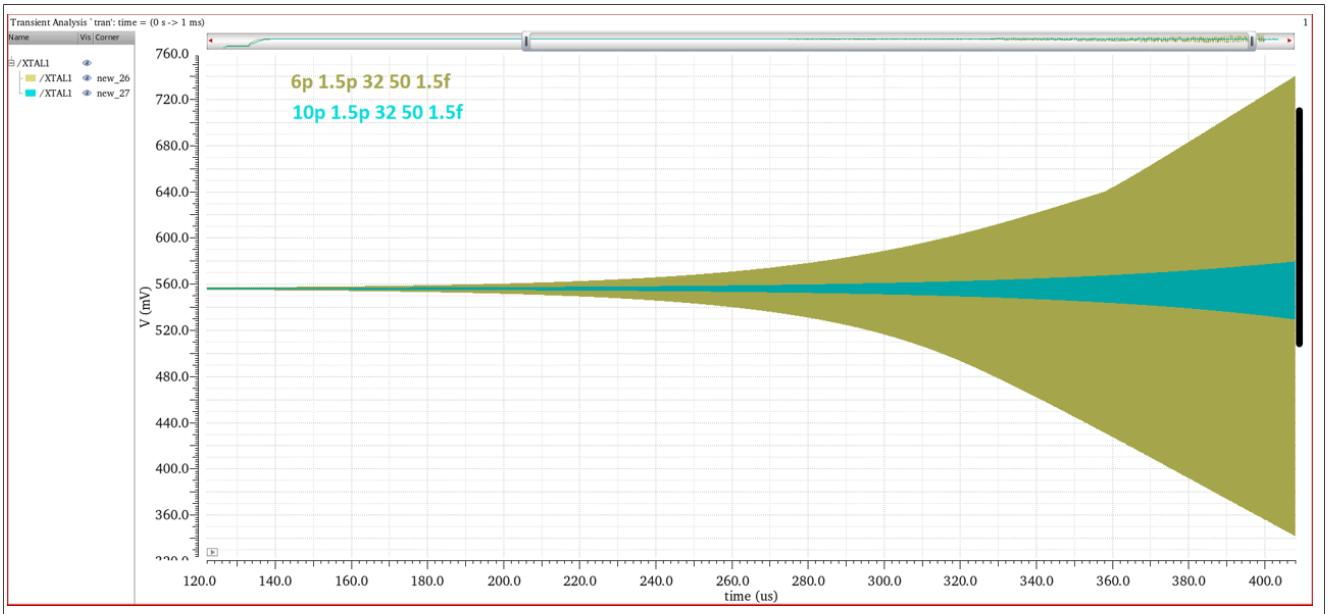

Figure 30. XTAL Start-Up, C_{LOAD} = 10 pF and 6 pF

11.2 Different $C_{MOTIONAL}$

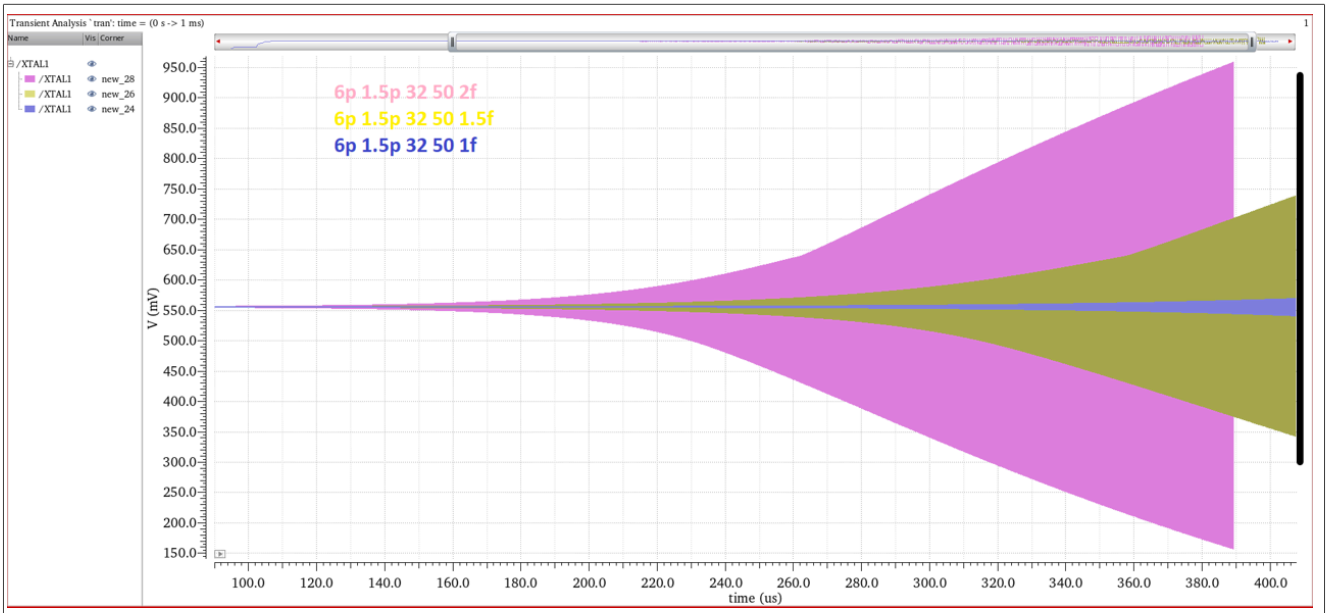

Figure 31. XTAL Start-Up, $C_{MOTIONAL}$ = 1 fF, 1.5 fF, 2 fF

11.3 Different C_{SHUNT}

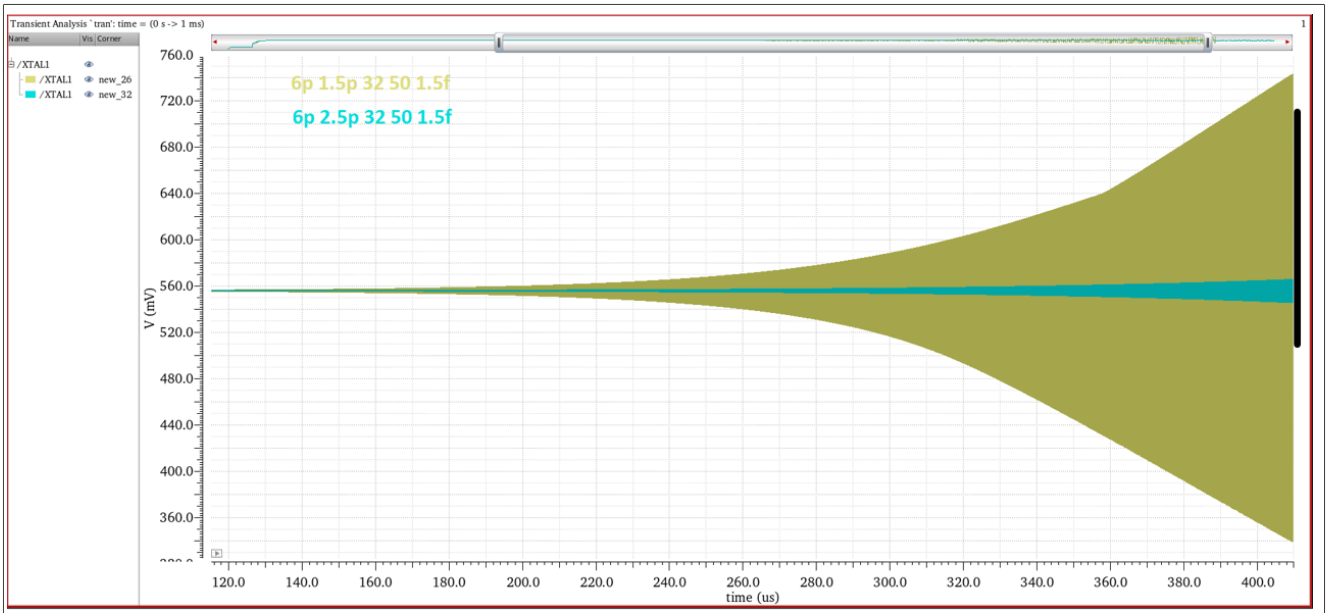

Figure 32. XTAL Start-Up, C_{XTAL} + C_{PCB_STRAY} = 1.5 pF and 2.5 pF

11.4 Different ESR

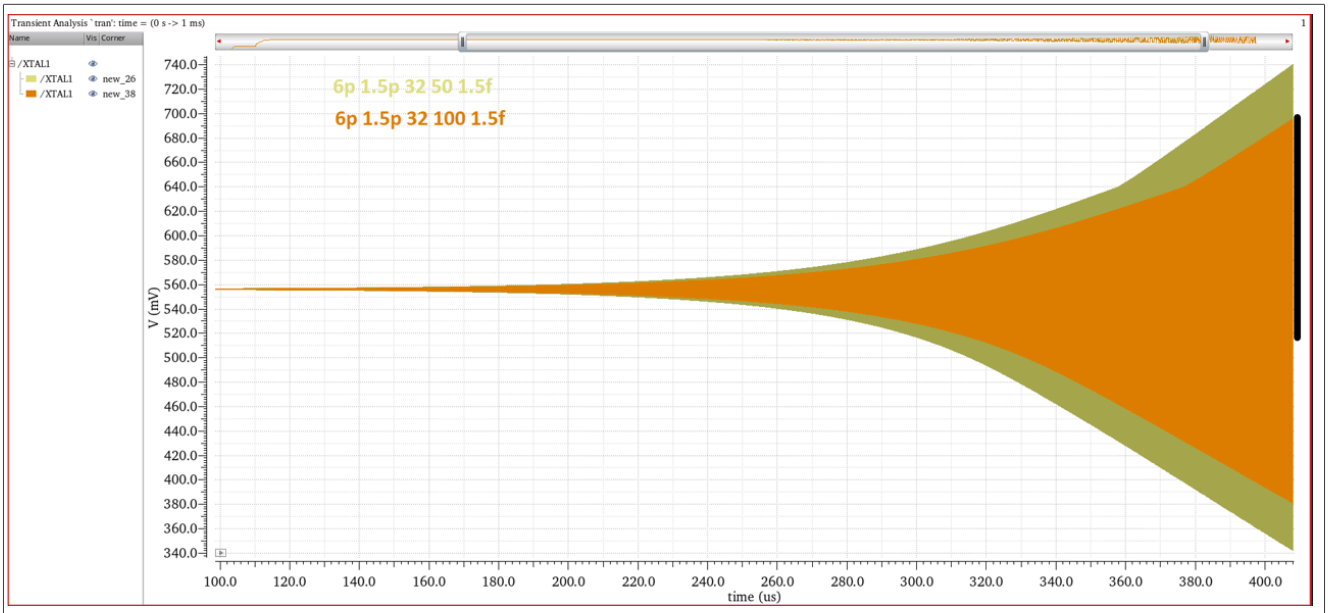

Figure 33. XTAL Start-Up, ESR = 50 Ω and 100 Ω

11.5 Different gm

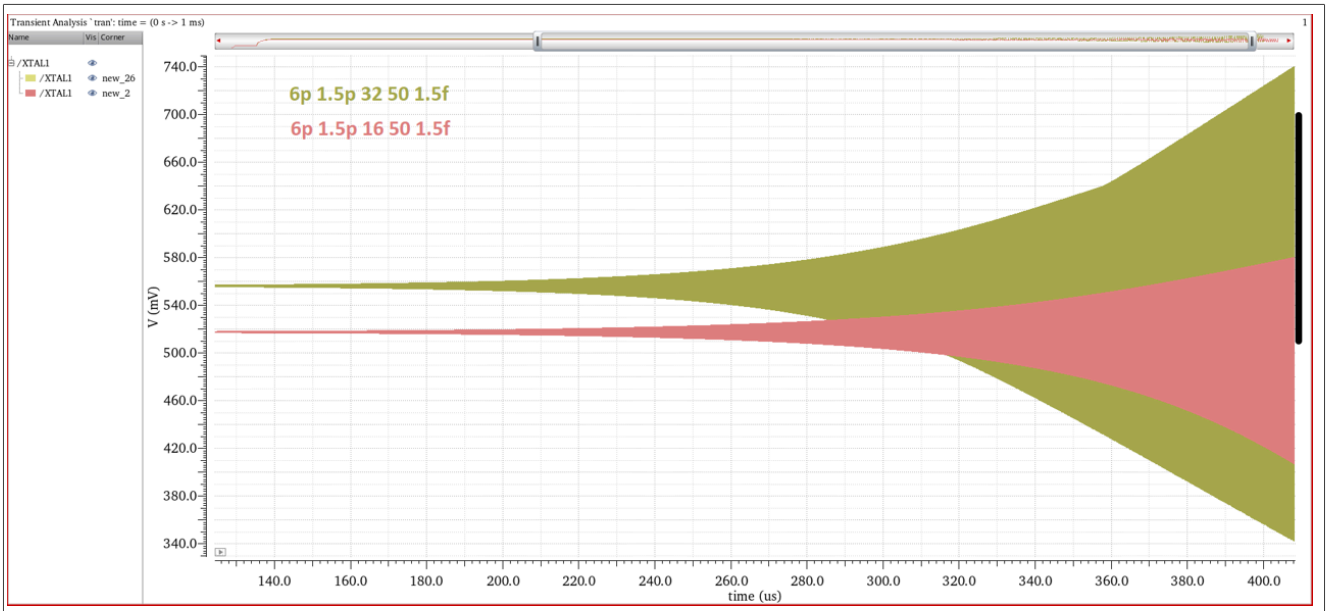

Figure 34. XTAL Start-Up, gm = 16 and 32

12 Abbreviations and acronyms

Table 7. Abbreviations and acronym

Acronym	Description
NFCC	NFC controller
ESR	Equivalent series resistance
XTAL	Crystal oscillator

13 References

[1] Data sheet – PN7160/PN7161: Near Field Communication (NFC) controller (link)
[2] Data sheet – CLRC663: High performance multi-protocol NFC frontend CLRC663 and CLRC663 plus (link)
[3] Data sheet – PN5180: High-performance multiprotocol full NFC frontend, supporting all NFC Forum modes (link)
[4] Data sheet – PN7462: NFC Cortex-M0 microcontroller (link)
[5] Data sheet – PN7642: Single-chip solution with high-performance NFC reader, customizable MCU, and security toolbox (link)
[6] Data sheet – PN5190B1: NFC frontend (link)
[7] Data sheet – PN5190B2: NFC frontend (link)
[8] Data Sheet – PN7220: NFC controller with NCI interface supporting EMV and NFC Forum applications (link)

14 Revision history

Table 8. Revision history

Document ID	Release date	Description
AN14518 v.1.0	29 November 2024	• Initial version

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