AN14350

NXP Semiconductors HDQFP Packaging

Rev. 1.0 — 1 July 2024 **Application note**

Document information

Information	Content
Keywords	S32K3, HDQFP Package, QFP, LQFP, J-Lead, Gull-wing lead
Abstract	This application note describes the HDQFP package, including the benefits of using it. It also includes the performance in terms of thermal, and electrical.

1 Introduction

This application note provides guidelines for the handling and board mounting of NXP's HDQFP packages. Included in this application note are recommendations for the design of PCB Footprint, board mounting, and soldering considerations for the HDQFP package.

2 Package background

The Quad Flat Package (QFP) is a surface-mount integrated circuit package. The QFP package has a standard form with a leaded plastic package with a flat rectangular body and square.

Leads extend from all four sides of the body. The leads or terminals are formed in a J-shape and gull-wing shape. The leads in J-shape are folded toward the package body whereas, for the latter, the leads are shaped away from the package body. Both types of external leads allow solid footing during assembly to a PCB. The standard Pb-free lead finish is matte tin.

2.1 Novel leadframe package

- Combines QFP gull-wing and PLCC J-lead in one package
- 0.65 mm pitch J-lead to J-lead and gull-wing lead to gull-wing lead
- 0.325 mm pitch J-lead to gull-wing lead

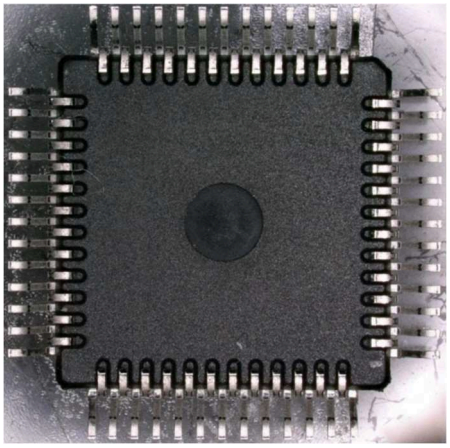
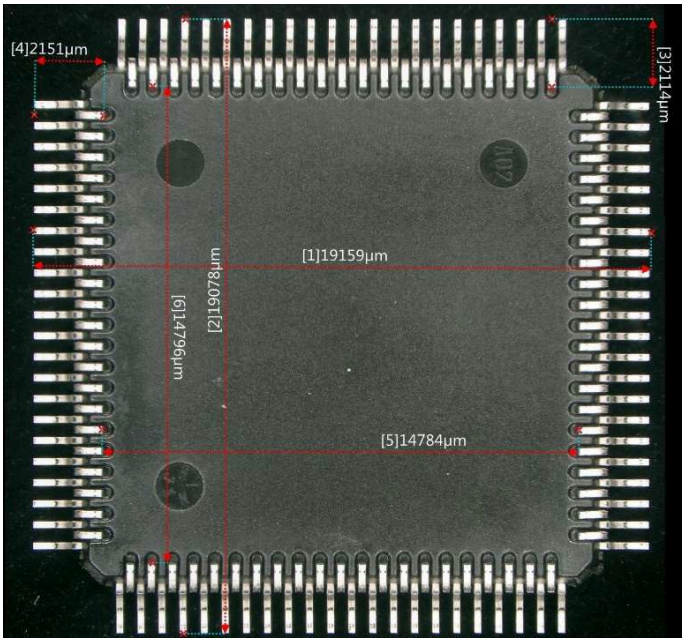
2.2 Benefits

- AEC Grade 1 proven reliability
- More IOs in smaller areas at lower cost
- Up to 65% reduction in board area (versus same lead count of LQFP)
- NXP unique technology

2.3 Productization

Next generation body and security platform for leaded products

Table 1. HDQFP package bottom view

	
100HDQFP	**172HDQFP**

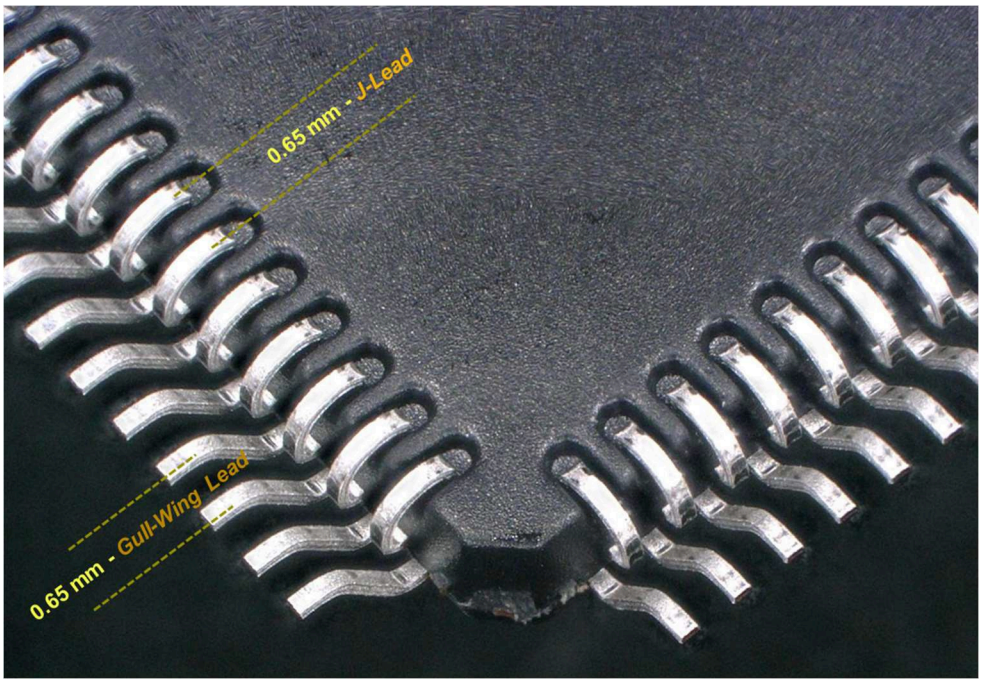
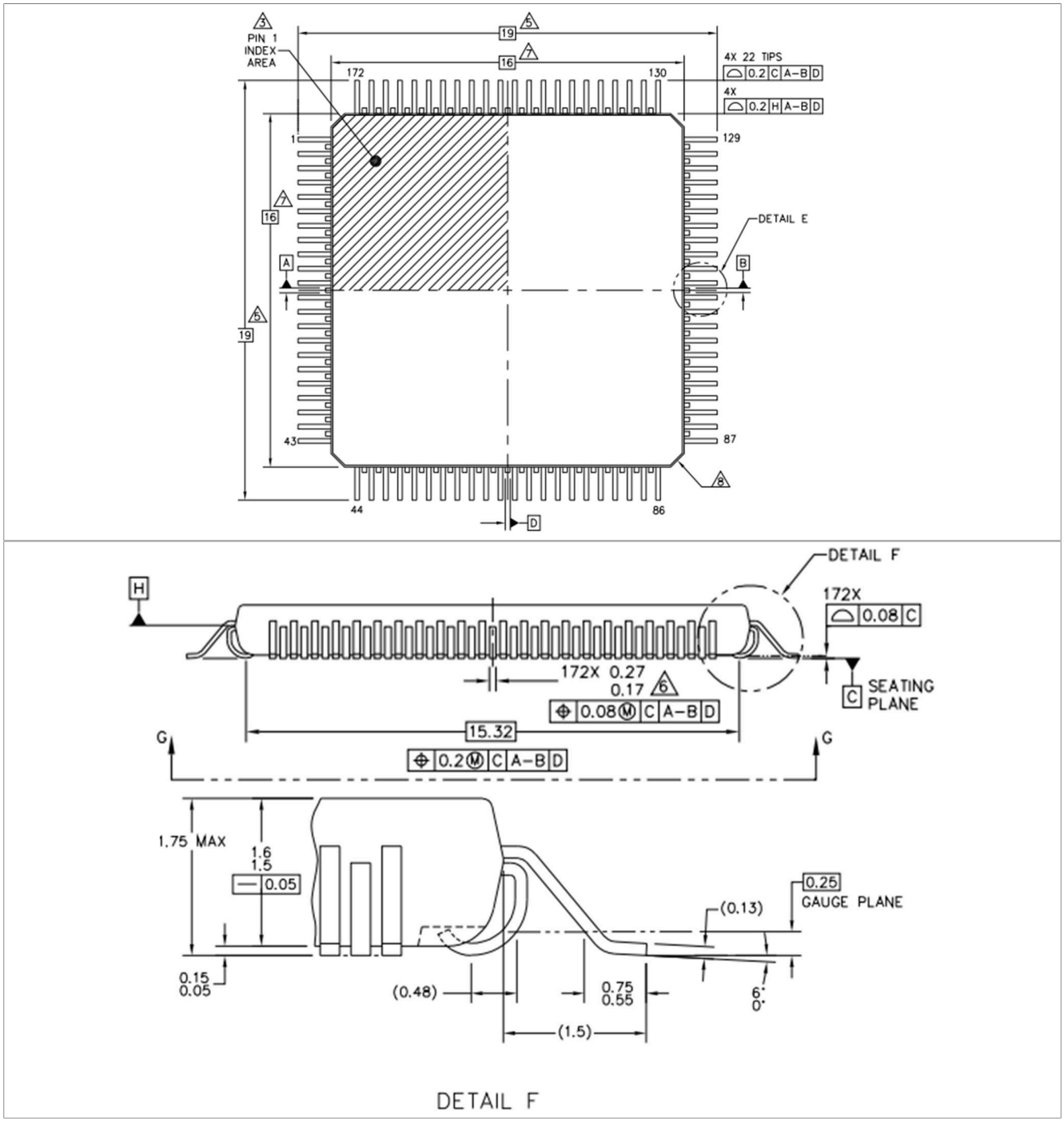


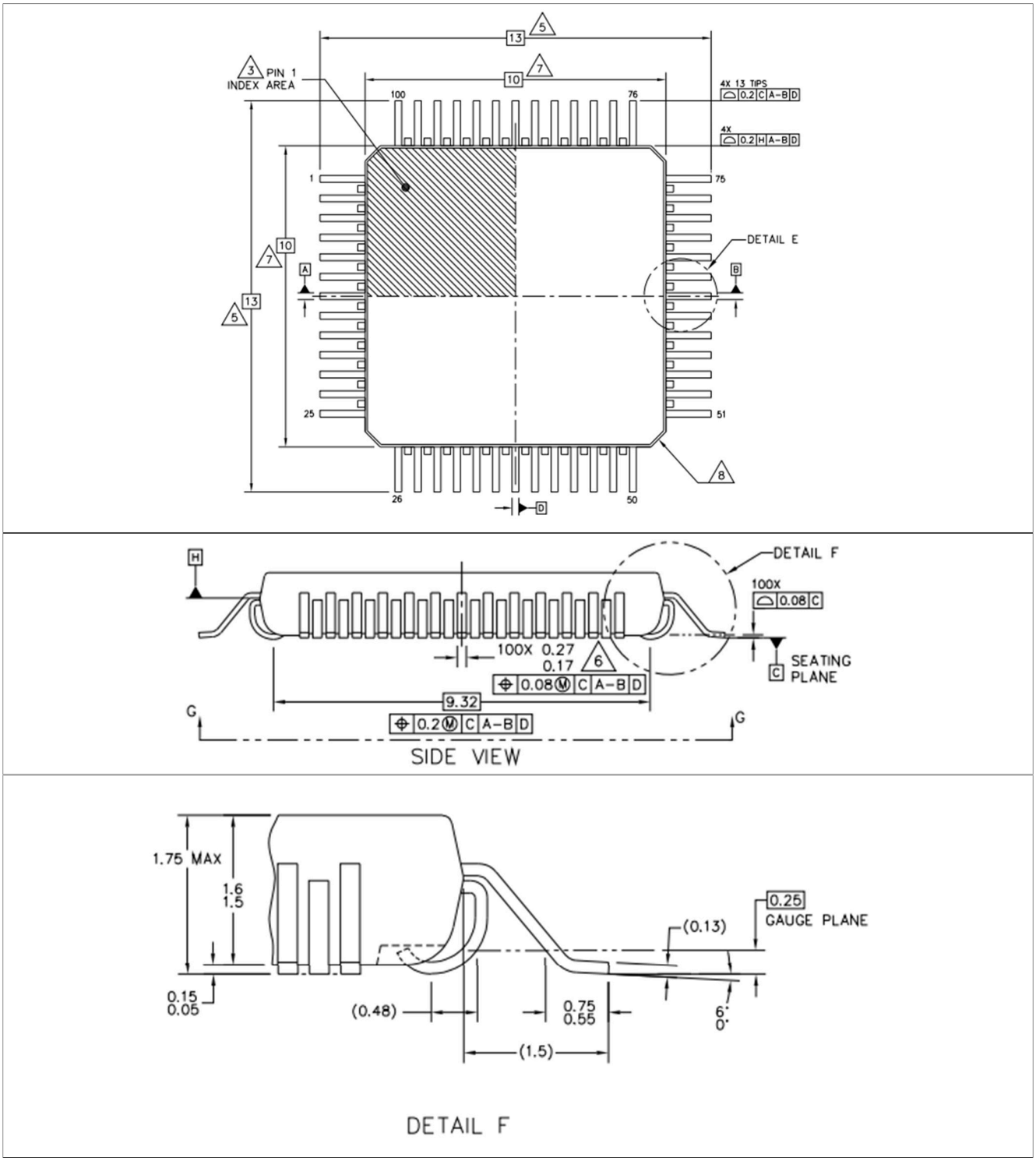
Figure 1. HDQFP package bottom - Corner view

3 HDQFP package outline drawing

3.1 172HDQFP package outline drawing



3.2 100HDQFP package outline drawing



4 PCB design guidelines and requirements for HDQFP package

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing.

- A 1.4 x 0.28 mm pad is recommended for both gull wing leads and J-leads
- 0.05 mm soldermask clearance shown around pad perimeter

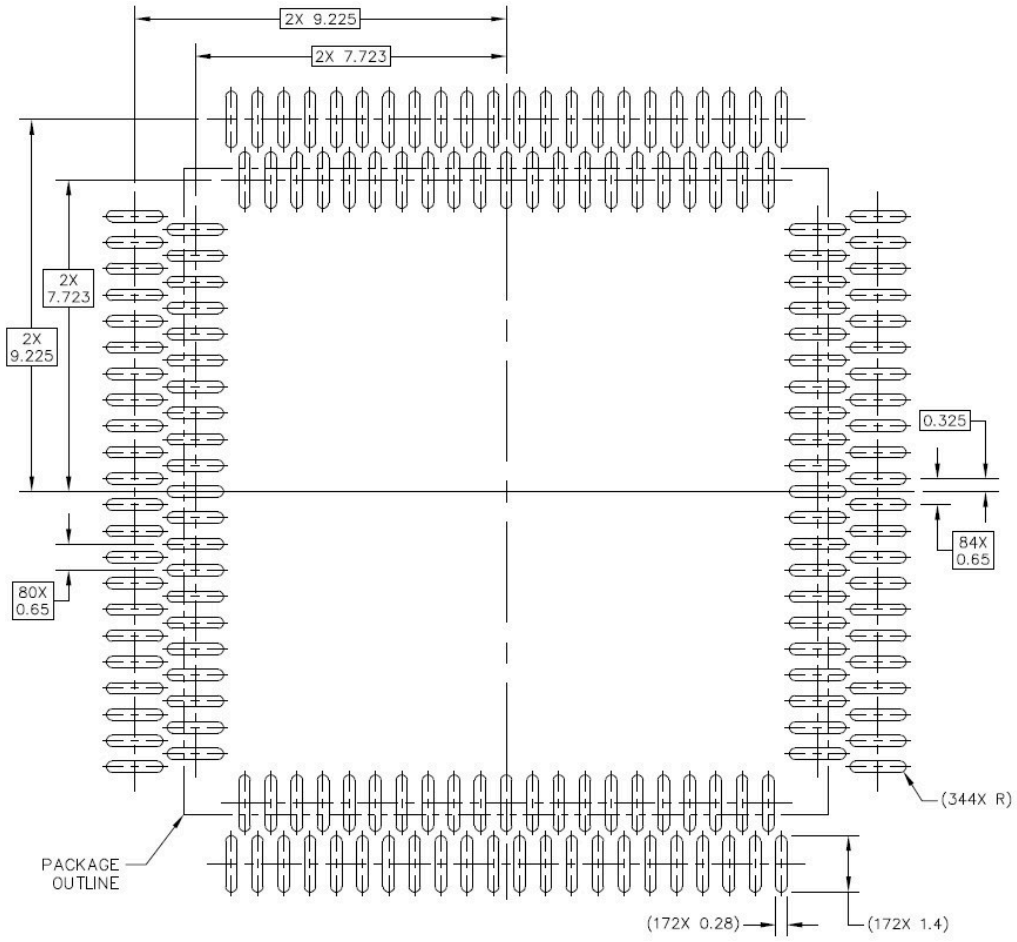


Figure 2. Copper Pads on PCB

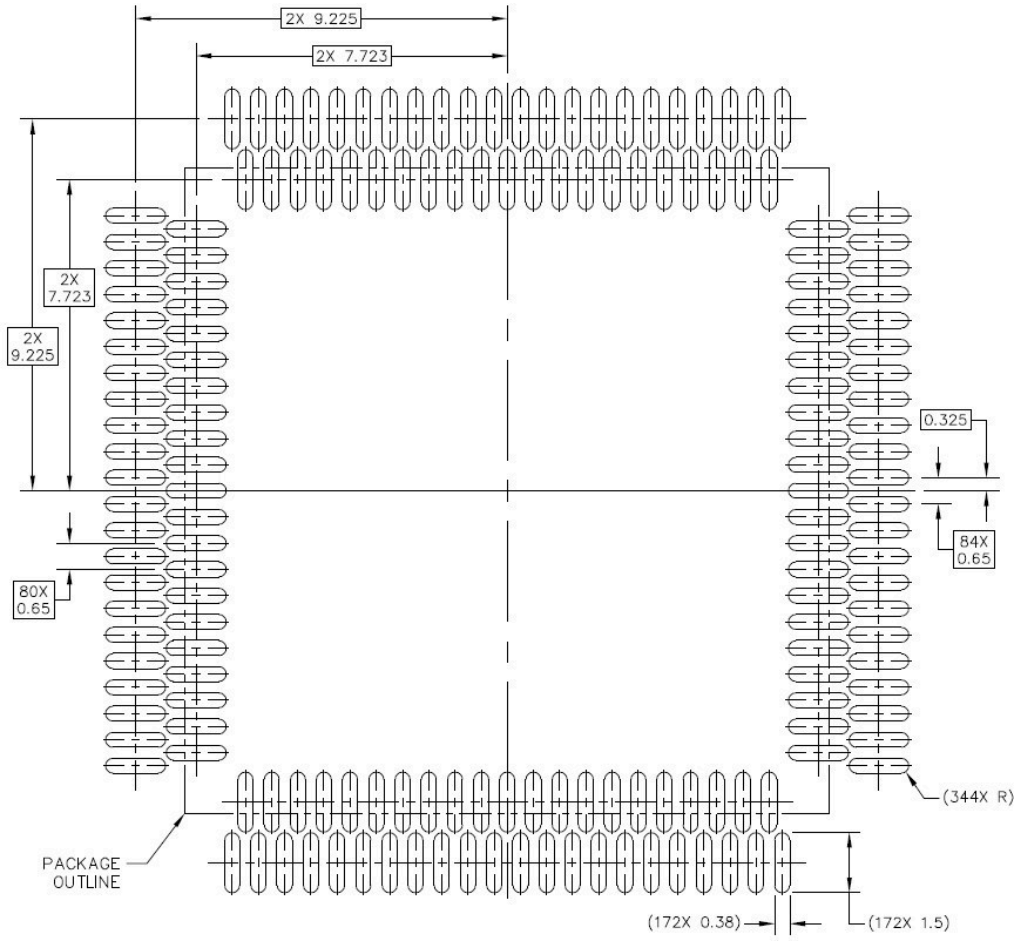


Figure 3. Soldermask on PCB

4.1 HDQFP package recommended PCB footprint design

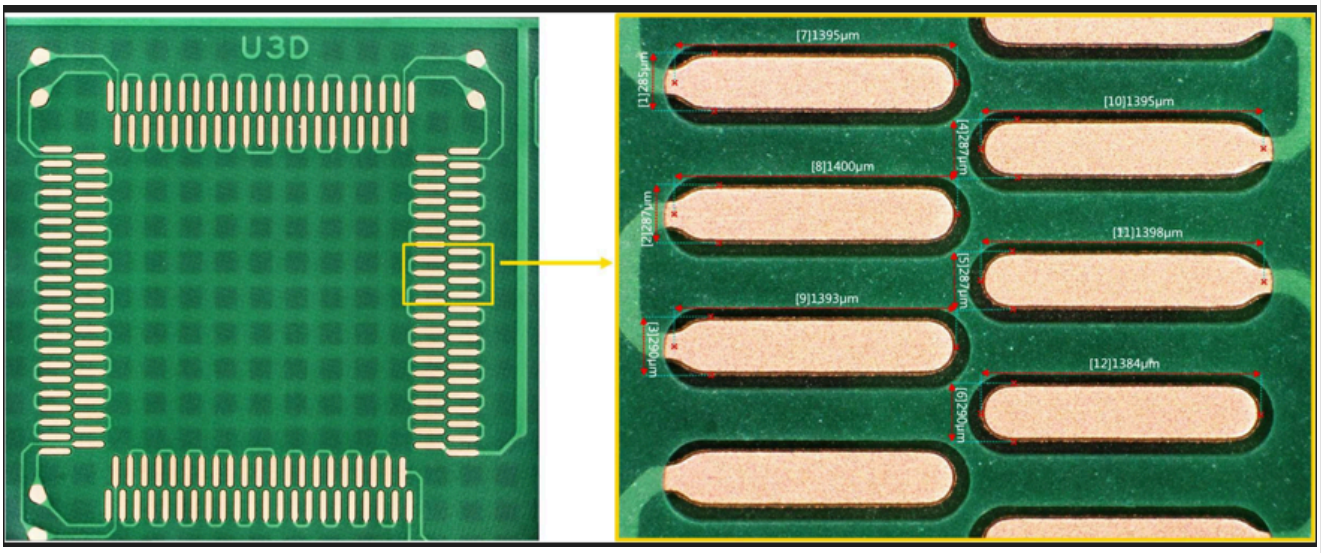


Figure 4. Example of the 172 HDQFP PCB footprint recommended

4.2 172HDQFP - Solder paste printing

- 0.125 mm thick stencil recommended
- Other thicknesses such as 0.150 mm are also shown to work

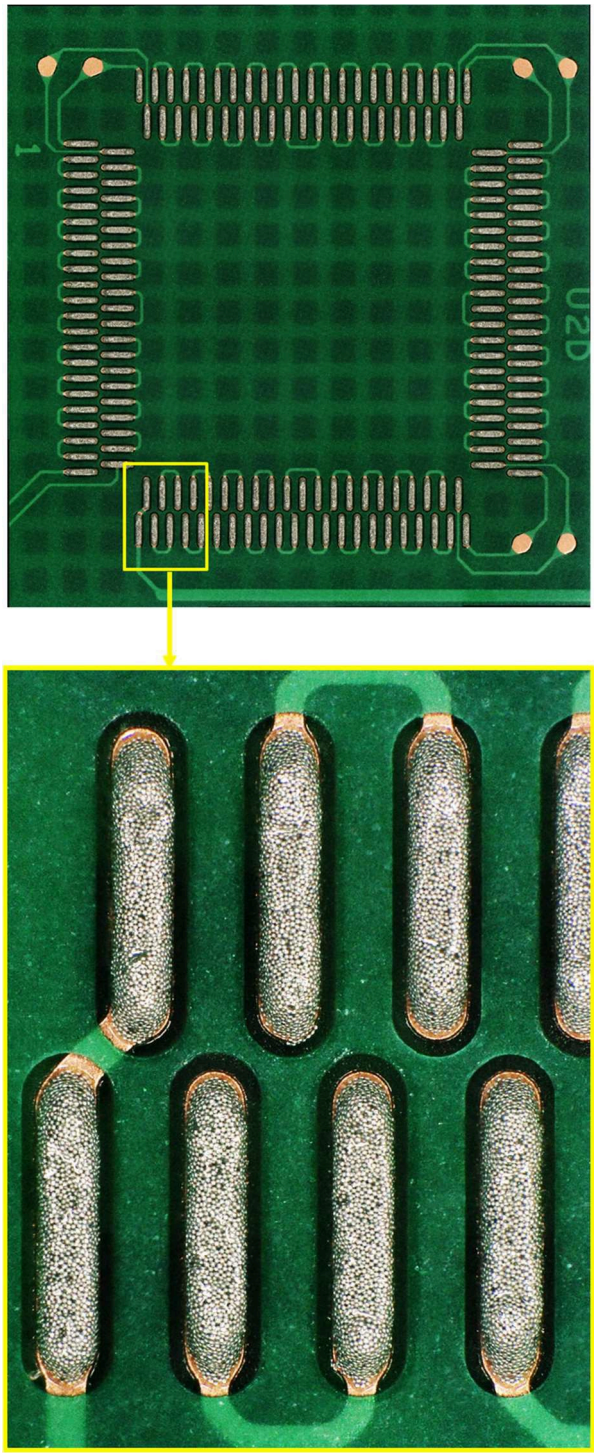


Figure 5. Example of the 172 HDQFP PCB footprint recommended with solder paste printing

4.3 HDQFP optical images reflowed onto PCB

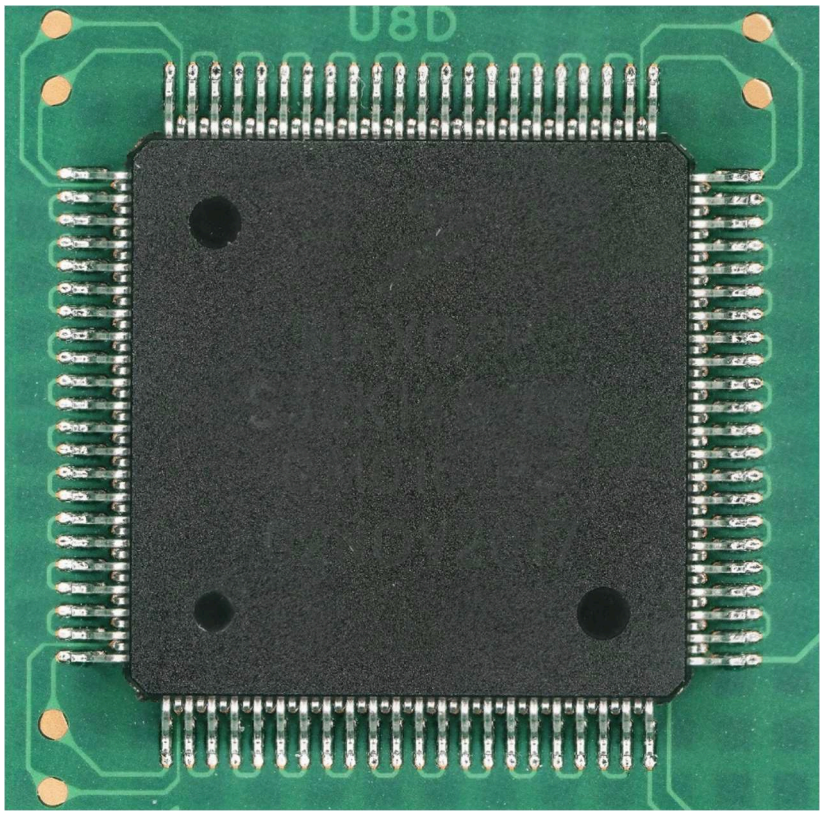


Figure 6. Package top view on PCB

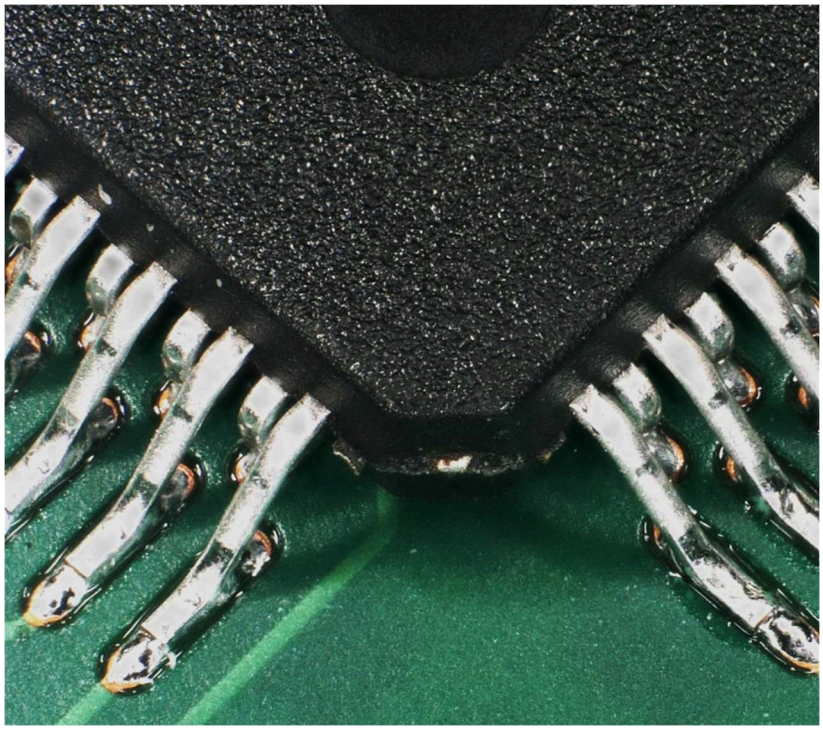


Figure 7. Package corner view on PCB

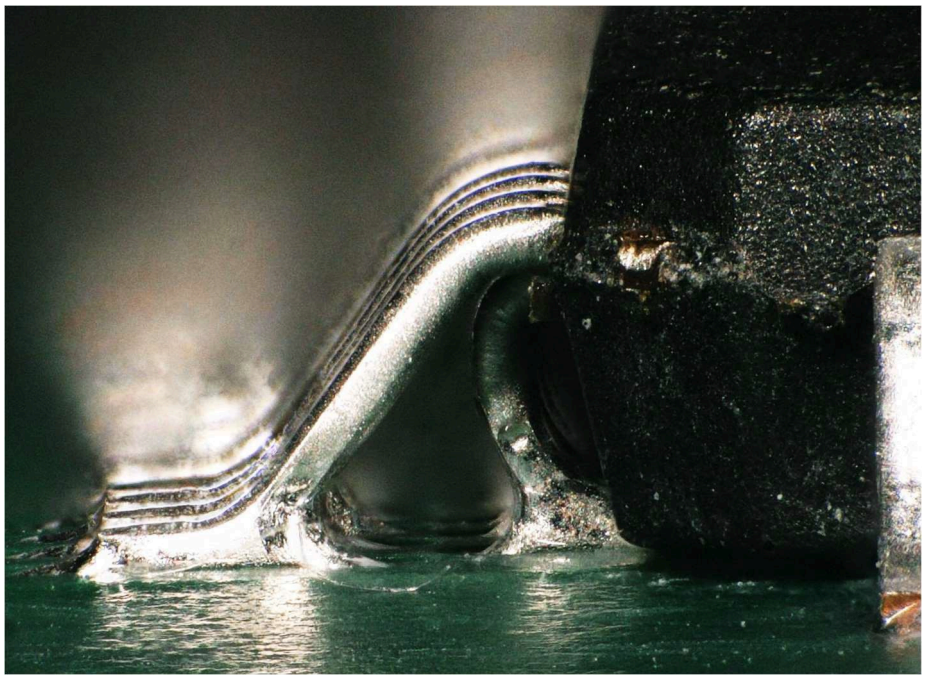


Figure 8. 172 HDQFP soldered by reflowed onto PCB

4.4 HDQFP automated optical inspection (AOI) compatibility

Solder joint inspection after SMT processes at the manufacturing site is feasible and demonstrated by several AOI systems/vendors. NXP and Viscom publish a white paper, which is available upon request. Figure 10 shows the images from an actual AOI tool on an SMT line using a 45-degree view.

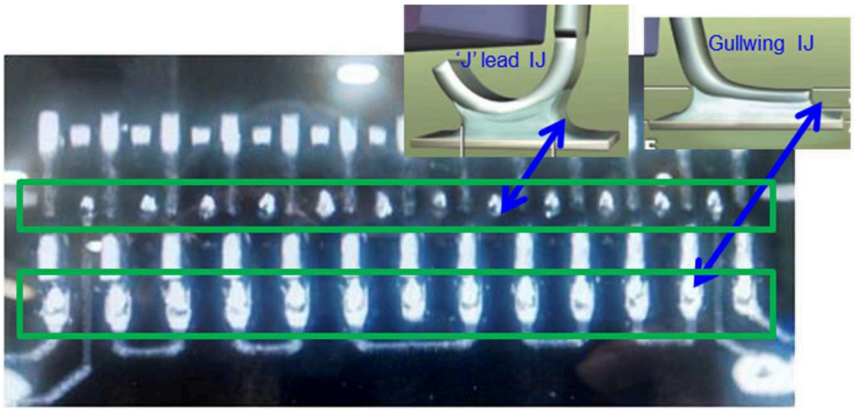


Figure 9. Stencil Thickness - 0.125 mm

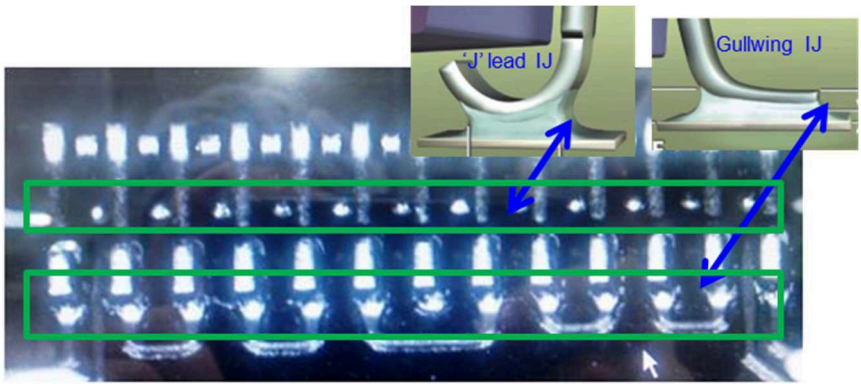


Figure 10. Stencil Thickness - 0.15 mm

5 HDQFP board level solder joint reliability

- NXP carried out extensive SMT assembly and board level reliability thermal cycling on HDQFP
- A specially designed test board was used (shown below)
- See PCB and SMT details at right
- SMT assemblies with 0.125 mm stencil thickness resulted in 100% soldering yield

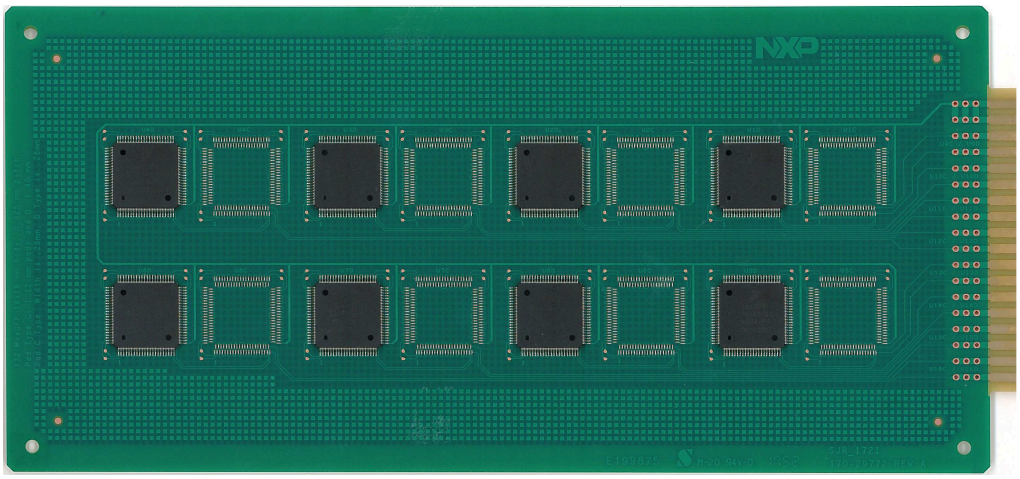


Figure 11. 172 HDQFP PCB for Board Level Reliability Testing

Table 2. HDQFP board level reliability testing PCB and SMT details

Item	Attribute	Value
Board	Length x Width (mm)	114.3 x 251.36
	Thickness (mm)	1.57
Board material	Insulating material	High Tg FR4
	Cu layers	6 layers
Pad	Pad dimensions (mm x mm)	Gull Wing and J Lead 1.40 x 0.28. 0.05 soldermask clearance.
	Surface finish	OSP (Organic Solderability Protectant)
Stencil	Thickness (mm)	0.125

Table 2. HDQFP board level reliability testing PCB and SMT details*...continued*

	Aperture dimensions	1:1 with Cu Pads
	Material	Fine grain stainless steel with nano coating
Solder Paste	Composition	SAC305
	Type	No clean, ROL0, Type IV powder
Reflow	Type	Convection Reflow in Air at 240C Peak

5.1 Typical post soldering board mounted 172 HDQFP X-Ray

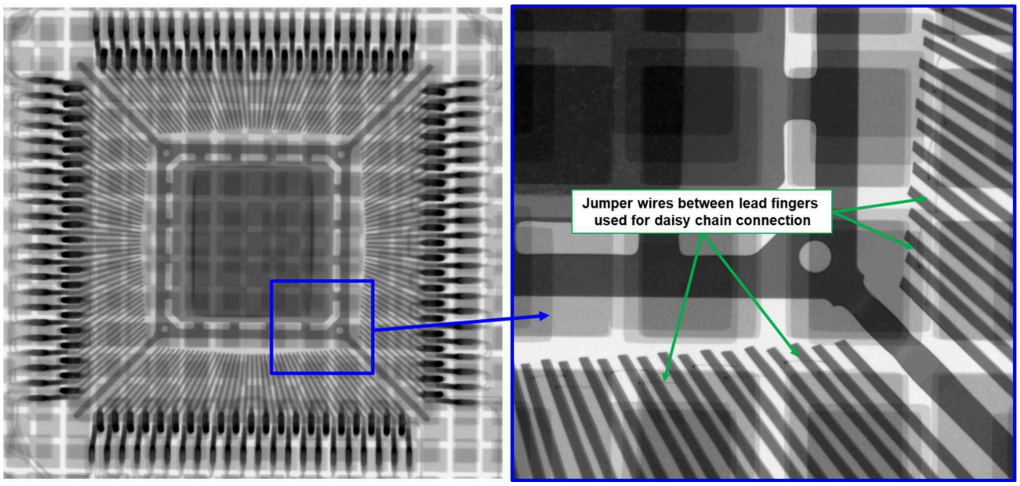


Figure 12. Top View (Through Package)

5.2 HDQFP board level reliability thermal cycling details

- Thermal cycling testing details:
  - -40°C to 125°C single chamber cycling
  - Min ramps and dwells, one-hour cycle
  - Continuous in place resistance monitoring with failure when resistance is 1000
  - Sample size of 32 parts
- Results:
  - First failure at 9191 cycles
  - Weibull characteristic life of 13,049 cycles
  - Typically cycles until >63% failure on a part basis, but due to excellent reliability, testing terminates at 12,018 cycles at 30% failure

Figure 13. Single chamber thermal cycling

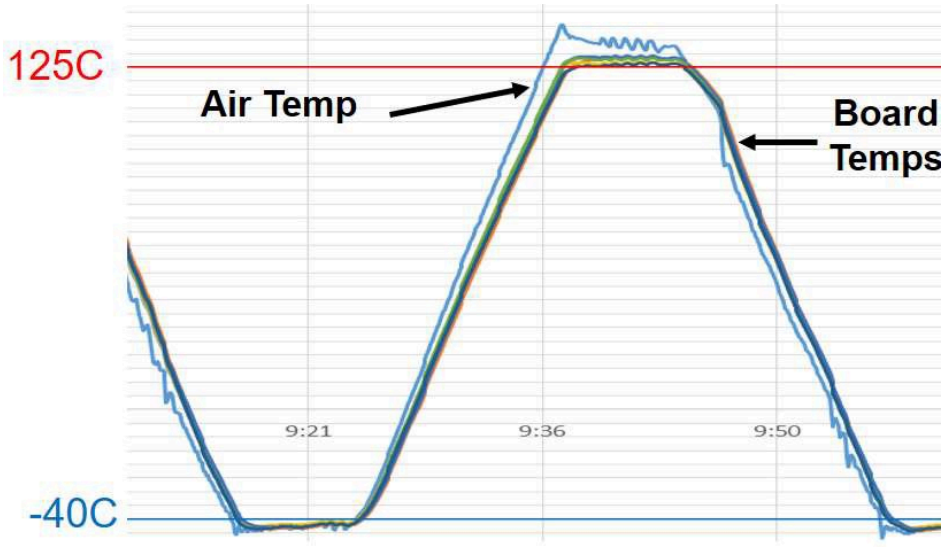


Figure 14. Thermal cycle profile

5.3 HDQFP time-zero cross-section analysis

5.4 HDQFP cross-section analysis pre-thermal cycling

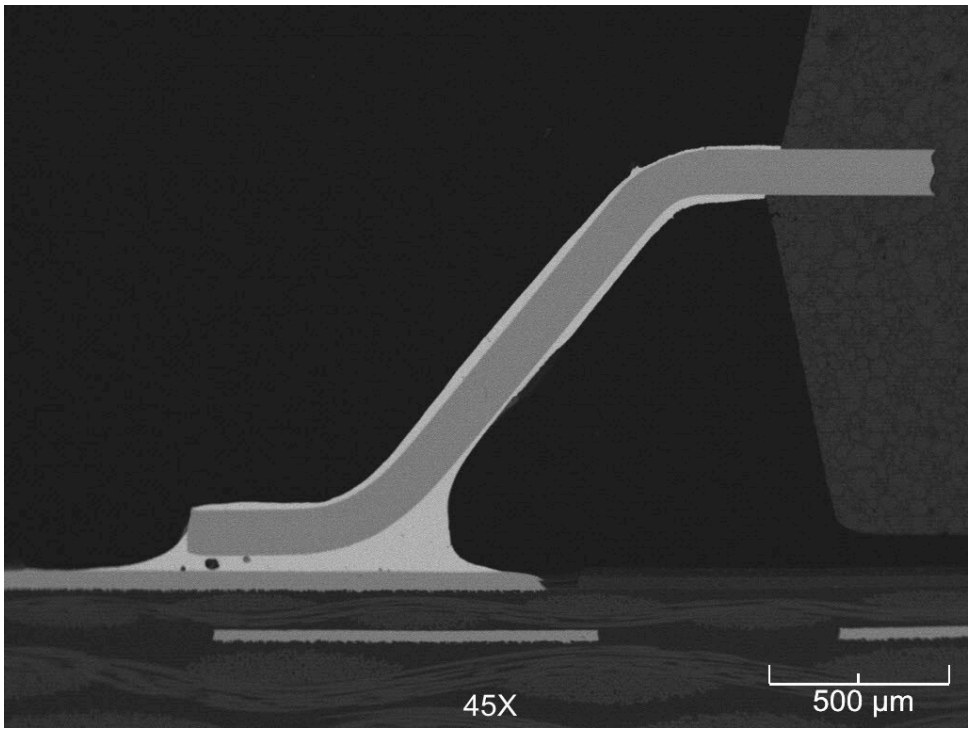


Figure 15. 172 HDQFP Gull Wing solder joint (45X)

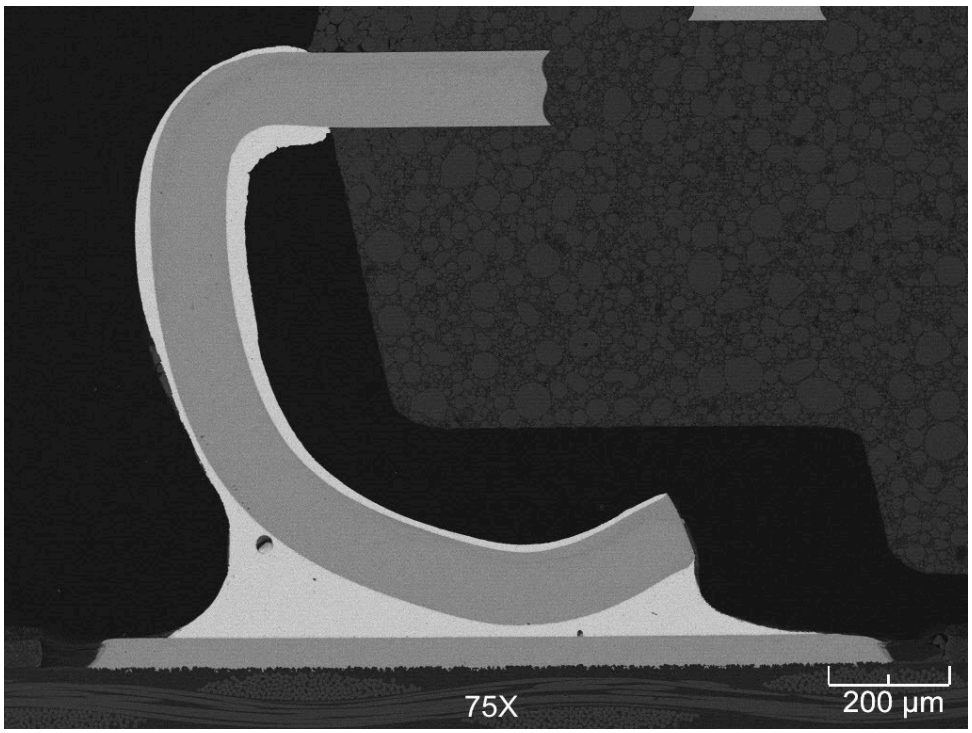


Figure 16. 172HDQFP J Lead solder joint (75X)

5.5 HDQFP cross-section analysis post-thermal cycling

- Part failed at 11212 (J Lead) and 10157 (Gull Wing) cycles.
- Pulled for cross-section at 12,018 cycles.
- Failures occurred in bulk solder.

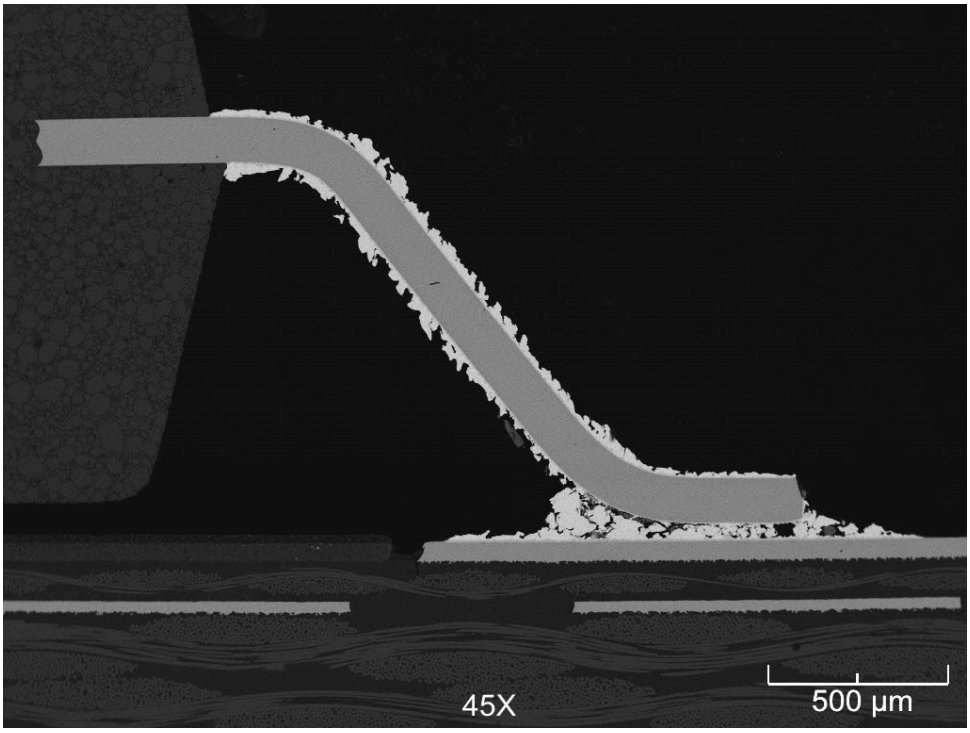


Figure 17. 172HDQFP Failed Gull Wing Joint (Lead 9)

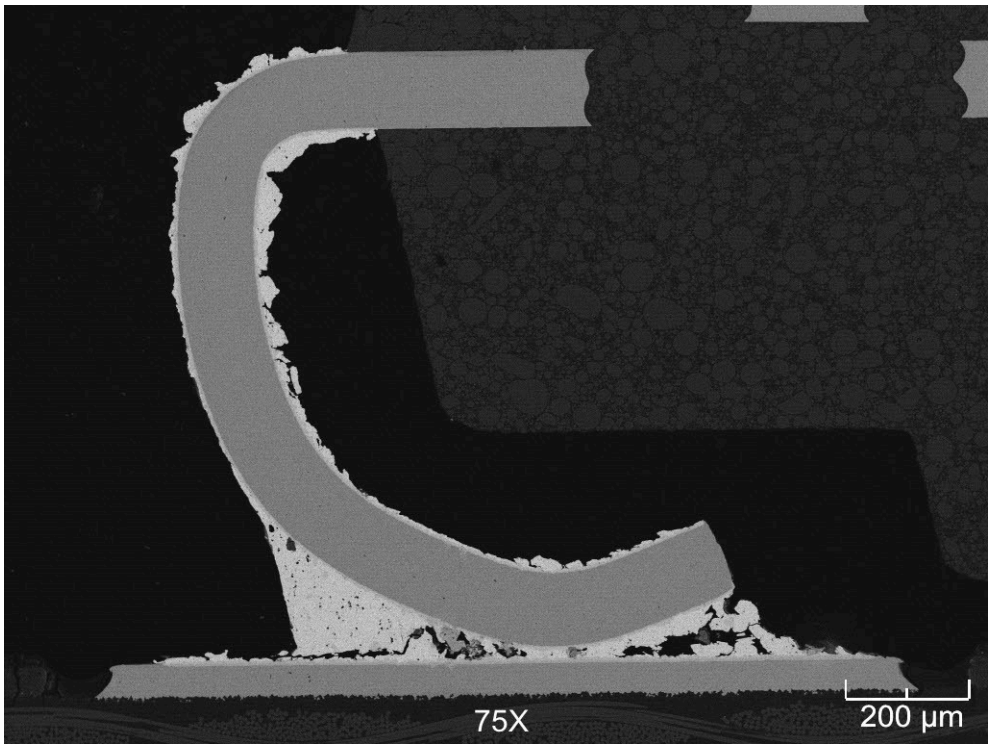


Figure 18. 172HDQFP Failed J lead Joint (Lead 124)

5.6 HDQFP board-level thermal cycling Weibull plot

- 172 HDQFP exceeded all known AEC Grade 1 BLR requirements with 9791 board level cycles to first failure
- Testing of this type typically continues until >63% failure, but due to excellent BLR result testing was terminated at 12,018 cycles at 30% failure.

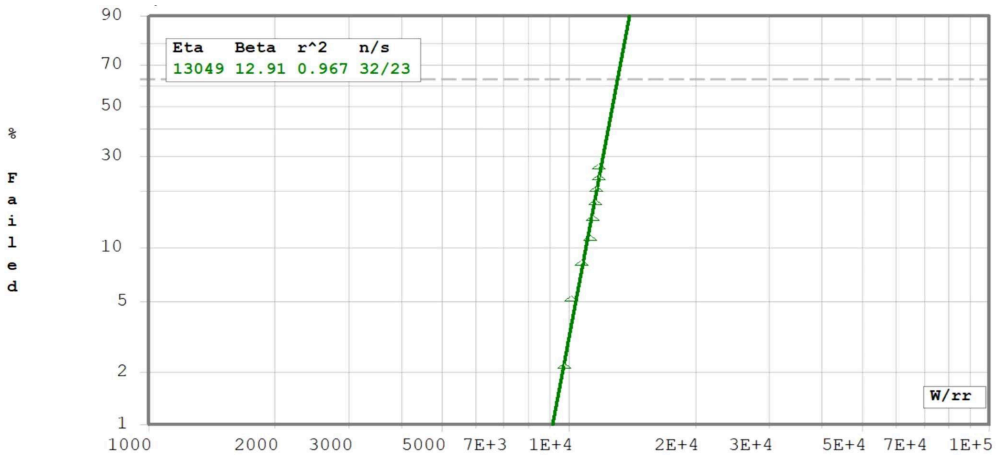


Figure 19. Thermal cycling Weibull plot

6 Thermal performance benefit

The thermal resistance values (θJA) for a 172-lead HDQFP, a 172-lead HDQFP_EP, a 176-lead QFP, and a 176-lead QFP_EP are calculated and compared in Table 2 according to JEDEC specification JESD51-7. This

is done using two layers of signal and two layers of power (2s2p) thermal test boards at three different die sizes: 45 mm^2, 50 mm^2, and 55 mm^2, respectively. Three die size (45 mm^2, 50 mm^2, and 55 mm^2) were used for all four package types in modeling. A larger die size resulting in a relatively smaller θJA value at the same body size is observed expectedly because larger die size can provide a larger area to dissipate heat. Also, as expected, a package with an exposed pad has better thermal performance than one without, because the additional heat-transfer area is considerable. The surprising thermal performance result is that the 55% smaller HDQFP package performs better than the larger QFP package at similar pin counts and same die size (for example, 172 HDQFP vs 176 LQFP). At the same die sizes, the improvement is about 16% for HDQFP and about 10% for HDQFP_EP as comparing to LQFP and LQFP_EP. The reason is likely the higher lead count density (that is, leads per area) of HDQFP compared to QFP. The real functional device tests later validate this simulation result. These results clearly indicate that HDQFP can fully replace QFP from a thermal perspective and even offer an advantage.

Table 3. Thermal resistance value (θJA) comparison between HDQFP and QFP at similar pin counts

	θJA (°C/W)		
Die size (mm^2)	**45**	**50**	**55**
172 HDQFP (16x16)	27.14	26.54	25.94
176 LQFP (24x24)	32.67	31.00	29.33
172 HDQFP_EP (16x16)	20.40	20.00	19.60
176 LQFP_EP (24x24)	22.67	22.33	22.00

7 Electrical performance benefit

The 100-lead HDQFP package (body size 10x10 mm) was selected for an electrical performance study, and its characteristics were compared with those of a 100-lead QFP (body size 14x14 mm) using the same die design. Therefore, the same bonding layout can be used for both 100 HDQFP and 100 LQFP because they have the same lead counts. The only difference is bonding wire length and geometry variation in lead frame designs, for example, lead length . Like the thermal performance study discussed above, this electrical performance study was also conducted by simulation. The die size used in the simulation was 4.25 x 3.91 mm. Figure 20 shows the visual comparison of the bonding diagram (bonding layout) between 100 HDQFP and 100 LQFP for this study. The wire lengths ranged from 1.71 mm to 2.36 mm for the 100 lead HDQFP part, and from 1.84 mm to 2.35 mm for the 100 lead QFP part. 20 um wire pure Cu (99.99%) wire with dc resistivity of 1.7 micro-ohm-cm is assumed in this simulation. The wire length is comparable in these two models to avoid its impact on electrical performance.

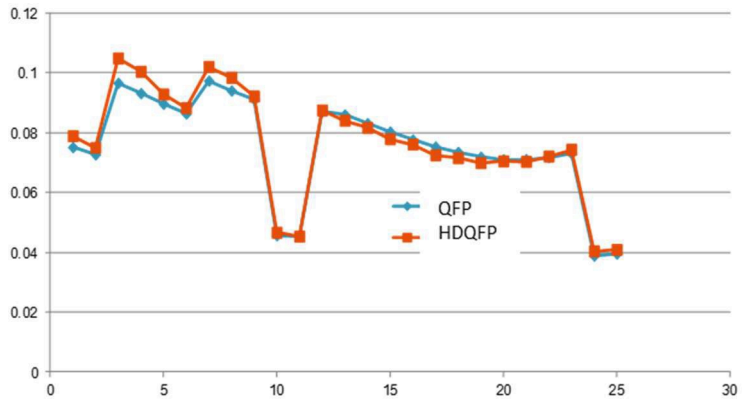


Figure 20. DC resistance comparison (unit in ohm) between 100 HDQFP and 100 LQFP is virtually identical and shows no difference

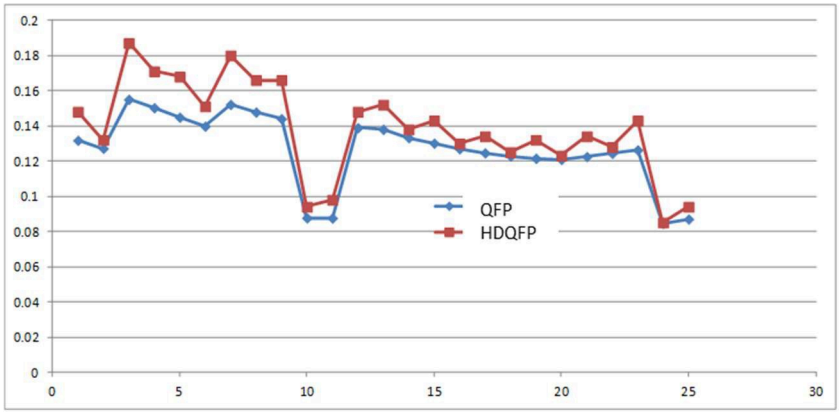


Figure 21. AC resistance (unit in ohm) comparison between 100 HDQFP and 100 LQFP is almost identical and shows no difference

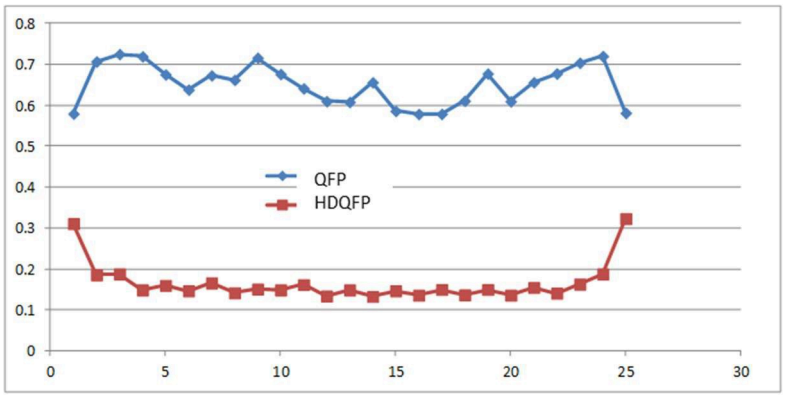


Figure 22. Self-capacitance values (unit in pF) at 100 MHz for both 100 HDQFP and 100 LQFP. HDQFP has a lower capacitance value indicating a better electrical performance than QFP.

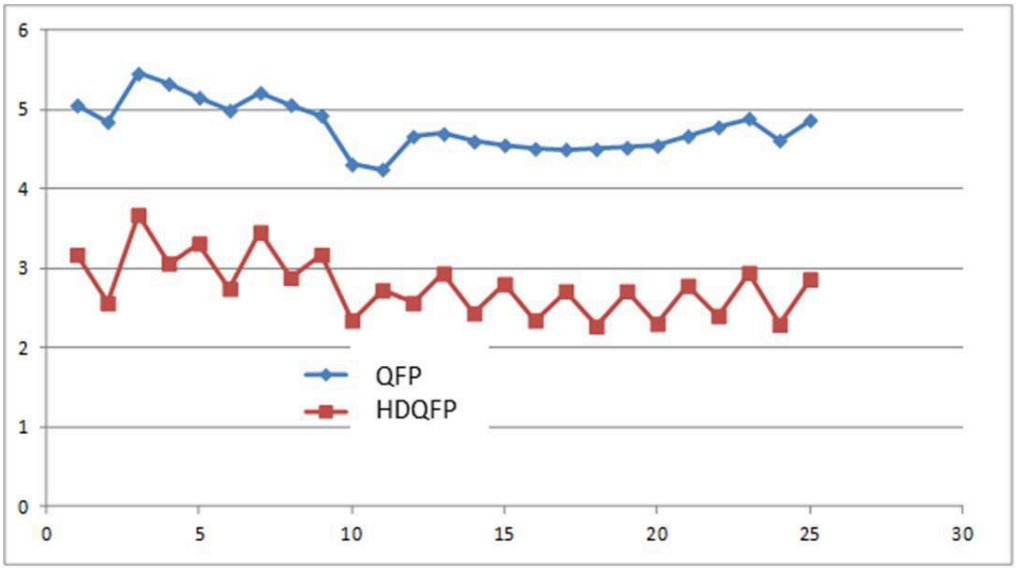


Figure 23. Self-inductance values (unit in nH) at 100 MHz for both 100 HDQFP and 100 LQFP. HDQFP has a lower inductance value indicating a better electrical performance than QFP.

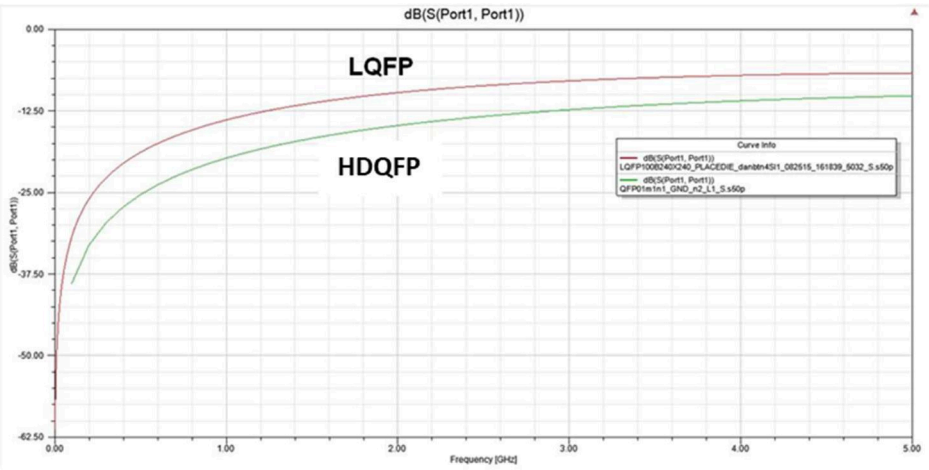


Figure 24. Return loss of signal nets for both 100 LQFP and HDQFP. HDQFP clearly performs better than LQFP.

8 Publications

1. “HDQFP_EP (High density QFP_EP): A thermally enhanced HDQFP platform” by Chu-Chung Stephen Lee, TuAnh Tran, Andrew Mawer, PL Mei, XS Pang and JZ Yao, 19th International conference & Exhibition on Device Packaging, Fountain Hills, AZ, Mar 13 to 16, 2023.
2. “A high density QFP with hybrid lead” by Milan Ma, Denis Bai, XS Pang, Yongchao Luo, JZ Yao and Chu-Chung Stephen Lee, 24th International Conference on Electronic Packaging Technology (ICEPT), 2023.
3. “Assembly and Reliability of a Novel High Density Dual Row MaxQFP”, Andrew Mawer, Mollie Benson, XS Pang, Chu- Chung Stephen Lee, JZ Yao and Alvin Youngblood, Surface Mount Technology Association (SMTA) 2022 Conference, Minneapolis, MN, USA, Oct 31 – Nov 3rd.
4. “MaxQFP – A high density QFP”, Presentation by Chu-Chung Stephen Lee, at CTEA (Central Texas Expo & Tech Forum), SMTA, Sept 13th, 2022, Austin Texas.
5. “MaxQFP: A high Density QFP”, Chu-Chung Stephen Lee, TuAnh-Tran, Andrew Mawer, Glenn Daves, XS Pang and JZ Yao, 2022 IEEE 72nd Electronic Components and Technology Conference (ECTC), pp.2174 – 2183, May 31 to Jun 2022, San Diego, CA, USA.
6. “A new high density QFP”, Chu-Chung Stephen Lee, et al, https://chipscalereview.com/wp- content/uploads/2021/11/ChipScale_Nov-Dec_2021-digital.pdf, pp. 18 - 26.
7. "MaxQFP: NXP new package platform," , Chu-Chung Lee et al, 2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC), 2021, pp. 195-200, doi: 10.1109/EPTC53413.2021.9663934.
8. “MaQFP: NXP’s new package solution for automotive application by Chu-Chung Stephen Lee et al, International symposium on Microelectronics, San Diego, CA USA, Volume 2021 Issue 1, Oct 2021: 000015 – 000020.
9. “MaxQFP: NXP new package platform for automotive application” by Chu-Chung Stephen Lee, et al, 17th International conference & Exhibition on Device Packaging, Virtual Conference, Apr 2020.

9 Summary

- HDQFP is a cost-effective, small footprint, high reliability package that exceeds AEC Grade 1 requirements.
- Excellent SMT yield and board level thermal cycling reliability demonstrated.
- The package has been extensively tested, modeled, and characterized.
- Automated Optical Inspection (AOI) of J-leads demonstrated using an angled camera.
- Planned usage in various NXP products.

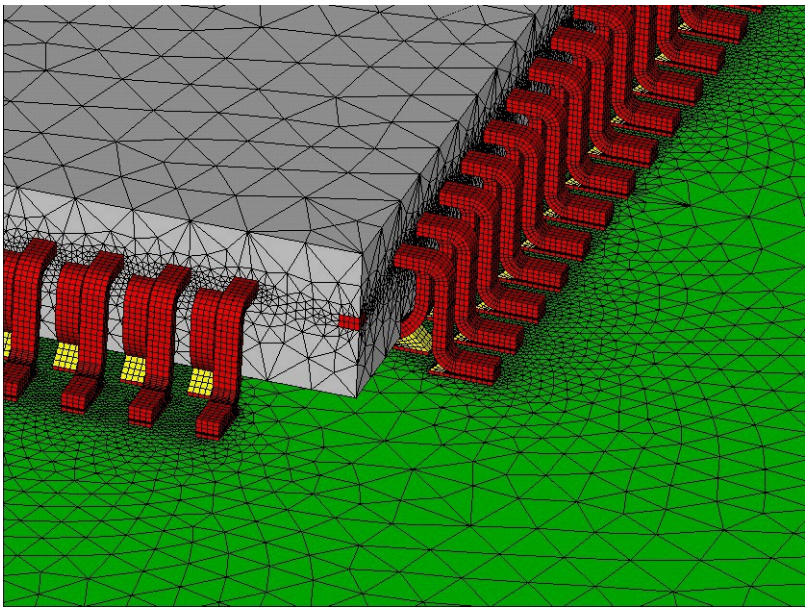


Figure 25. Finite Element Model of HDQFP on PCB

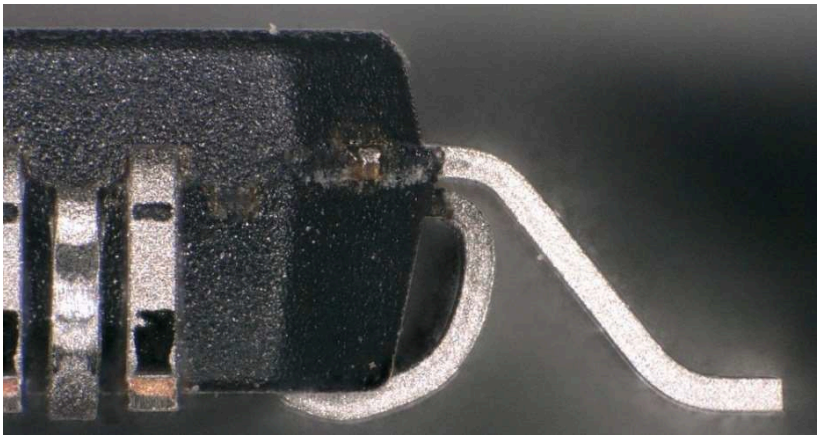


Figure 26. Side View of HDQFP

Revision history

Table 4. Revision history

Document ID	Release Date	Description
AN14350 v.1.0	1 July 2024	Initial release

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