AN14317

Low power implementation on MCXN236

Rev. 1.0 — 14 May 2024 **Application note**

Document information

Information	Content
Keywords	AN14317, MCXN23x, Low power, Power consumption, Wake-up time
Abstract	This application note introduces the power domains, power modes, low power entry, wake-up, and low power and wake-up optimization of MCXN23x. It also provides a demo to reproduce the typical power consumption and wake-up time data in the data sheet.

1 Introduction

The MCX N23x series microcontrollers combine the Arm Cortex-M33 TrustZone core with multiple high-speed connectivity options running at 150 MHz, providing advantages in security, industrial strength, and power-efficient operations.

The power-efficient operating modes are as follows:

- 50 µA/MHz in Active mode
- 124 µA in Deep Sleep mode
- 2.39 µA in Power Down mode
- 1.5 µA in Deep Power Down mode

This application note describes the following contents of MCXN23x:

- Power domains and power supplies
- Power modes
- Low power entry and configurations
- Wake-up source and wake-up time
- Low power and wake-up optimization
- Demo that reproduces the power consumption and wake-up time specified in the MCX N23x data sheet

2 Power domains and power supplies

This section describes the overall power domains, voltage supplies, and different power supply configurations.

2.1 Power domains and voltage supplies

The device contains the following domains: CORE_MAIN, CORE_WAKE, CORE_SRAM, SYSTEM, VBAT, USB, VDD, IO_2, IO_3, IO_4, and ANALOG. Figure 1 shows the overall power domains and voltage supplies. This section mainly introduces the CORE, SYSTEM, and VBAT domains. For specific modules contained in each domain, refer to the “Power domain assignments for modules” table in the *MCX N23x Reference Manual*.

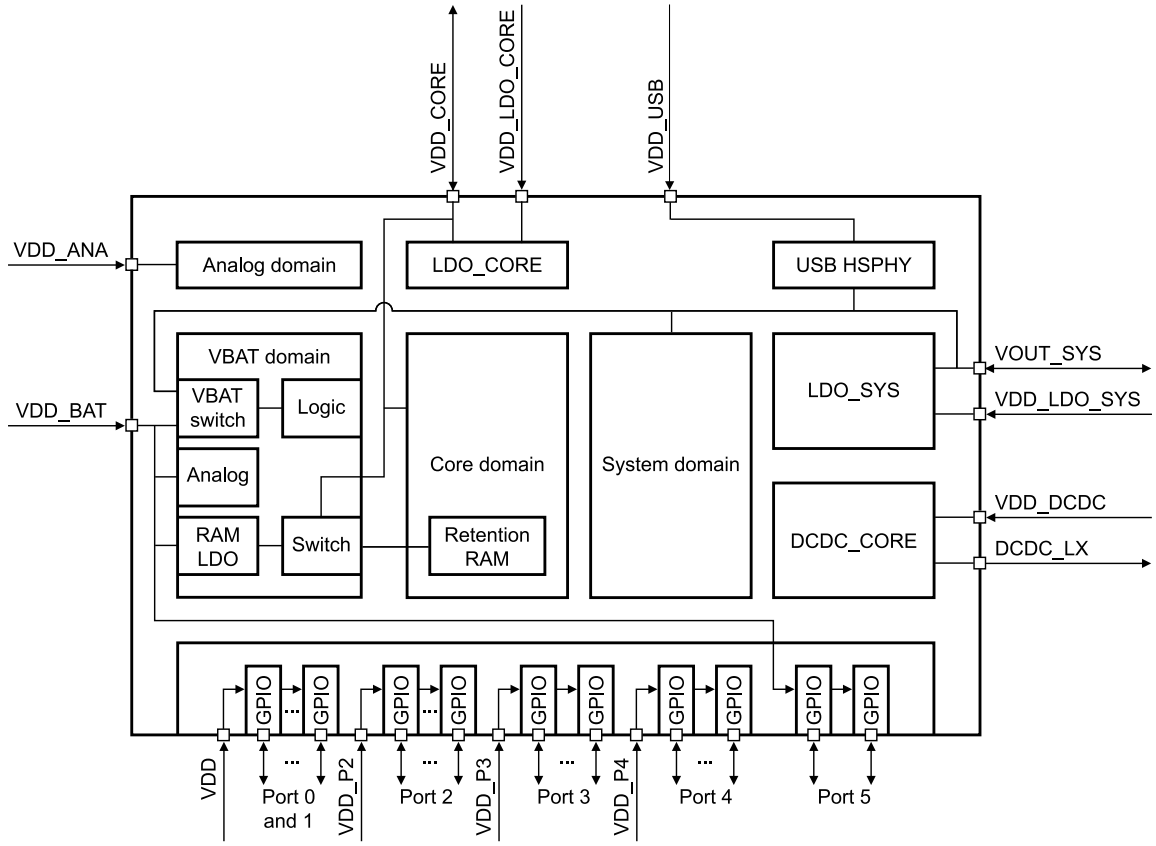

Figure 1. Power domains and voltage supplies

Figure 2 shows the CORE domain supply voltage for most digital modules, and is divided into three subdomains, namely CORE_MAIN domain, CORE_SRAM domain, and CORE_WAKE domain. CORE_MAIN domain mainly includes cores, peripherals and masters (DMAs, SmartDMA, and so on). The CORE_SRAM domain includes all RAM blocks. The CORE_WAKE domain includes wake-up peripherals (Windowed Watchdog Timer, CTIMER0, and so on).

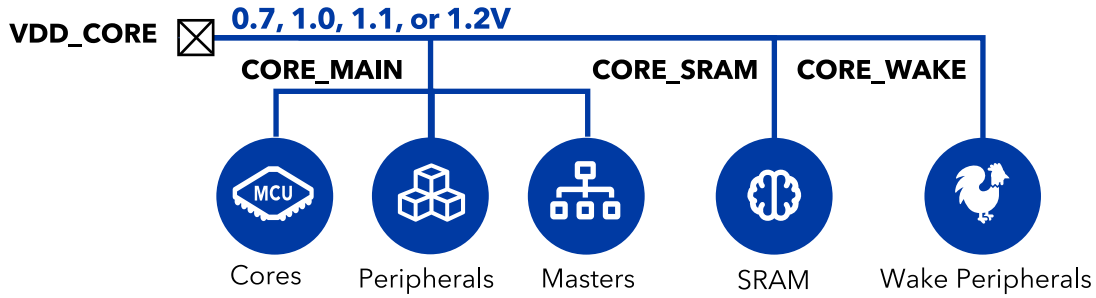

Figure 2. Core domain and voltage supply

In active mode, VDD_CORE can be configured to 1.2 V (Over Drive mode), 1.1 V (Standard Drive mode), and 1.0 V (Mid Drive mode). In Power Down mode, VDD_CORE can be configured to 0.7 V. Table 1 describes the maximum frequency that CPU and AHB can achieve at different voltage levels.

Table 1. Voltage level and frequency

VDD_CORE	f_{CPU}, f_{AHB} ≤
1.2 V	150 MHz

Table 1. Voltage level and frequency*...continued*

VDD_CORE	f_{CPU}, f_{AHB} ≤
1.1 V	100 MHz
1.0 V	50 MHz
0.7 V	Gated off

Figure 3 shows that the SYSTEM domain is used for power management, including high voltage detect / low voltage detect (HVD / LVD) and system power control (SPC). The normal mode supply voltage of this power domain is 1.8 V. It supports Fuse programming at 2.5 V.

Note: *The maximum total accumulated time for elevated VDD_SYS (VDD_SYS > 1.98 V) is 20 seconds over the lifetime of the device.*

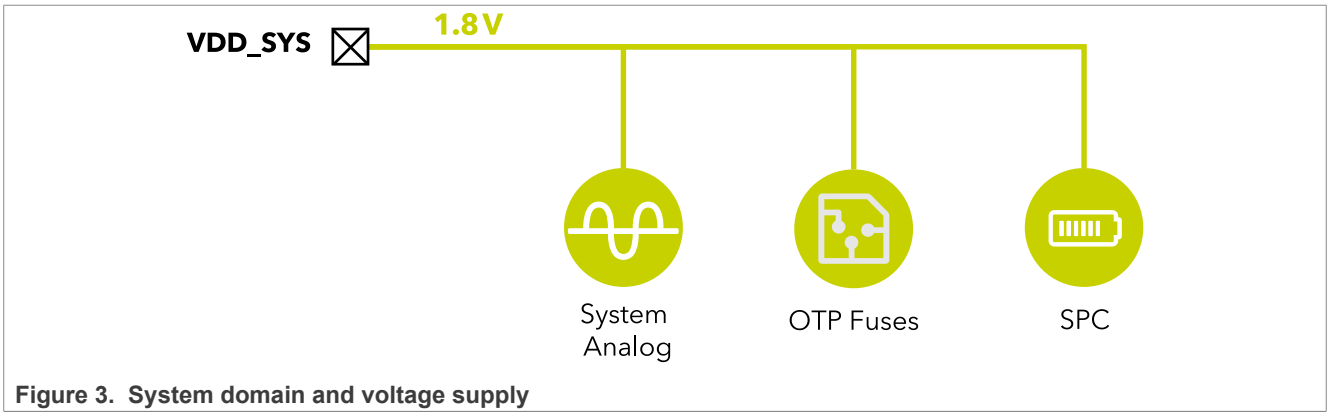

Figure 3. System domain and voltage supply

Figure 4 shows the VBAT domain supply to always-ON modules, including OSC_32K, FRO_16K, back up retention RAMA regulator, RTC, and PORT5. The VDD_BAT ranges from 1.71 V - 3.6 V.

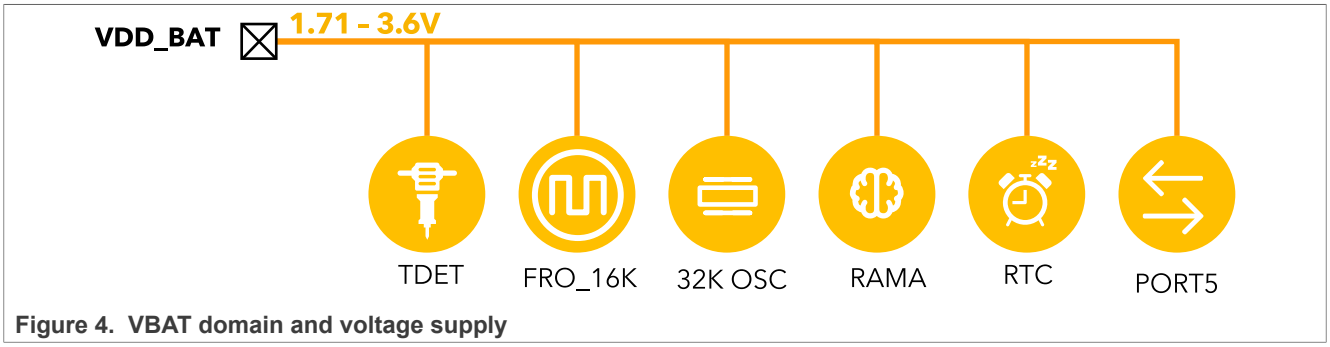

Figure 4. VBAT domain and voltage supply

In addition to the power domains already described above, Figure 5 shows the remaining power domains of this device, along with the corresponding modules and voltage supply ranges.

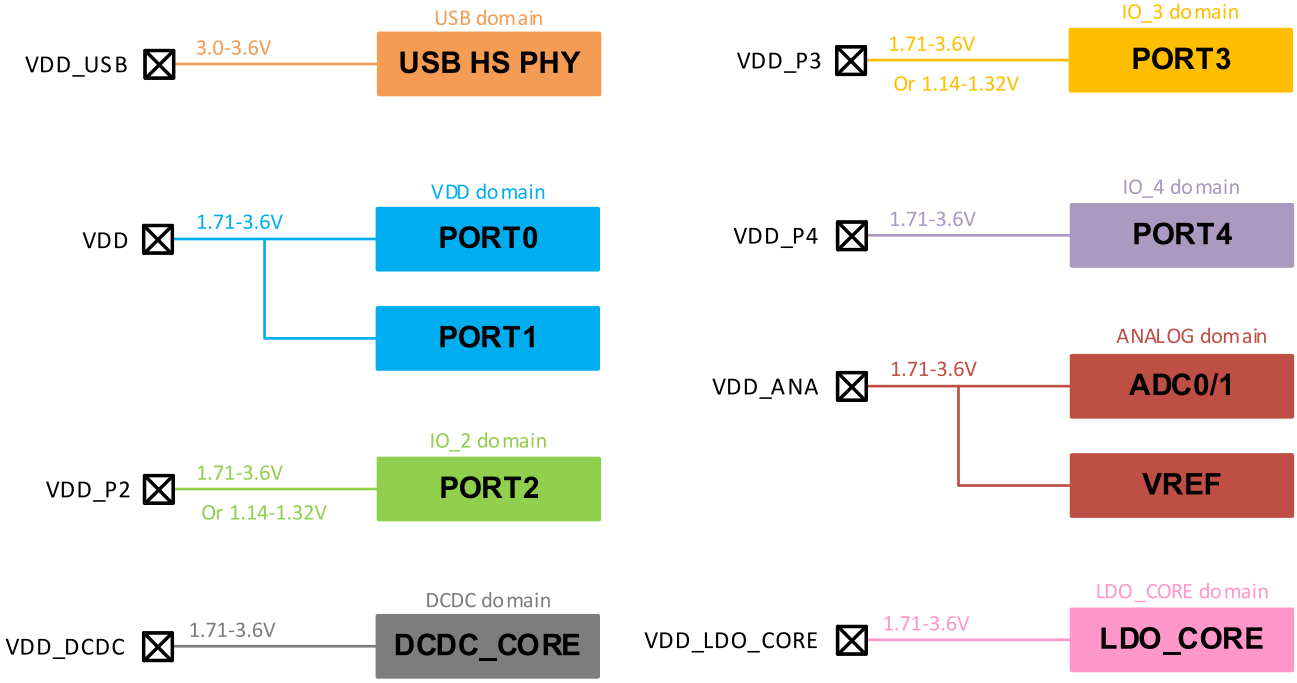

Figure 5. Power domains and voltage supplies

2.2 Power supply configurations

Figure 6 shows that the on-chip DCDC converter or LDO regulator is used to regulate the input voltage to the appropriate VDD_CORE to supply the CORE domain.

When using DCDC_CORE to generate VDD_CORE, it has better efficiency than LDO_CORE. For the device package, which has the VDD_LDO_CORE pin, should short this VDD_LDO_CORE pin to the VDD_CORE pin, and disable LDO_CORE by configuring the CNTRL[CORELDO_EN] bit field.

Another configuration is to use LDO_CORE to generate VDD_CORE to save cost and eliminate the passive components for the DCDC_CORE. For packages where VDD_DCDC has an independent pin, you can connect VDD_DCDC and DCDC_LX to GND with a 10 kΩ resistor to disable DCDC. For packages where VDD_DCDC and VDD_LDO_SYS share a package pin, to disable DCDC, DCDC_LX must be floating. Regardless of the package, you must disable DCDC_CORE by configuring the CNTRL[DCDC_EN] bit field.

Note: *In Power Down mode, DCDC_CORE can directly output 0.7 V, however, LDO_CORE must enable Internal Voltage Scaling (IVS) to supply 0.7 V to the CORE domain.*

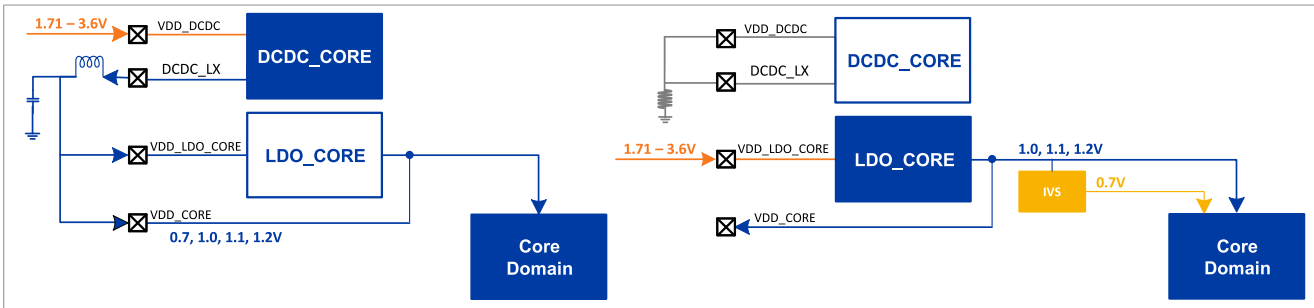

Figure 6. On-chip regulators for CORE domain

Figure 7 shows an example using a single 3.3 V supply to MCU, which uses the power-efficient DCDC_CORE. It can also be changed to low-cost LDO_CORE by referring to Figure 6.

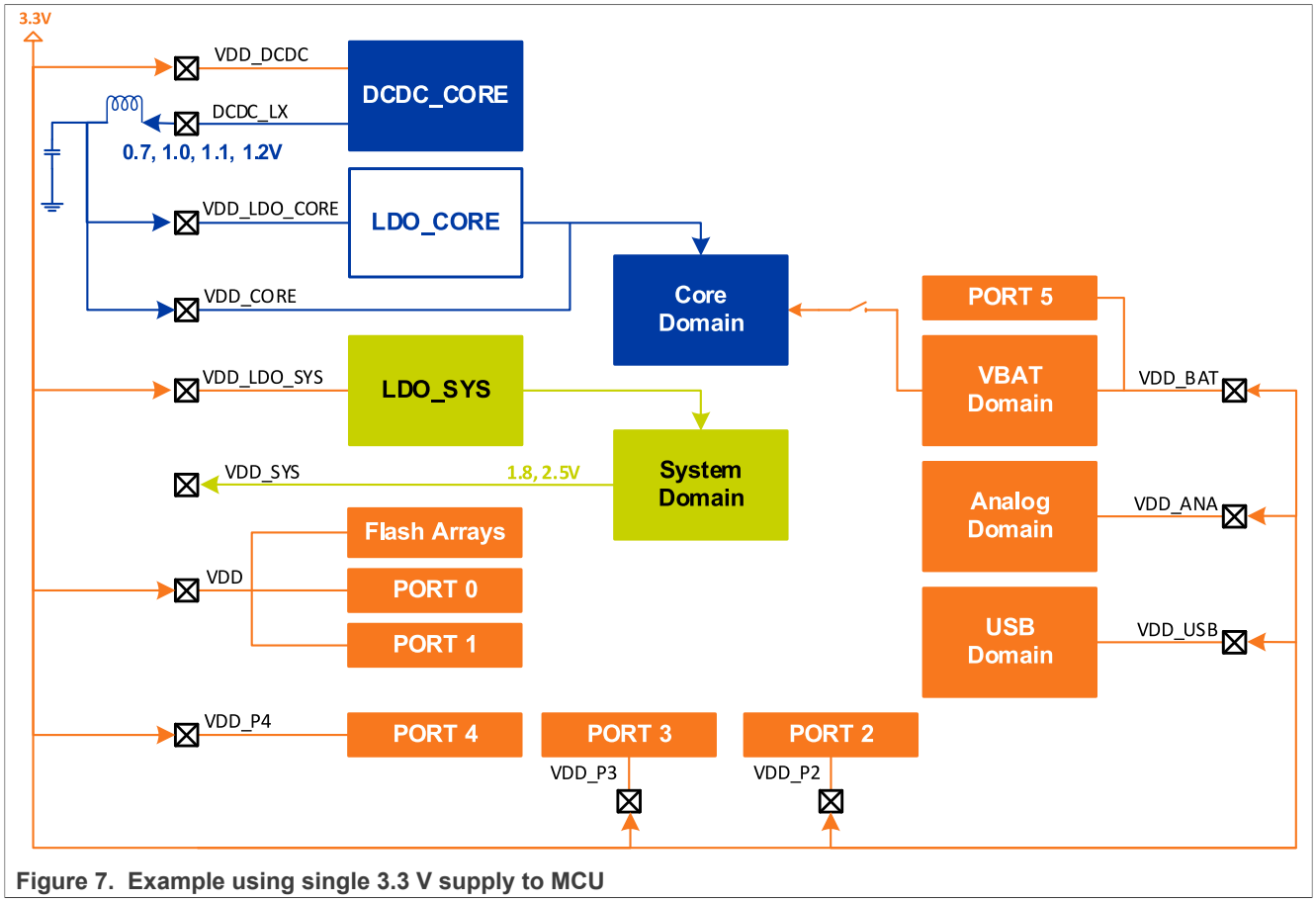

Figure 7. Example using single 3.3 V supply to MCU

3 Power modes

The device supports Active, Sleep, Deep Sleep, Power down, Deep Power Down, and VBAT power modes. Table 2 describes the status of Clock, CORE_MAIN domain, CORE_WAKE domain, SYSTEM domain, FLASH, and SRAM in different power modes. Table 2 can be used to compare the status of these modules in different power modes or find the status of these modules in a certain power mode.

Table 2. Modules status and power modes

	Active	Sleep	Deep Sleep	Power Down	Deep Power Down	VBAT
Clock gate off	NO	Only CPU	Optional[1]	All	All	All
CORE_MAIN	ON	ON	LP[2]	Static[3]	OFF[4]	OFF
CORE_WAKE	ON	ON	LP	LP/Static	OFF	OFF
SYSTEM	ON	ON	ON	ON	ON	OFF
Flash	ON/Static	ON/Static	Static	OFF	OFF	OFF
System SRAM	ON/Static	ON/Static	Static	Static/OFF	OFF	OFF
VBAT RAMA	ON/Static	ON/Static	Static	Static/OFF	Static/OFF	Static/OFF

[1] Optional means CPU, System, and Bus clock OFF, however, FIRC, SIRC, and SOSC can be enabled by configuring the corresponding STEN bit.
[2] LP means that it can be active with an async functional clock.
[3] Static means that the module is in state retention status (no clock but the data can be kept).
[4] OFF means power down.

The following sections introduce the features of different power modes.

3.1 Active

The default mode after reset.

- Clocks to CPU, memories, and peripherals are enabled.
- CPU execution is possible.
- Adjust VDD_CORE to the minimum possible value based on the required frequency to achieve optimal power consumption. For details, see Table 1.

3.2 Sleep

- CPU clock OFF.
- System and Bus clock remain ON.
- Most modules can remain operational.
- Use the **ACTIVE_CFG** register to configure core voltage level and drive strength.

3.3 Deep Sleep

- CPU clock, System clock, and Bus clock OFF.
- SRAM is in Deep Sleep mode (SRAM cannot be accessed, however, the data is retained).
- SOSC, SIRC, and FIRC can be enabled by configuring the corresponding STEN bit.
- Some modules can remain operational with low power asynchronous clock sources.

3.4 Power Down

It is the lowest power mode that can retain all registers.

- CPU clock, System clock, and Bus clock OFF.
- Flash memory is powered off.
- Place the CORE_MAIN domain of the chip into a static state.
- The CORE_WAKE domain can be configured to Deep Sleep or Power Down mode.
- SRAM blocks can be configured to deep sleep or shutdown individually.
- The voltage of the CORE domain can be regulated to 0.7 V (retention voltage).

3.5 Deep Power Down

The device wakes from Deep Power Down mode through the Reset routine.

- CPU clock, System clock, and Bus clock OFF.
- Flash memory is powered off.
- The CORE domain is powered off.
- The SYSTEM domain remains ON.
- System RAM is powered off.
- RAMA can be retained.

3.6 VBAT

VBAT mode permits the lowest power level. Powering off VDD_SYS and VDD_CORE externally puts the chip into VBAT mode.

- CPU clock, System clock, and Bus clock OFF.
- CORE domain, SYSTEM domain, Flash, and System SRAM are powered off.
- The POR sequence wakes the chip from VBAT mode.
- RAMA can be retained.

4 Low power entry and configurations

This section describes the low power mode entry controllers and related configurations in low power mode.

4.1 Low power entry

As described in Table 5, the power mode entered is controlled by CKCTRL[CKMODE] and PMCTRLMAIN[LPMODE] bit fields.

The CKCTRL[CKMODE] bit field configures the amount of clock gating when the core enters a low power mode because of WFI or WFE. Table 3 describes the functions corresponding to different CKMODE values. Configuring CKMODE > 0 requires the SLEEPDEEP field in the Arm core to become 1. Configuring PMCTRLMAIN[LPMODE] > 0 requires writing 1111b to CKMODE.

Table 3. Function of CKMODE field

CKCTRL[CKMODE]	Function
0000b	No clock gating
0001b	Core clock gated
1111b	Core, platform, and peripheral clocks are gated, and core enters low power mode

The CORE_MAIN domain and CORE_WAKE domain have independent registers for configuring low power modes that are PMCTRLMAIN and PMCTRLWAKE. Table 5 lists allowed combinations for CORE_MAIN domain and CORE_WAKE domain.

PMCTRLMAIN[LPMODE] selects the desired low power mode when a core executes a WFI or WFE instruction. Writes to this field are blocked if you have not enabled the protection level using Power Mode Protection (PMPROT). Table 4 describes the functions corresponding to different LPMODE values.

Table 4. Function of LPMODE field

PMCTRLx[LPMODE]	Function
0000b	Active/Sleep
0001b	Deep Sleep
0011b	Power Down
1111b	Deep Power Down

Table 5 shows all the configurations of the device to enter low power mode.

Table 5. Power mode entry

Power mode	CKCTRL [CKMODE]	PMPROT [LPMODE]	PMCTRLMAIN [LPMODE]	PMCTRLWAKE [LPMODE]
Active	N/A	N/A	N/A	N/A
Sleep	0000b	0000b	0000b	0000b
	0001b			

Table 5. Power mode entry*...continued*

Power mode	CKCTRL [CKMODE]	PMPROT [LPMODE]	PMCTRLMAIN [LPMODE]	PMCTRLWAKE [LPMODE]
Deep Sleep	1111b	0001b	0001b	0001b
Power Down	1111b	0011b	0011b	0001b
				0011b
Deep Power Down	1111b	1111b	1111b	1111b

Note:

- *In Sleep mode, configure CKCTRL[CKMODE] to 0000b for faster wake-up time or 0001b for lower power consumption.*
- *If more functionality is needed in Power Down mode, leave the CORE_WAKE domain in Deep Sleep mode.*

4.2 Configuration highlights

In addition to selecting power mode, you can also configure relevant hardware in different power modes. The ACTIVE_CFG and ACTIVE_CFG1 registers configure the hardware in Active and Sleep mode, such as regulators voltage level and drive strength. Autonomous change to use LP_CFG and LP_CFG1 when in low power mode (Deep Sleep, Power Down, and Deep Power Down).

Table 6. Configuration highlights

ACTIVE_CFG LP_CFG	Configures: • Regulators voltage level • Regulators drive strength
	Enables: • HVDs, LVDs • Bandgap, BG buffer, CMP buffer • VDD_CORE Glitch Detect • VDD voltage detect • Low power current reference IREF • VDD_CORE Internal Voltage Scaling (IVS)
ACTIVE_CFG1 LP_CFG1	Enables: • CMPs, CMP DACs, and VREF • USB 3V detect

5 Wake-up

Table 7 describes normal wake-up source and typical wake-up time in different low power modes, where the typical wake-up time is the data in the data sheet.

Table 7. Wake-up information

Symbol	Description	Wake-up source	Typical wake-up time
t_{SLEEP}	Sleep -> Active	All peripherals	0.22 µs
t_{DSLEEP}	Deep Sleep -> Active	Async peripherals	8.7 µs
t_{PWDN}	Power Down -> Active	WUU, Reset pin	9.8 µs
t_{DPWDN}	Deep Power Down -> Active	WUU, Reset pin	5.6 ms

6 Low power and wake-up optimization

This section explains various methods for optimizing power consumption and factors to consider for wake-up optimization.

6.1 Power consumption optimization

Following are the different ways of performing power consumption optimization.

- Regulator
  - Configure the appropriate voltage level and drive strength.
  - In Power Down mode, DCDC_CORE and IVS can provide 0.7 V to the CORE domain. DCDC_CORE provides better efficiency and therefore lower power consumption, and IVS reduce wake-up latency with fast voltage changes.
- Peripherals
  - Disable unused analog peripherals by ACTIVE_CFG1 and LP_CFG1 registers.
- Memories
  - Flash
    - Set FLASHDOZE bit when the MCU enters low power mode.
  - SRAM
    - Manual clock gating by the AHBCLKCTRL0 register of SYSCON.
    - Auto clock gating by the AUTOCLKGATEOVERRIDE and AUTOCLKGATEOVERRIDEC registers of SYSCON.
    - RAMA is the only block that can be retained in all power modes.
    - SYSTEM SRAM can be individually disabled or retained as shown in Table 8.

Table 8. SRAM configurations

SRAMDIS[i]	SRAMRET[i]	MCU Power Mode	SRAM power mode
1b	N/A	All	Shutdown
0b	N/A	Active or Sleep	Active
		Deep Sleep	Deep Sleep
	0b	Power Down	Deep Sleep
	1b		Shutdown
N/A	N/A	Deep Power Down or VBAT	Shutdown

Note:

- *Active of SRAM means you can access SRAM normally.*
- *Deep Sleep of SRAM means you cannot access SRAM but the data is retained.*
- *Shutdown of SRAM means you cannot access SRAM and data is lost.*

- Clocks
  - Select the appropriate CPU clock.
  - Disable unused clock source.
  - Configure the AHBCLKCTRLx registers of SYSCON to disable or divide the clocks to modules.
  - Disable SCG LDO if PLL and SOSC are not used.
- Monitors
  - Disable unused voltage monitors.

6.2 Wake-up time consideration

The following are some points to consider with wake-up time:

- SLOW_CLK frequency
  - The wake-up process is implemented through the core mode controller (CMC). SLOW_CLK is the clock source of CMC and its frequency is equal to ¼ SYSTEM_CLK.
- Different VDD_CORE level
  - Recovery time required for different voltage levels. For details, refer to the "LPWKUP_DELAY configuration" table in the *MCX N23x Reference Manual*.
- The longer time of Clock recovery time and Flash recovery time.
- Interrupt latency

7 Demo operation

The following demo is used to reproduce the typical power consumption (see section "*Power consumption operating behaviors*") and wake-up time (see "*Power mode transition operating behaviors*" table) data in the *MCX N23x Data Sheet*. You can also modify its parameters to measure the power consumption and wake-up time corresponding to different configurations.

7.1 Hardware requirement

- FRDM-MCXN236 board Rev. C
- One Type-C USB cable

Note:

- *To measure wake-up time, the prerequisite is to prepare an oscilloscope or logic analyzer.*
- *To measure power consumption, the prerequisite is to prepare an MCU-Link Pro or multimeter.*

7.2 Software requirement

- IAR 9.50.1

7.3 Setup

This section explains the steps to set up the demo, download and configure the project, and select power mode. It also explains how to measure power consumption and wake-up time.

7.3.1 Hardware setup

1. Remove R71, solder the header at JP2, and use the jumper to connect as shown in Figure 8.
2. Use a Type-C USB cable to connect J10 of FRDM-MCXN236 and the USB port of the PC.

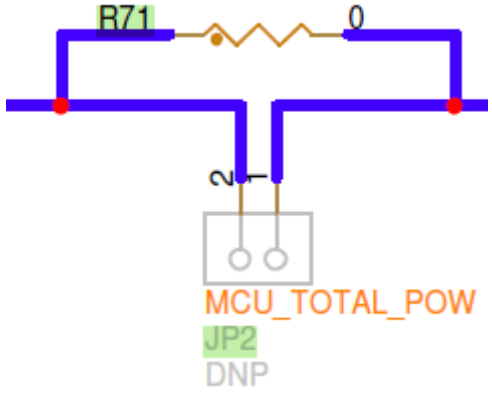

Figure 8. Partial schematic of FRDM-MCXN236

7.3.2 Download project

Download the project from the link: https://github.com/nxp-appcodehub/dm-low-power-measurement-on-mcxn236 or refer to the associated software file (*AN14317SW*) available on nxp.com.

7.3.3 Configure and download project

As shown in Figure 8, the default configuration for this project is WAKEUP_EN=0, which is used to reproduce the power consumption data in the data sheet. If you want to reproduce the wake-up time in the data sheet, update it to WAKEUP_EN=1.

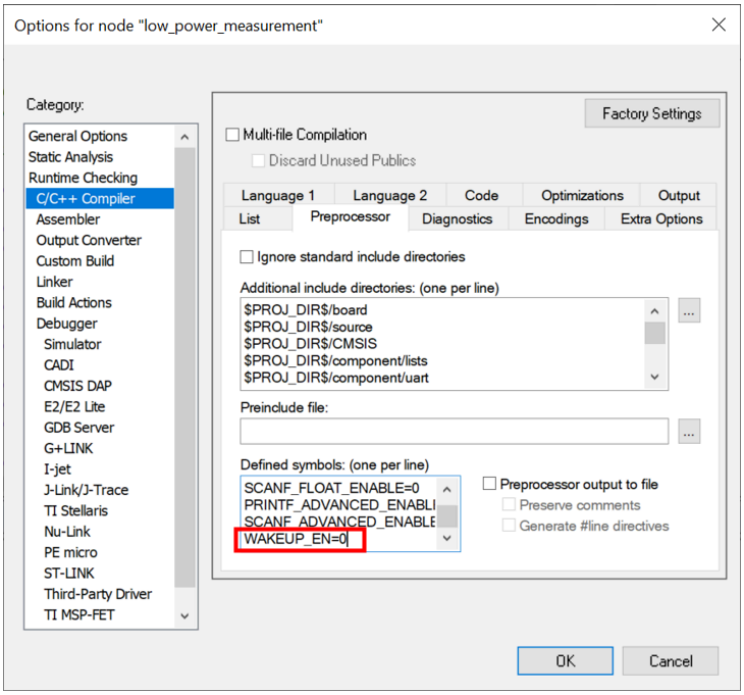

Figure 9. Parameter configuration

As shown in Figure 10, make and download the project to FRDM-MCXN236.

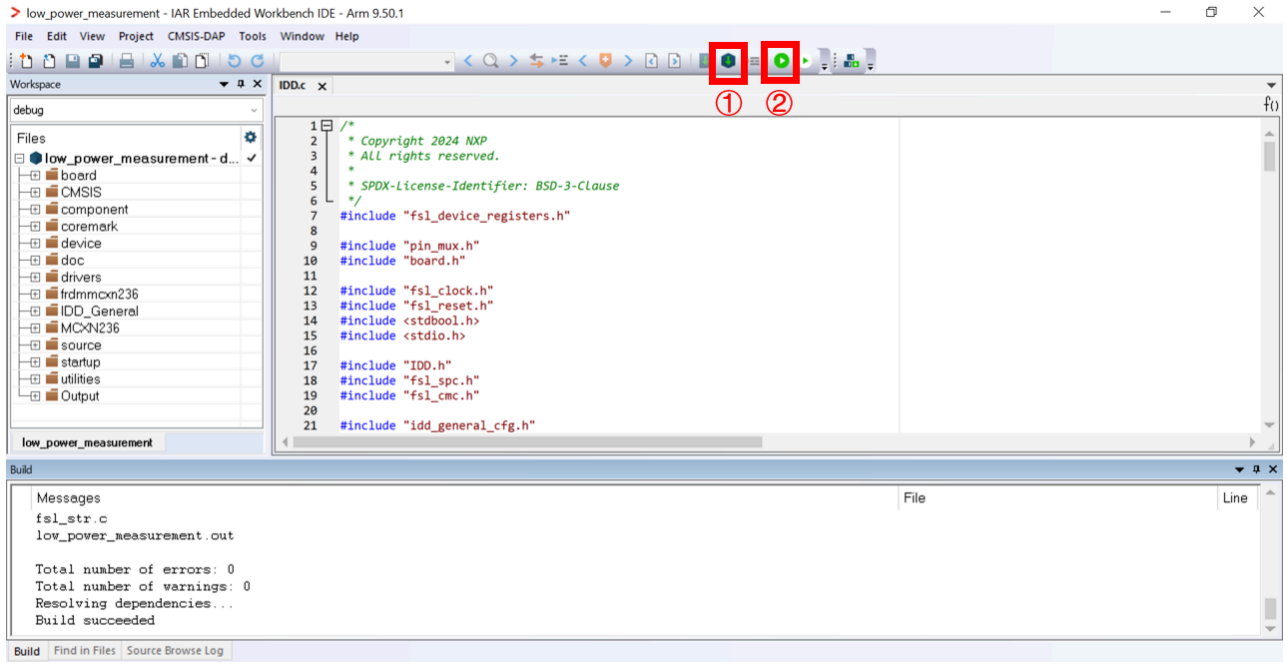

Figure 10. Make and download project

7.3.4 Select power mode

1. Open a serial terminal with a 57600 baud rate.
2. Follow the prompts in Figure 11 and enter a number to select a different power mode.

```
**********************************************************************
*          Starting low power measurement on mcxn236                 *
**********************************************************************

Select power mode:
0.      Symbol_IDD_ACT_OD_1.
5.      Symbol_IDD_CM_OD_1.
61.     Symbol_IDD_SLEEP.
69.     Symbol_IDD_DSLEEP_LP.
86.     Symbol_IDD_PDOWN_LP.
103.    Symbol_IDD_PDOWN_RET_0V7.
109.    Symbol_IDD_DPOWN_32K.
*     Please input Number and end with carriage return.     *
```

Figure 11. Select power mode

3. After inputting the case number, the symbol and register values are printed as shown in Figure 12.

Figure 12. Configuration information of different power modes

```
select_case = 0
IDD_ACT_OD_1

Configure 1A.
Active Mode Selected
Read registers:
CMC CKCTRL                  :0x0
CMC PMPROT                  :0x0
CMC GPMCTRL                 :0x0
CMC PMCTRLMAIN              :0x0
CMC PMCTRLWAKE              :0x0
CMC SRAMDIS0                :0x0
CMC SRAMRET0                :0x0
CMC FLASHCR                 :0x0
CMC DBGCTL                  :0x0
SCG RCCR                    :0x5000000
SCG SOSCCSR                 :0x1810001
SCG_SOSCCFG                 :0x14
SCG SIRCCSR                 :0x1800000
SCG FIRCCSR                 :0x800000
SCG FIRCCFG                 :0x0
SCG LDOCSR                  :0x80000009
SCG APLLCSR                 :0x3000003
```

7.3.5 Measure power consumption

Two ways of measuring power consumption are:

- Using MCU-Link Pro
- Using multimeter

7.3.5.1 Use MCU-Link Pro and MCUXpresso IDE to measure power consumption

1. Connect MCU-Link Pro and FRDM-MCXN236 according to Table 9 and afterward connect MCU-Link Pro and FRDM-MCXN236 to the host PC.

Table 9. MCU-Link Pro and FRDM-MCXN236 connection

MCU-Link Pro	FRDM-MCXN236
J9-1	JP2-2
J9-3	JP2-1
J9-2	J3-14

2. Follow the steps shown in Figure 13 to measure current with MCUXpresso.

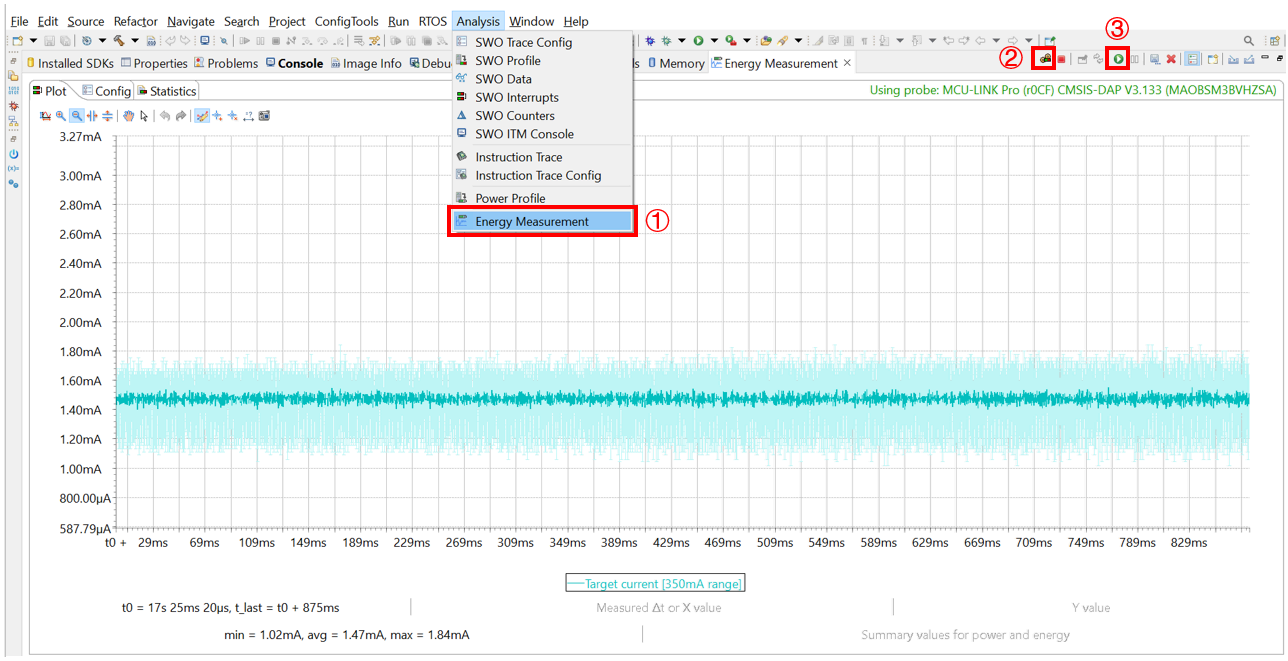

Figure 13. MCUXpresso energy measurement

7.3.5.2 Use a multimeter to measure power consumption

You can also use a multimeter to measure the current at JP2 of the FRDM-MCXN236 board.

7.3.6 Measure wake-up time

As shown in Figure 14, get the wake-up time by measuring the delay between the falling edges of J8-13 (P0_20) and J8-28 (P3_11) using an oscilloscope.

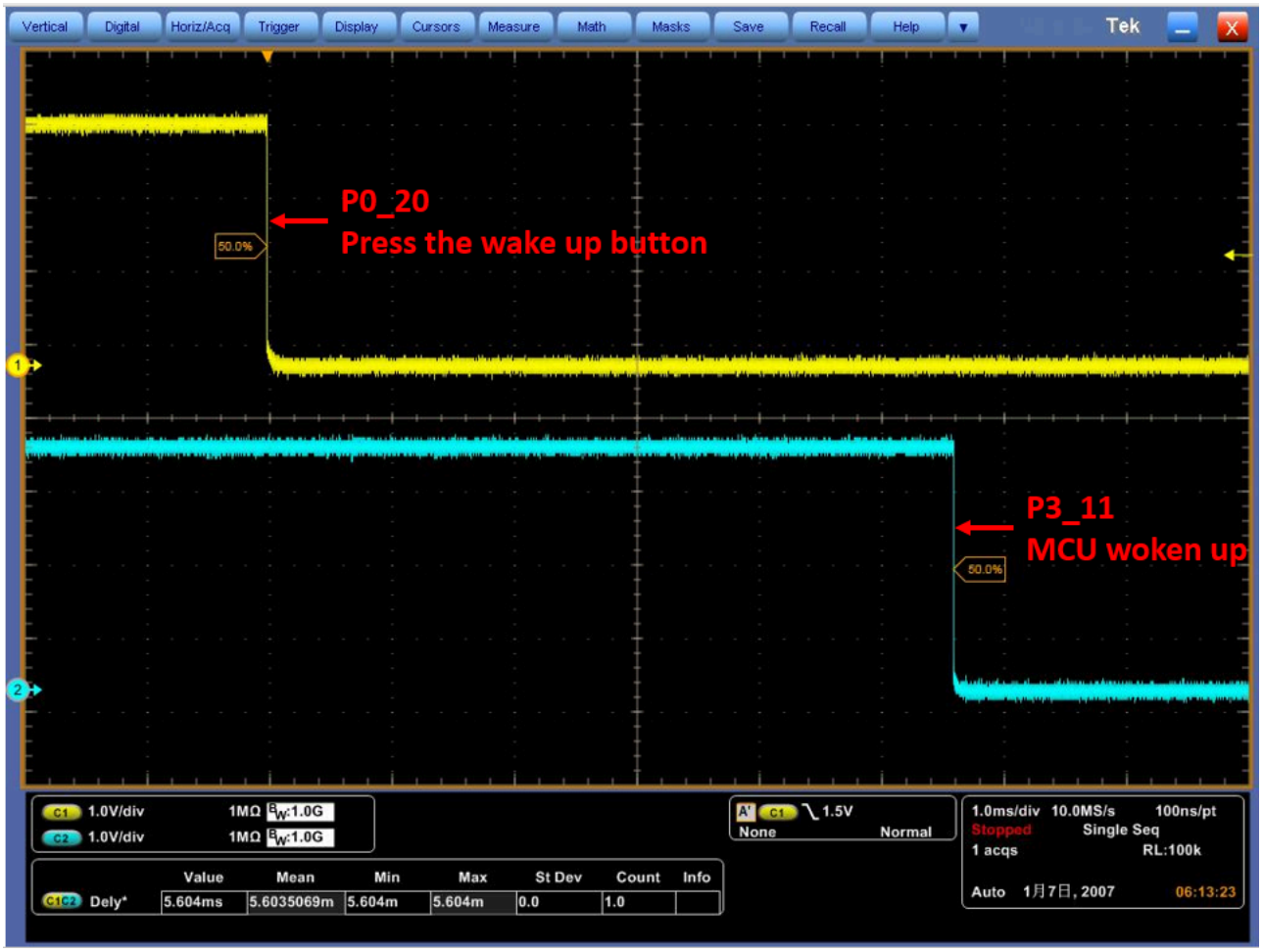

Figure 14. Measure wake-up time

7.4 Reference results

The power consumption and wake-up time in Table 10 are provided as a reference.

Note:

- *Different samples, temperature, and measuring instruments affect test results.*
- *Before measuring each data, POR is required.*
- *To measure the power consumption of IDD_CM_OD_1, port CoreMark to this project.*
- *The wake-up time of Deep Power Down must be configured as 144 MHz boot, and all other measurement data uses the default 48 MHz boot.*
- *To measure the wake-up time of other configurations, refer to the "LPWKUP_DELAY configuration" table in the MCX N23x Reference Manual.*
- *Refer to “Power mode transition operating behaviors” table in MCX N23x data sheet that lists wake-up time, and “Power consumption operating behaviors” section in MCX N23x data sheet that describes different power consumption data.*

Table 10. Test results on the FRDM-MCXN236 board Rev. C

Symbol	Power consumption in data sheet	Tested power consumption	Wake-up time in data sheet	Tested wake-up time
IDD_ACT_OD_1	7.43 mA	7.679 mA	N/A	N/A
IDD_CM_OD_1	8.93 mA	8.763 mA	N/A	N/A
IDD_SLEEP	1.48 mA	1.451 mA	0.22 µs	0.22 µs
IDD_DSLEEP_LP	0.12 mA	0.120 mA	8.7 µs	8.6 µs
IDD_PDOWN_LP	1.75 µA	1.95 µA	9.8 µs	9.7 µs
IDD_PDOWN_RET_0V7	2.52 µA	2.89 µA	N/A	N/A
IDD_DPOWN_32K	1.28 µA	1.55 µA	5.6 ms	5.6 ms

8 Summary

This application note introduces the power domains, power modes, low power entry, wake-up, and low power and wake-up optimization of MCXN23x, and provides a demo to reproduce the typical power consumption and wake-up time data in the *MCX N23x data sheet*.

9 Note about the source code in the document

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10 Revision history

Table 11 summarizes the revisions to this document.

Table 11. Revision history

Document ID	Release date	Description
AN14317 v.1	14 May 2024	Initial public release

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