

AN14246

Power supply IC PCA9450C

Rev. 1.0 — 1 July 2024

Application note

Document information

Information	Content
Keywords	Power supply IC PCA9450C
Abstract	This application note provides information regarding peripheral device power connection using the PCA9450C



1 Overview

The PCA9450C is a power supply IC (PMIC: Power Management IC) designed for i.MX 8M Plus application processor. This IC provides the power supply voltage required for the i.MX 8M Plus and controls the power-up/down sequence and operating modes. It can support power supply voltage for peripheral devices connected to the i.MX 8M Plus. The PCA9450C PMIC incorporates power supply design for applications using the i.MX 8M Plus.

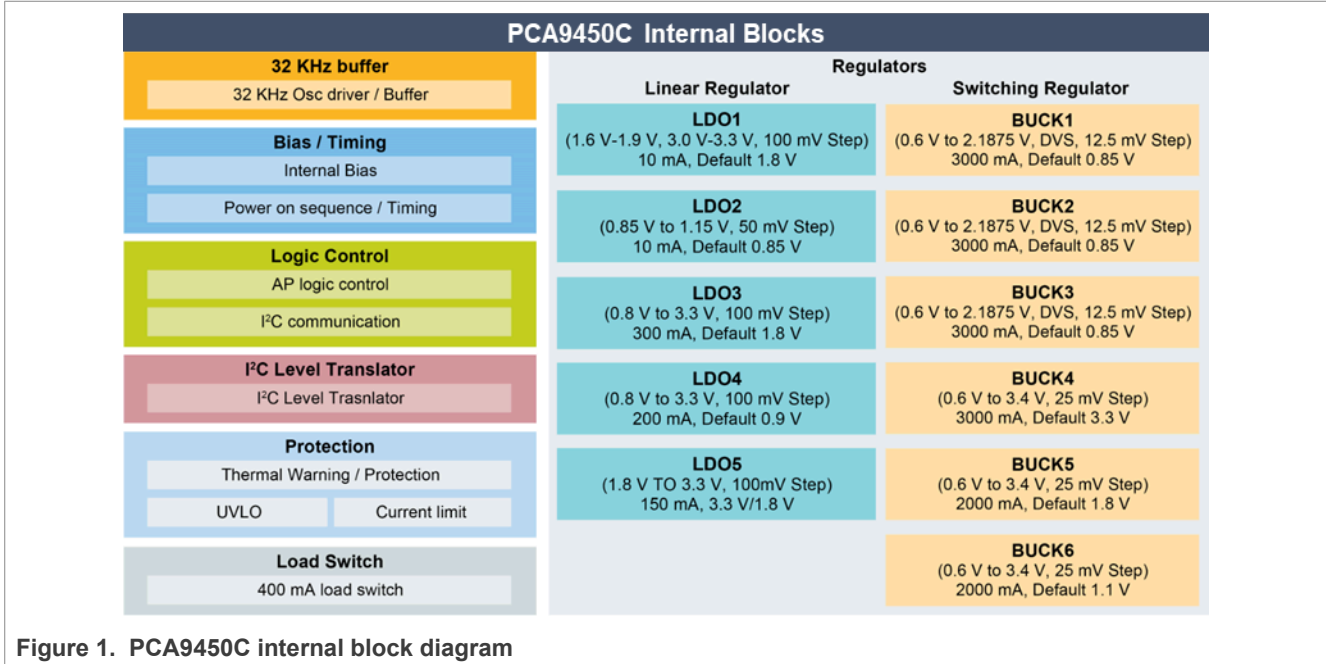


Figure 1. PCA9450C internal block diagram

1.1 Features

- PMIC optimized for i.MX 8M Plus
 - Compatible with all i.MX 8M Plus operating modes
 - Supports power supply voltage and required Power Up/Down sequences
- Supports powering LPDDR4/DDR4/DDR3L memory
- 6-channel BUCK regulator (BUCK1~6)
 - Two channels of 3A BUCK regulators (BUCK1, 3)
BUCK1 and BUCK3 can be connected in dual phase (working in parallel) to provide 6A output Equipped with DVS function¹
 - Two channels of 3A BUCK regulators (BUCK2, 4)
 - Two channels of 2A BUCK regulators (BUCK5, 6)
- 5-channel Linear regulator (LDO1~5)
 - i.MX 8M Plus SNVS mode² Two channels of 10 mA LDOs for IO power (LDO1,2)
 - 300 mA LDO 1 channel (LDO3)
 - 200 mA LDO 1 channel (LDO4)
 - 150 mA LDO 1 channel (LDO5)

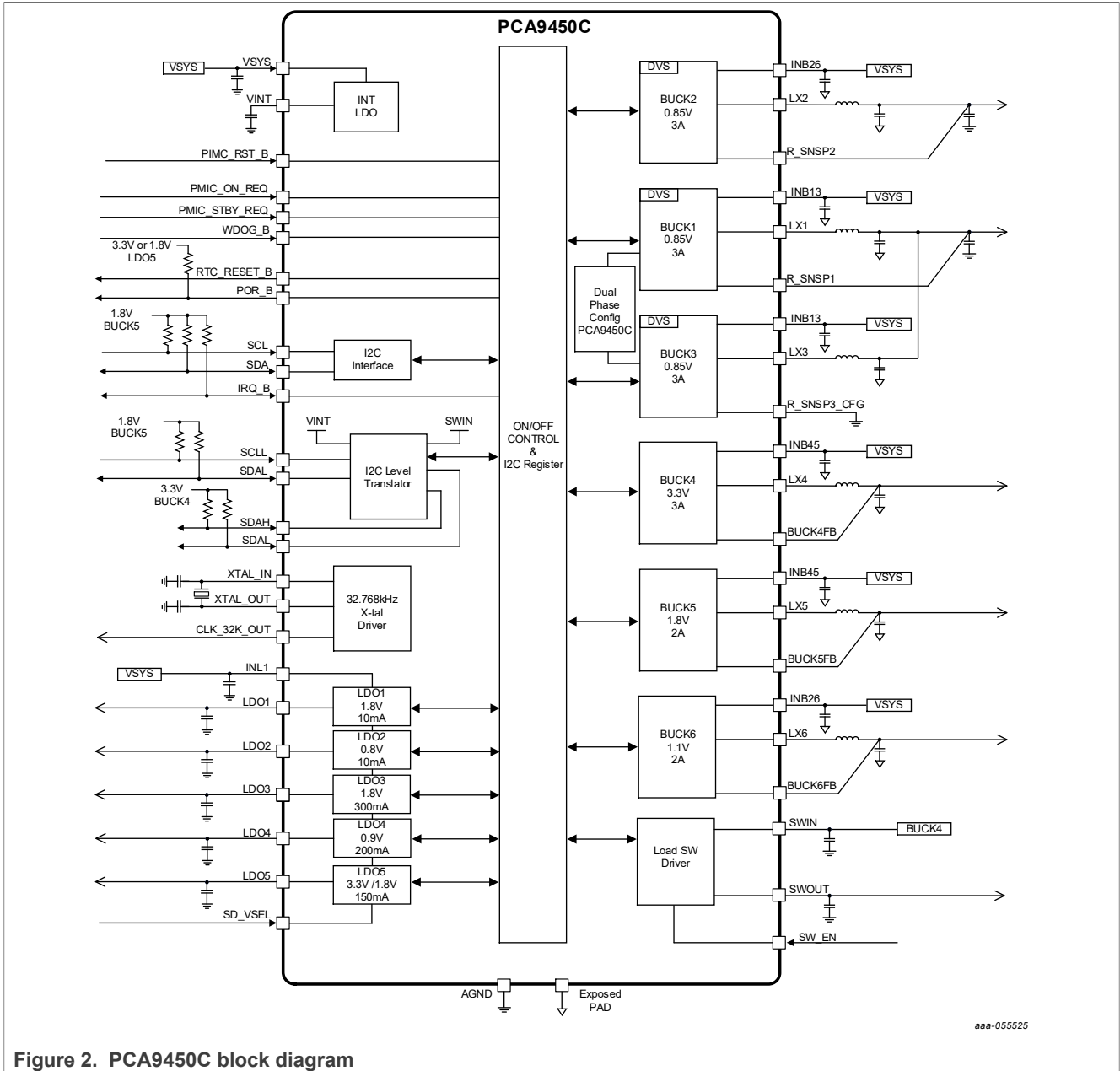
1 DVS (Dynamic Voltage Scaling): This control dynamically changes the PCA9450C power supply voltage according to the i.MX 8M Plus operation mode. The voltage slew rate at the time of change can also be set.

2 SNVS (Secure Non-Volatile Storage) mode: In the i.MX 8M Plus, only the built-in RTC and some functions (wake-up, etc.) are operating. The power from PCA9450C is supplied only to the SNVS power supply (NVCC_SNVS_1P8).

- 400 mA Load switch 1 channel (Load SW)
- Equipped with protection and monitoring functions
 - Output voltage monitoring and overcurrent protection
 - Input undervoltage monitoring
 - Temperature monitoring
- 32.768 kHz crystal oscillation driver mounted
- I2C communication interface (Fast Plus Mode max 1 MHz): PCA9450C control
- I2C level translator on board (1.8 V to 3.3 V or 5 V)
- Temperature range (T_{amb}): - 40 °C ~ +105 °C
- HVQFN 56-pin: Size 7 x 7 x 0.4 mm

2 Block diagram

[Figure 2](#) shows a block diagram of the PCA9450C.



aaa-055525

Figure 2. PCA9450C block diagram

- The VSYS pin is the power supply input pin of the PCA9450C. PCA9450C state transitions to the power supply mode shown in [Table 2](#) according to the VSYS input voltage value. The guaranteed operating range is 2.7 V to 5.5 V, and the absolute maximum rating is -0.5 V to 6.0 V. Each BUCK input should be supplied with the same power supply as VSYS.
- The SWIN pin is the input pin for the Load SW and is mainly used as a 3.3 V power supply for the SD CARD. When using the Load SW, SWIN pin should be connected to the BUCK4 output (3.3 V).
- BUCK1 and BUCK3 regulators are used as dual phase mode. BUCK1 and BUCK3 regulators are controlled by BUCK1 registers.
- The i.MX 8M Plus does not use the LDO2 regulator, which is always on in SNVS mode, RUN mode, and STANDBY mode (described below), so do not leave the LDO2 pin open and connect it to ground with a capacitor.

- The i.MX 8M Plus does not use the LDO4 regulator. It is turned off by default. If used for other purposes, a register setting is required.

3 Power supply table and connection diagram

3.1 i.MX 8M Plus and peripheral device power supply table

The PCA9450C supports power supply to i.MX 8M Plus and peripheral devices. Table 1 shows the supply voltage to each peripheral device.

Table 1. i.MX 8M Plus and Peripherals Power Supply Table

MPU Peripherals	Power 5V						
	PCA9450C					External Components	
	0.85V / 6A	1.1V / 2A	1.8V / 2A	3.3V / 3A	Load SW	3.3V	5V
i.MX 8M Plus	✓	✓	✓	✓			
LPDDR4 Memory		✓	✓				
NOR Flash			✓				
NAND Flash			✓	✓			
Wi-Fi/Bluetooth			✓	✓			
SD Card					✓		
Camera			✓			✓	✓
Display			✓			✓	✓
Audio Codec				✓			✓
Ethernet			✓	✓			
USB Type-A/C				✓			✓

All of the i.MX 8M Plus's internal logic and interface power can be supplied from the PCA9450C. The PCA9450C can power memory (DDR, Flash, SD Card), Wi-Fi/Bluetooth, and other devices. However, additional power supplies may be required for Camera, Display, Audio Codec, USB, etc., depending on the required current and voltage.

3.2 i.MX 8M Plus and peripheral device power connection diagram

Figure 3 shows the power supply connection diagram for i.MX 8M Plus and peripheral devices. The "Selectable voltage 1.8V or 3.3V for I/F" in the figure means that either BUCK4 (3.3V) or BUCK5 (1.8V) can be selected for connection to the power supply starting from NVCC_.

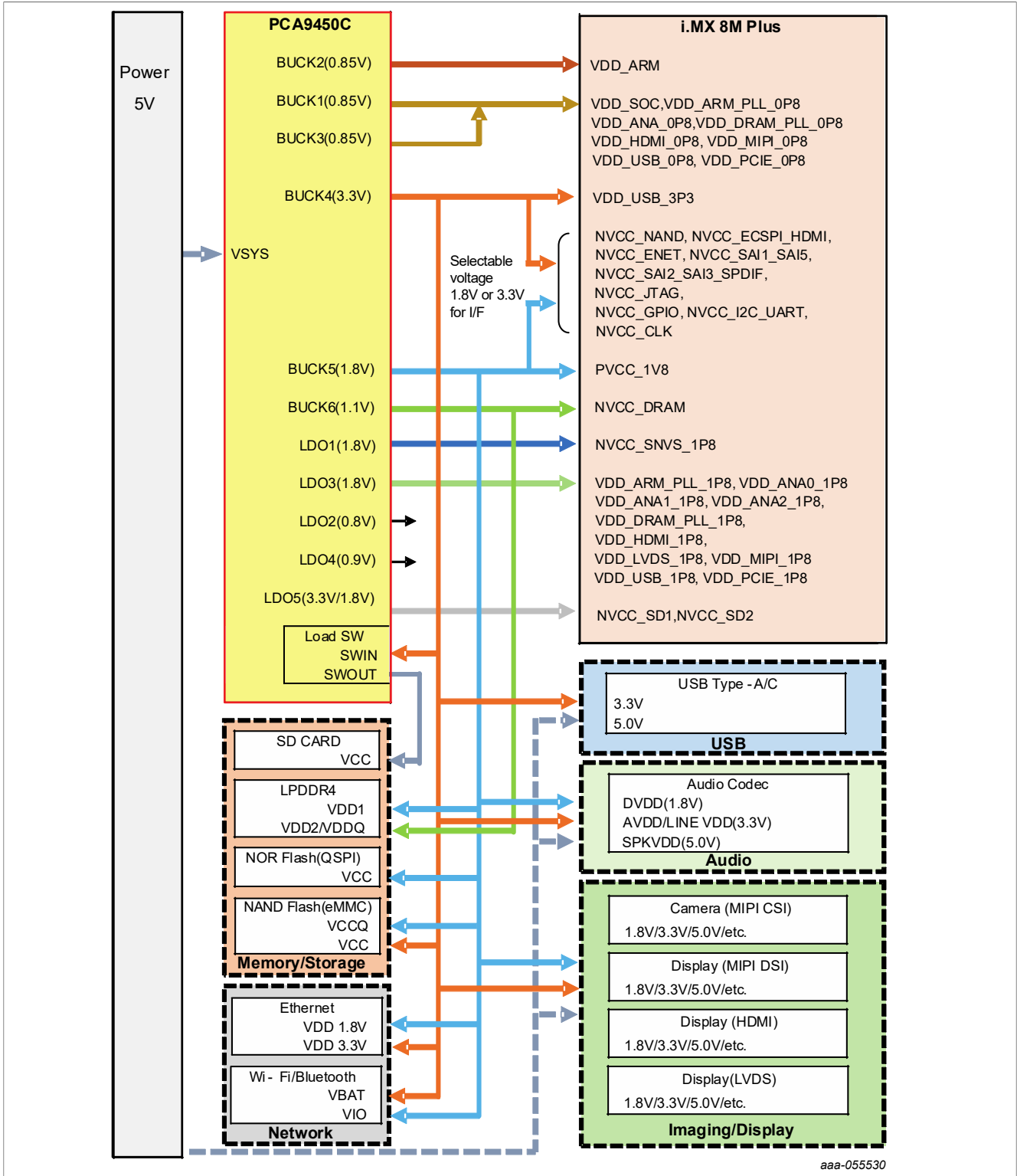


Figure 3. i.MX 8M Plus and peripheral device power connection diagram

4 Connection by DDR memory type

The i.MX 8M Plus supports three types of DDR memory (LPDDR4/DDR4/DDR3L). The PCA9450C can support the supply voltage required for each memory by setting the BUCK6 voltage to 1.1 V or 1.2 V or 1.35 V in the register settings after i.MX 8M Plus start-up. Figure 4 shows a connection diagram for each DDR memory type.

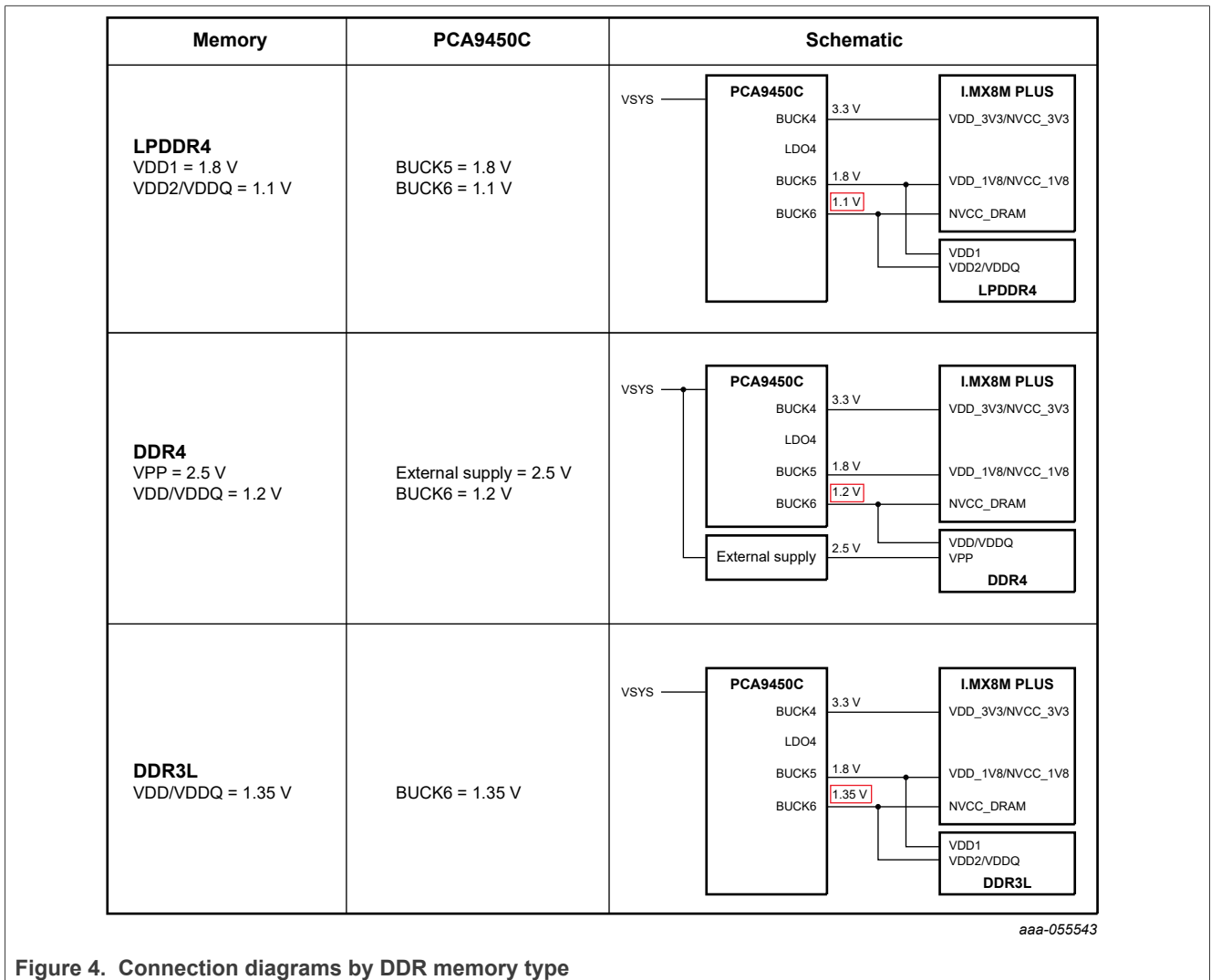


Figure 4. Connection diagrams by DDR memory type

5 Operation mode Transition

5.1 Operating mode

The PCA9450C has seven operating modes: OFF mode, READY mode, SNVS mode, PWRUP mode, RUN mode, STANDBY mode, and PWRDN mode, controlled by the input voltage on the VSYS pin and an external control signal.

5.1.1 OFF mode

In the OFF mode, PCA9450C has no VSYS pin voltage.

When the VSYS pin voltage falls below the VSYS_POR (Power On Reset) threshold voltage, the PMIC transitions to OFF mode from any other mode. In this mode, all regulators are turned off and all internal registers of the PMIC are reset.

5.1.2 READY mode

In the READY mode, the PCA9450C only operates its internal logic.

When the voltage on the VSYS pin exceeds the VSYS_POR threshold voltage, the device transitions to READY mode from OFF mode. The internal LDOs are enabled and ready to transition to SNVS mode.

5.1.3 SNVS mode

In the SNVS mode, PCA9450C supplies power to the SNVS block of the i.MX 8M Plus.

When the voltage on the VSYS pin exceeds the VSYS_UVLO (Under Voltage Lock Out) voltage, LDO1 and LDO2 start to output, powering the SNVS block of the i.MX 8M Plus and providing a clock from the 32.768 kHz crystal oscillator driver.

5.1.4 PWRUP mode

In the PWRUP mode, PCA9450C regulator starts Power Up sequence.

For Power Up sequence, see [Section 5.3.1](#).

5.1.5 RUN mode

In the RUN mode, PCA9450C regulators are on.

When the PMIC_ON_REQ pin (which requests the transition to RUN mode from SNVS mode) goes HIGH, all regulators start to output voltage according to the Power UP sequence.

5.1.6 STANDBY mode

In the STANDBY mode, the PCA9450C supplies the required voltage when the i.MX 8M Plus is in standby mode.

When the PMIC_STBY_REQ pin (which requests the transition to STANDBY mode from RUN mode) is HIGH, BUCK1/3 and BUCK2 operate at a preset low voltage or turn off. The other regulators continue to operate as in the RUN mode.

5.1.7 PWRDN mode

In the PWRDN mode, PCA9450C regulator starts the Power Down sequence.

See [Section 5.3.2](#) for Power Down sequence.

5.2 Operating mode transition table

5.2.1 State transition table for VSYS terminals and major terminals

The state transitions of the VSYS pin and main pins are shown in [Table 2](#). The "*" in the table means that the input signal level has no effect on the operating mode transitions.

Table 2. State transition table for VSYS pin and major pins

	I/O	OFF mode	READY mode	SNVS mode	PWRUP mode	RUN mode	STANDBY mode	PWRDN mode
VSYS	I	< VSYS_POR	> VSYS_POR	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO	> VSYS_UVLO
PMIC_ON_REQ	I	*	*	LOW	HIGH	HIGH	HIGH	LOW
PMIC_STBY_REQ	I	*	*	*	*	LOW	HIGH	*
POR_B	O	LOW	LOW	LOW	LOW	HIGH	HIGH	LOW
RTC_RESET_B	O	LOW	LOW	HIGH	HIGH	HIGH	HIGH	HIGH

The POR_B pin is the reset signal output pin to the i.MX 8M Plus, and the RTC_RESET_B pin is the reset signal output pin for the 32.768 kHz crystal oscillator driver. A HIGH output indicates reset release, and a LOW output indicates reset status.

5.2.2 Regulator state transition table by mode of operation

Table 3 shows the operating conditions of the regulator in each operating mode. The "*" in the table means that the output signal level is indefinite.

Table 3. Regulator state transition table by operating mode

	OFF mode	READY mode	SNVS mode	PWRUP mode	RUN mode	STANDBY mode	PWRDN mode
BUCK1/BUCK3	OFF	OFF	OFF	*	0.85V	0.85V	*
BUCK2	OFF	OFF	OFF	*	0.85V	0.85V or OFF	*
BUCK4	OFF	OFF	OFF	*	3.3V	3.3V	*
BUCK5	OFF	OFF	OFF	*	1.8V	1.8V	*
BUCK6	OFF	OFF	OFF	*	1.1V	1.1V	*
LDO1	OFF	OFF	1.8V	1.8V	1.8V	1.8V	1.8V
LDO2	OFF	OFF	0.85V	0.85V	0.85V	0.85V	0.85V
LDO3	OFF	OFF	OFF	*	1.8V	1.8V	*
LDO4	OFF	OFF	OFF	*	OFF	OFF	*
LDO5	OFF	OFF	OFF	*	1.8V or 3.3V	1.8V or 3.3V	*

5.3 Power Up/Down sequence

Figure 5 shows the Power Up/Down sequence.

POK in Figure 5 means Output Power good or Power OK, indicating that 85 % of the set output voltage has been reached.

VINT in Figure 5 shows the output of the internal LDO, and CLK_32K_OUT shows the output of the 32.768 kHz crystal oscillation driver.

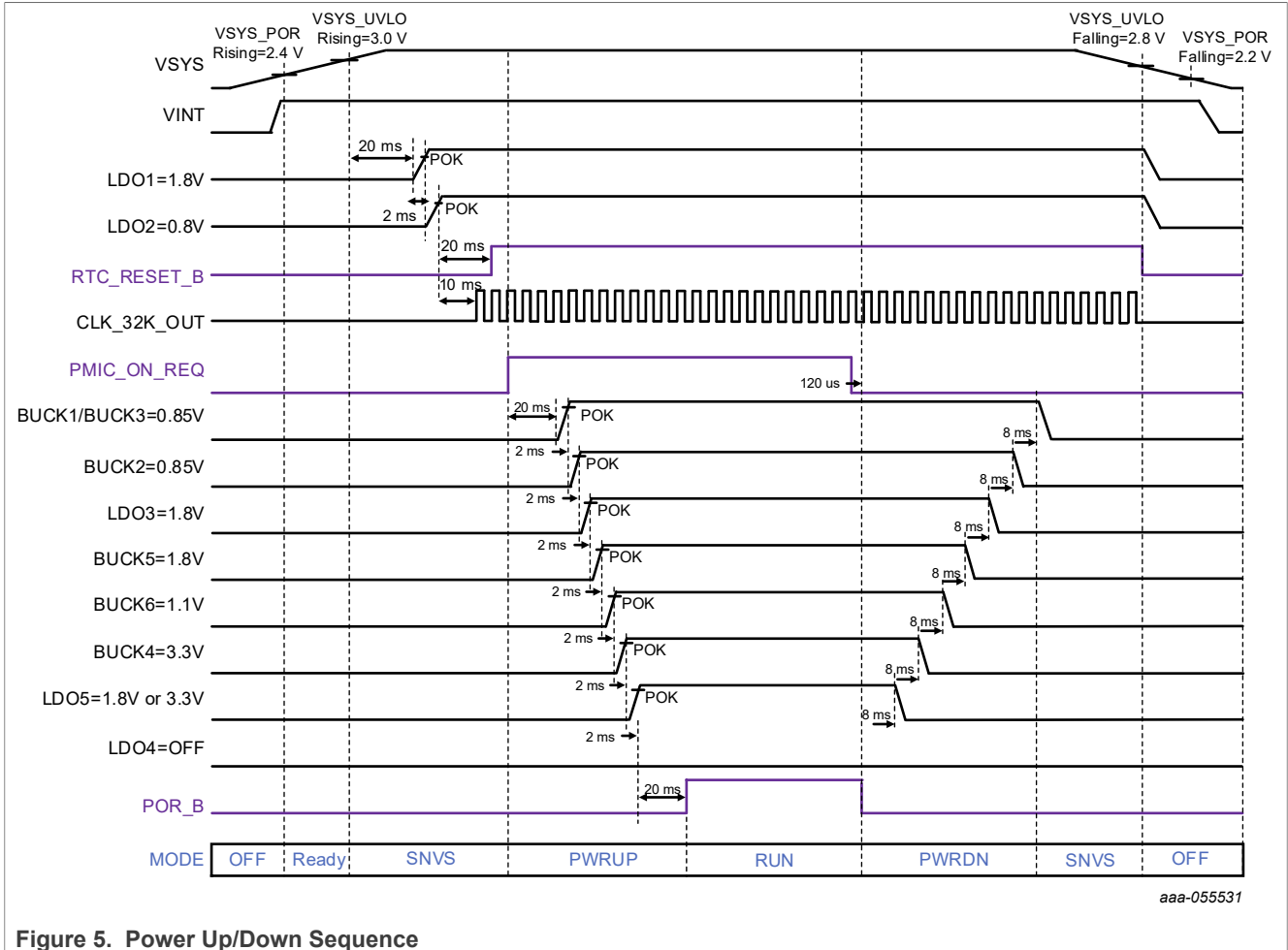


Figure 5. Power Up/Down Sequence

5.3.1 Power Up sequence

When the VSYS pin voltage exceeds the VSYS_POR threshold voltage, the device transitions to READY mode from OFF mode

When the VSYS pin voltage exceeds the VSYS_UVLO (Under Voltage Lock Out) voltage, the device transitions to SNVS mode. LDO1 starts output after 20 ms. When LDO1 reaches POK, LDO2 starts output after 2 ms. When the LDO2 reaches POK, CLK_32K_OUT starts output after 10 ms and RTC_RESET_B asserts HIGH after 20 ms.

When a HIGH level signal is applied to the PMIC_ON_REQ pin from the i.MX 8M Plus in the SNVS mode, the device transitions to the PWRUP mode. After 20 ms from that point, the power-up sequence starts and each regulator starts up in the order BUCK1/3, BUCK2, LDO3, BUCK5, BUCK6, BUCK4, and LDO5. When the output voltage of each regulator reaches POK, the next regulator begins to rise after an interval of 2 ms.

5.3.2 Power Down sequence

When a LOW level is applied to the PMIC_ON_REQ pin in RUN mode or STANDBY mode, the IC transitions to PWRDN mode after debounce time (120 us) and the POR_B signal falls to start the Power Down sequence. Each regulator starts powering down at 8 ms intervals in the reverse order of the Power Up sequence. When the last BUCK1/3 finishes power down, it transitions to SNVS mode.

When the VSYS pin voltage falls below the VSYS_UVLO (Under Voltage Lock Out) voltage, LDO1 and LDO2 and the 32.768-kHz clock supply are stopped and the device transitions to OFF mode. When the VSYS pin voltage falls below the VSYS_POR (Power On Reset) voltage, the internal LDO (VINT) is stopped.

5.4 STANDBY mode transition

Figure 6 shows the transition between RUN mode and STANDBY mode controlled by the PMIC_STBY_REQ pin. When the i.MX8 Plus applies a HIGH level signal to the PMIC_STBY_REQ pin, the PCA9450C goes from RUN to STANDBY mode. When the i.MX8 Plus applies a LOW level signal to the PMIC_STBY_REQ pin, the PCA9450C goes back to RUN mode.

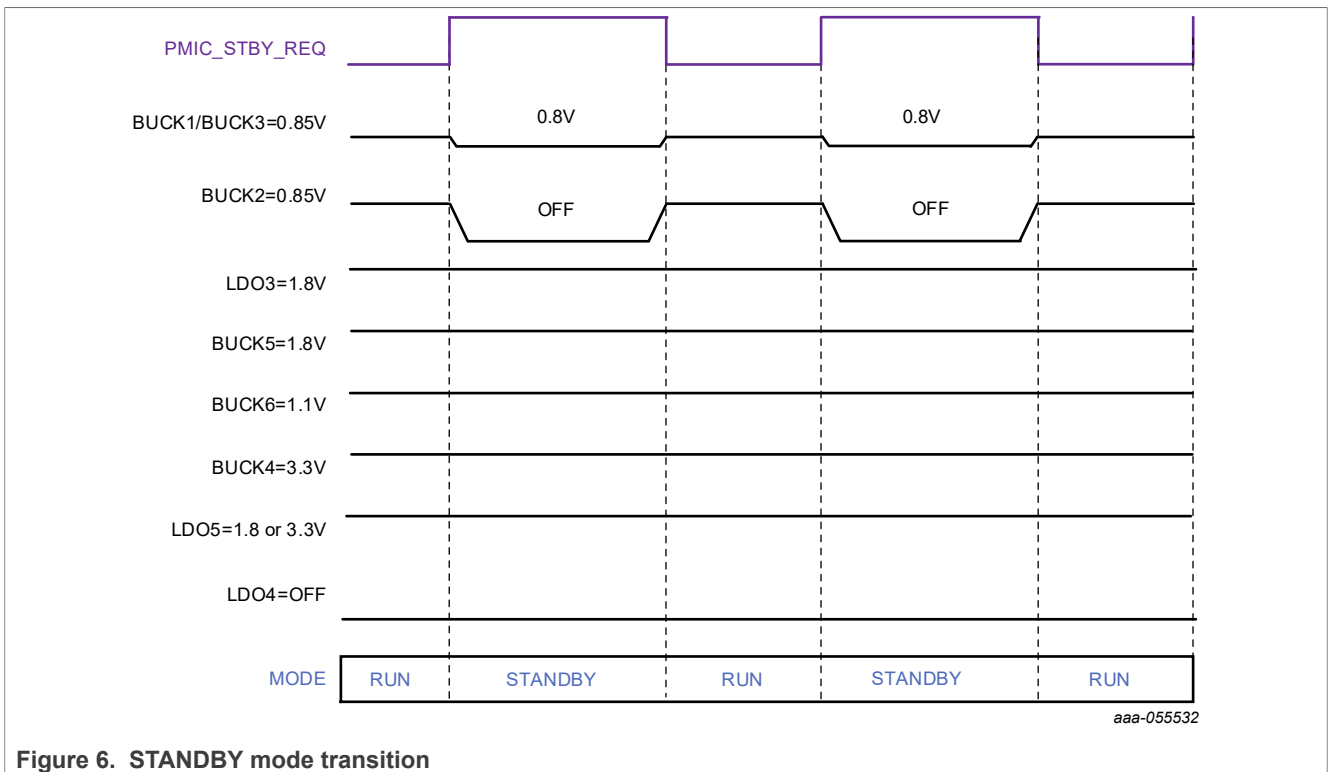


Figure 6. STANDBY mode transition

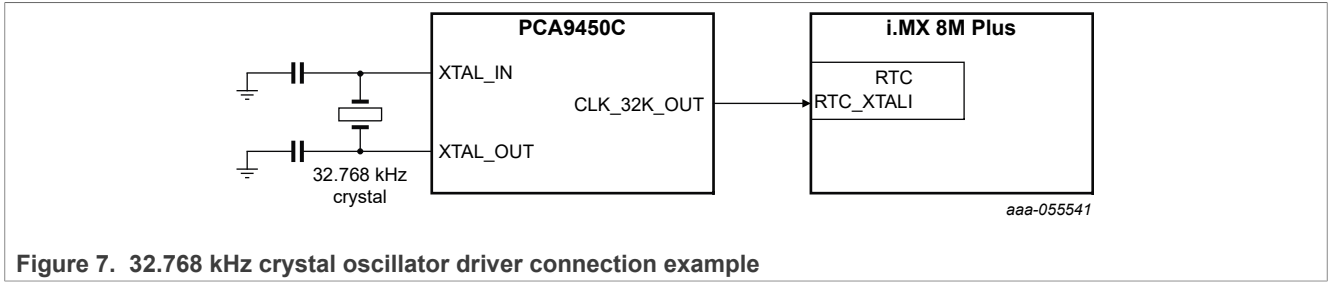
BUCK1/3 and BUCK2 can be set to different output voltages for RUN mode and STANDBY mode, respectively. This function reduces the overall system power consumption during STANDBY mode.

In the example shown in Figure 6, BUCK1/3 = 0.85 V and BUCK2 = 0.85 V during RUN mode, and BUCK1/3 = 0.8 V and BUCK2 = OFF during STANDBY mode.

6 System function blocks

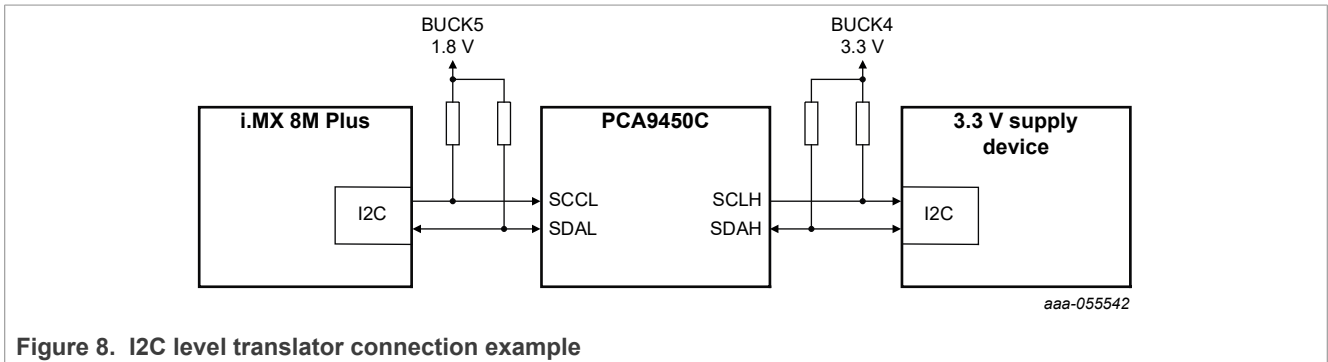
6.1 32.768 kHz crystal oscillator driver

The PCA9450C has a 32.768 kHz crystal driver that provides an accurate clock to the i.MX 8M Plus. This clock can be used to drive the RTC in the i.MX 8M Plus. The PCA9450C outputs a clock continuously unless it is in OFF mode. This feature allows the i.MX 8M Plus to use a high-precision, built-in RTC, eliminating the need for an external RTC.



6.2 I2C level translator

The PCA9450C is equipped with a level translator for I2C. 1.8 V, the voltage of the I2C interface of the i.MX 8M Plus, can be passed through this I2C level translator to enable communication with peripheral devices with 3.3 V/5 V I2C interfaces.



In the example shown in [Figure 8](#), SCLL and SDAL on the low-voltage side are connected to BUCK5 = 1.8 V, and SCLH and SDAH on the high-voltage side are connected to BUCK4 = 3.3 V. The integrated IC level translator in the PCA9450C allows the i.MX 8M Plus to communicate with peripherals with a 3.3 V or 5 V IC interface without the need for additional level translation circuitry.

7 References

1. PCA9450 data sheet: <https://www.nxp.com/docs/en/data-sheet/PCA9450.pdf>
2. PCA9450 application note: <https://www.nxp.com/docs/en/application-note/AN12840.pdf>
3. PCA9450-EVK evaluation board, including Gerber files, schematics, and GUI software: <https://www.nxp.com/PCA9450-EVK>
4. 8MPLUSLPD4-EVK (i.MX 8M Plus with PCA9450C and LPDDR4): <https://www.nxp.com:/8MPLUSLPD4-EVK>

8 Revision history

Table 4. Revision history

Document ID	Release date	Description
AN14246 v.1.0	1 July 2024	• Initial version

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	i.MX 8M Plus and Peripherals Power Supply Table5	Tab. 3.	Regulator state transition table by operating mode 9
Tab. 2.	State transition table for VSYS pin and major pins9	Tab. 4.	Revision history 12

Figures

Fig. 1.	PCA9450C internal block diagram 2	Fig. 5.	Power Up/Down Sequence 10
Fig. 2.	PCA9450C block diagram4	Fig. 6.	STANDBY mode transition 11
Fig. 3.	i.MX 8M Plus and peripheral device power connection diagram6	Fig. 7.	32.768 kHz crystal oscillator driver connection example 12
Fig. 4.	Connection diagrams by DDR memory type 7	Fig. 8.	I2C level translator connection example 12

Contents

1 Overview 2

1.1 Features 2

2 Block diagram 3

3 Power supply table and connection diagram 5

3.1 i.MX 8M Plus and peripheral device power supply table 5

3.2 i.MX 8M Plus and peripheral device power connection diagram 5

4 Connection by DDR memory type 7

5 Operation mode Transition 7

5.1 Operating mode 7

5.1.1 OFF mode 7

5.1.2 READY mode 8

5.1.3 SNVS mode 8

5.1.4 PWRUP mode 8

5.1.5 RUN mode 8

5.1.6 STANDBY mode 8

5.1.7 PWRDN mode 8

5.2 Operating mode transition table 8

5.2.1 State transition table for VSYS terminals and major terminals 8

5.2.2 Regulator state transition table by mode of operation 9

5.3 Power Up/Down sequence 9

5.3.1 Power Up sequence 10

5.3.2 Power Down sequence 10

5.4 STANDBY mode transition 11

6 System function blocks 11

6.1 32.768 kHz crystal oscillator driver 11

6.2 I2C level translator 12

7 References 12

8 Revision history 12

Legal information 13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.