AN13937

BTS6403C Evaluation Board Application Note

Rev. 1.1 — 15 April 2024 **Application note**

1 Introduction

This application note focusses on the BTS6403C Evaluation board, the application diagram, board layout, bill of materials and control signals are described. Also some typical measurement graphs are shown, even under Digital Pre-Distortion (DPD) conditions.

Refer to the datasheet for the detailed RF performance of the BTS6403C.

The Customer Evaluation Kit contains the following items:

- BTS6403C EVB
- 5 loose samples

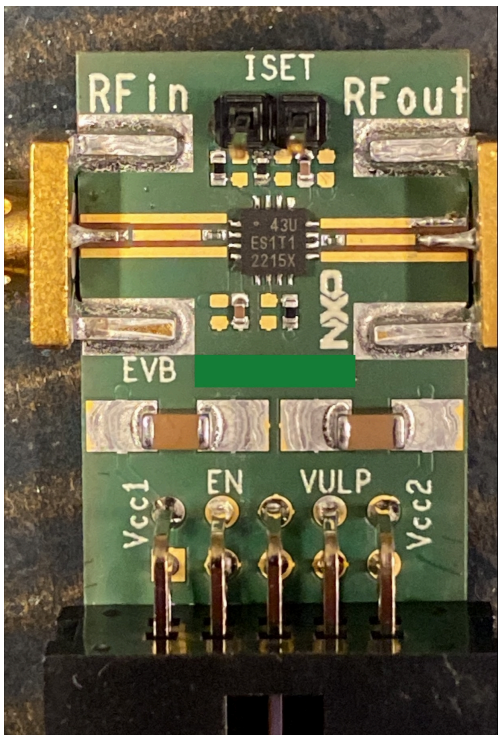


Figure 1. BTS6403C customer evaluation board (EVB). VULP is for internal test purpose only.

2 Ordering information

Table 1. Ordering information

Description	Part name	Ordering 12NC
BTS6403C Customer Evaluation Kit	OM1717/BTS6403C	9354 543 29598

3 Product description

The BTS6403C is a wideband, high linearity pre-driver amplifier for 5G massive MIMO infrastructure applications, with fast on-off switching to support TDD systems. The BTS6403C is designed to operate between 4.4 GHz and 5 GHz. The BTS6403C It is housed in a 3 mm × 3 mm × 0.85 mm 16 terminal HVQFN16 package.

The BTS6403C key features and benefits are listed below.

- High saturated output power $P_{o(sat)}$ = 28 dBm
- High power-gain Gp = 35.5 dB
- High linearity performance ACLR = -42 dBc
- Unconditionally stable
- Fast switching to support TDD systems
- 5 V single supply, quiescent current 100 mA
- Small 16-terminal leadless package 3 mm × 3 mm × 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1

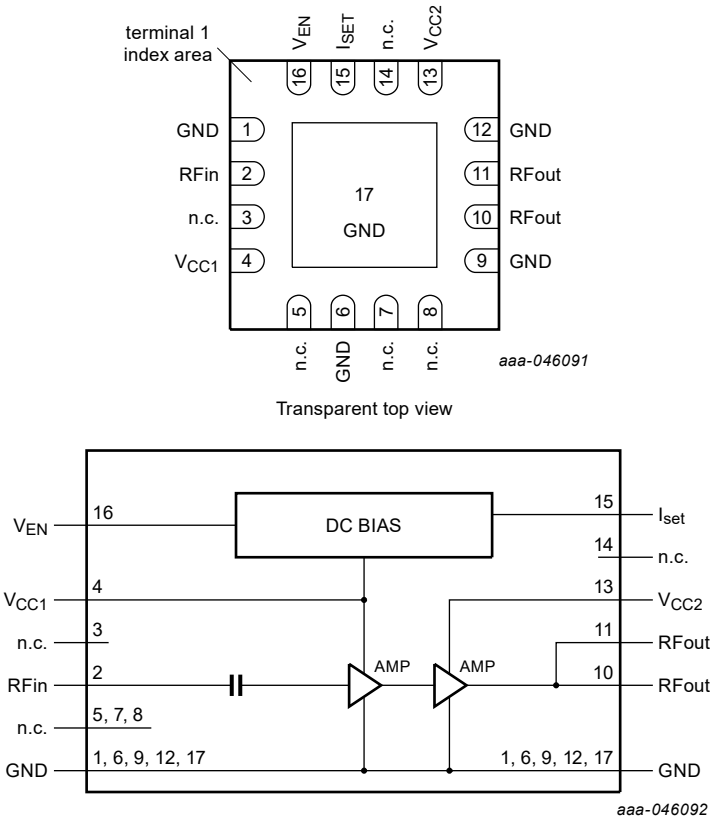


Figure 2. BTS6403C pin out and functional diagram

4 Application information

4.1 Application circuit

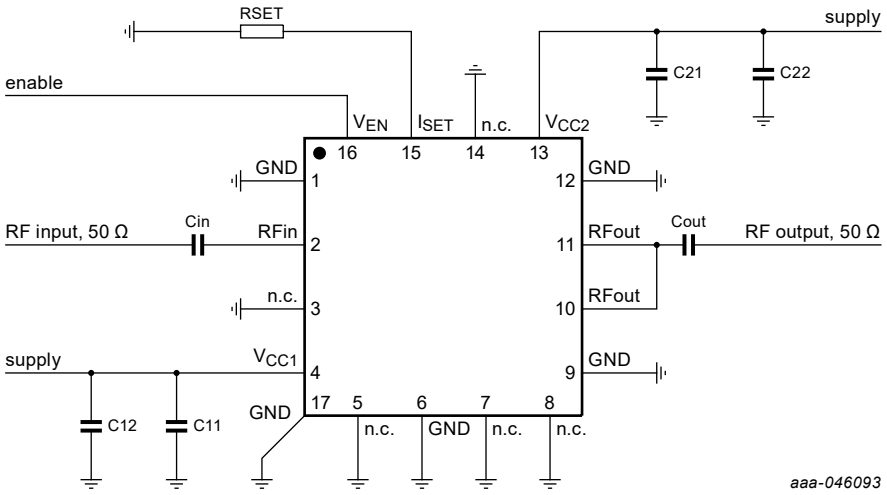


Figure 3. BTS6403C Application schematic

Table 2. List of components

Component	Description	Value	Remarks
Cin	capacitor	18pF	For DC blocking
Cout	capacitor	3.9pF	For DC blocking
C11, and C21	capacitor	10nF	Must be close (<10 mm) to the IC
C12, and C22	capacitor	10uF	Depending on low frequency impedance of regulator applied
RSET	Resistor	10 kΩ	If lower value is applied, a stability check is required

Ven protection:

When there are requirements for maximum currents in the control lines (under all possible conditions), apply a series resistor in the Ven line to limit the maximum current. High V_{en} current may happen when V_{cc} is low (or low impedance to GND) and V_{en} is high (not a normal operating condition).

When a series resistor is placed in the Ven line the maximum current is limited. This series resistor can be necessary when V_{en} is HIGH.

If V_{cc} is low impedance to ground and Ven rises above one forward diode voltage (ESD protection diode), the current in the V_{en} line is unlimited.

With 5kΩ series resistance the current at any condition is limited to few mA (depending on Ven value),but switching time is hardly affected.

5 Evaluation board

The BTS6403C evaluation board simplifies the RF evaluation of this pre driver. The evaluation board enables testing the RF performance of the device, in an isolated environment. To de-embed applied RF output connector and transmission line up to the DC blocking capacitor, de-embedding data is available on request.

The BTS6403C evaluation board is fabricated on a 26 mm x 48 mm x 1 mm thick 4 layer PCB. The 0.254 mm top layer uses R4350B or TU-862 for optimal RF performance. The board is fully assembled according to the schematic shown below. The board is supplied with two SMA connectors to connect input and output to the RF test equipment.

5.1 Evaluation circuit

The application board circuit diagram that is implemented on the EVB is shown in Figure 4.

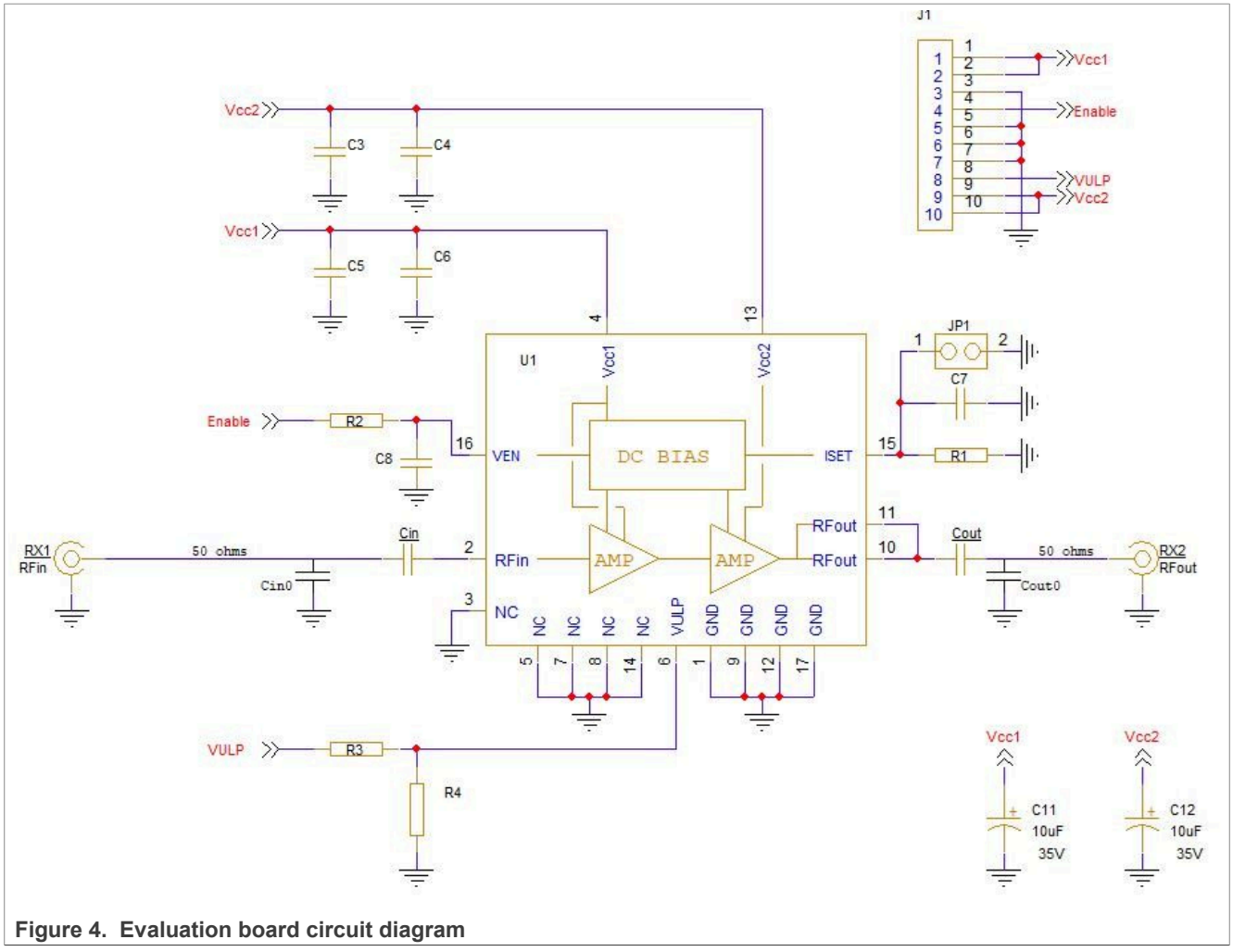


Figure 4. Evaluation board circuit diagram

5.1.1 Explanation of the connections

•V_{CC1}: supply for the first amplifiers stages and biasing / regulator circuitry. Apply at least 10 nF decoupling close to the pin and a larger value capacitor further away (depending on the supply low frequency impedance).

•V_{CC2}: supply for the last amplifier stage. Apply at least 10 nF decoupling close to the pin and a larger value capacitor further away (depending on the supply low frequency impedance).

•I_{set}: used to adjust the quiescent current. The adjustment is inversed proportional to the resistor value. NXP recommends keeping R1 10 kΩ to avoid potential stability issues

•RF_{out} (two pins): DC coupled RF output (parallel pins), DC blocking capacitor required.

•V_{ulp}: for internal test purposes only, connect to ground.

•RF_{in}: AC coupled RF input, however due to internal ESD protection circuitry the amount of DC allowed to this input is limited. For this reason NXP recommends applying an additional DC blocking capacitor

•V_{en}: logic input. In the NXP EVB a series SMD placeholder, populated with 0 R (zero Ω), is available. When the V_{en} is logic high and V_{CC} is low impedance to ground (none standard “use case”) current flows into this V_{en} pin. To limit the current, a 5.6 kΩ resistor can be used in position R2.

5.2 PCB Layout information and component selection

- A good PCB layout is an essential part of an RF circuit design. The evaluation board of the BTS6403C can serve as a guideline for laying out a board using the BTS6403C.
- The evaluation board uses micro strip coplanar ground structures for controlled impedance lines for the high frequency input and output.
- C6, C11 and C4, C12 decoupling capacitors respectively bypass V_{CC1} and V_{CC2}. C4 and C6 preferably should be located as close as possible < 1 mm to the device, to avoid AC leakage via the bias lines. For long bias lines, it may be necessary to add decoupling capacitors along the line further away from the device
- In this report, as well as in the data sheet the value of C1 and C2 are stated as 18 pF and 3.9pF. The values of C1 and C2 are critical for power on/off settling time. When the value for those capacitors is increased significantly the switching speed is affected.
- Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The layout and component placement of the BTS6403C evaluation board is given in Figure 6
- Resistor R2 in the Venable Line on EVB is chosen to be 0 Ohm, for current limitations in the system application it is recommended to use a resister value of 2kΩ to 5kΩ.
- Although the RF input port is DC free a blocking capacitor is recommended in order to protect the pin for DC voltages above one forward diode voltage (ESD protection diodes)

5.2.1 Evaluation board layout

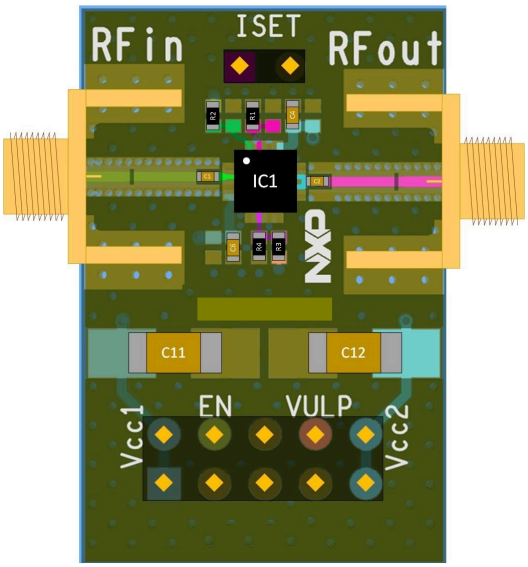


Figure 5. BTS6403C evaluation board layout and component placement

5.2.2 Bill of materials

Table 3. Evaluation board BOM

Gives the bill of materials as is used on the EVB

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
IC1	BTS6403C				
PCB	28x17x1mm				TU-862
C1	Capacitor	0201	18pF	Various	DC block RF-in
C2	Capacitor	0201	3.9pF	Various	DC block RF-out
C4,C6	Capacitor	0402	10nF	Various	RF decoupling
C11,C12	Capacitor	1206	10uF	Various	Optional
R1	Resistor	0402	10kOhm	Various	Quiescent current setting
R2,R3.R4	Resistor	0402	0 Ohm	Various	Bridge
RC1,RC2	SMA RF connector			Johnson, End launch SMA 142-0701-841	RF connections
JP1	Jumper			Molex, PCB header,	
J1	DC header			Molex, PCB header, straight, 2 row 5 way	DC connections

5.2.3 PCB stack and recommended footprint

The PCB material used to implement the pre-driver circuit is a 0.3 mm TU-862 low loss printed circuit board which is merged to a 0.7 mm FR4 layer for mechanical stiffness. See Figure 6 The official drawing of the recommended footprint can be found via following link SOT758-1.pdf. When micro strip coplanar PCB technology is used it is recommended to use at least 12 ground-via holes of 300um in the ground plane under the device, this is also used on the EVBs as shown in Figure 7.

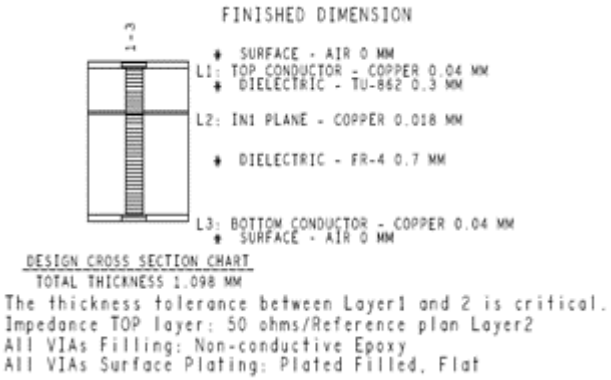


Figure 6. PCB stack information

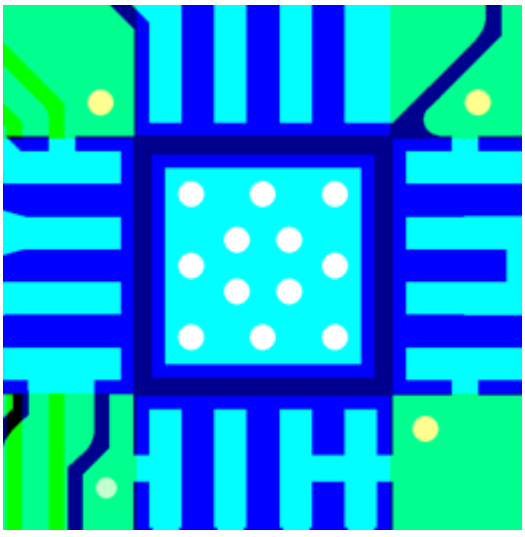


Figure 7. PCB footprint information

6 Evaluating the BTS6403C

All RF performance results given in the next chapters are referenced to the SMA connectors on the evaluation board. In the data sheet characteristics, board connectors and PCB tracks are de-embedded up-to the product input and output DC blocking capacitors.

The typical device performance given in the data sheet is characterized on the evaluation board equal to the board described in this application note. The BTS6403C mounted on the evaluation board in the customer evaluation kit is industrially tested on the most important RF parameters. Like Gain, Noise Figure, IP3o, and PL(1dB).

All connection names are clearly displayed on the board. See Figure 1.

Note: *Because of the standard layout, the board is used for different products. Not all connections are used, like VULP*

6.1 Typical results.

For detailed performance of the BTS6403C we refer to the device product datasheet.

V_{CC} = 5.0 V; T_{amb} = 25 °C; input 50 Ω and output 50 Ω; RSET = 10 kΩ. unless otherwise specified. All RF parameters have been characterized on the evaluation board described in this application note

Table 4. Typical results

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm, f = 4.4 GHz	-	122	150	mA
		ON state, quiescent	-	100	125	mA
		OFF state	-	1.2	2.5	mA
G_p	power gain	ON state, t_{amb} = -40 °C to 115 °C [1]				
		f = 4.4 GHz	33	35.5	38	dB
		f = 5 GHz	31.5	34	36.5	dB
		OFF state	-	-49.0	-	dB
$P_{L(1dB)}$	output power at1 dB gain compression	f = 4.4 GHz	-	27.5	-	dBm
		f = 5 GHz	-	26.5	-	dBm
$IP3_o$	output third-order intercept point	2-tone; tone spacing = 100 MHz; P_o = 15 dBm, f = 4.4 GHz	-	33	-	dBm

[1] These values are guaranteed via final test at t_{amb}

6.2 Graphs

6.2.1 S-parameters

The measured S-parameters are given in Figure 8, Figure 9, Figure 10, Figure 11, For the measurements, a typical BTS6403C EVB is used. All the S-parameter measurements have been carried out using the setup Figure 21

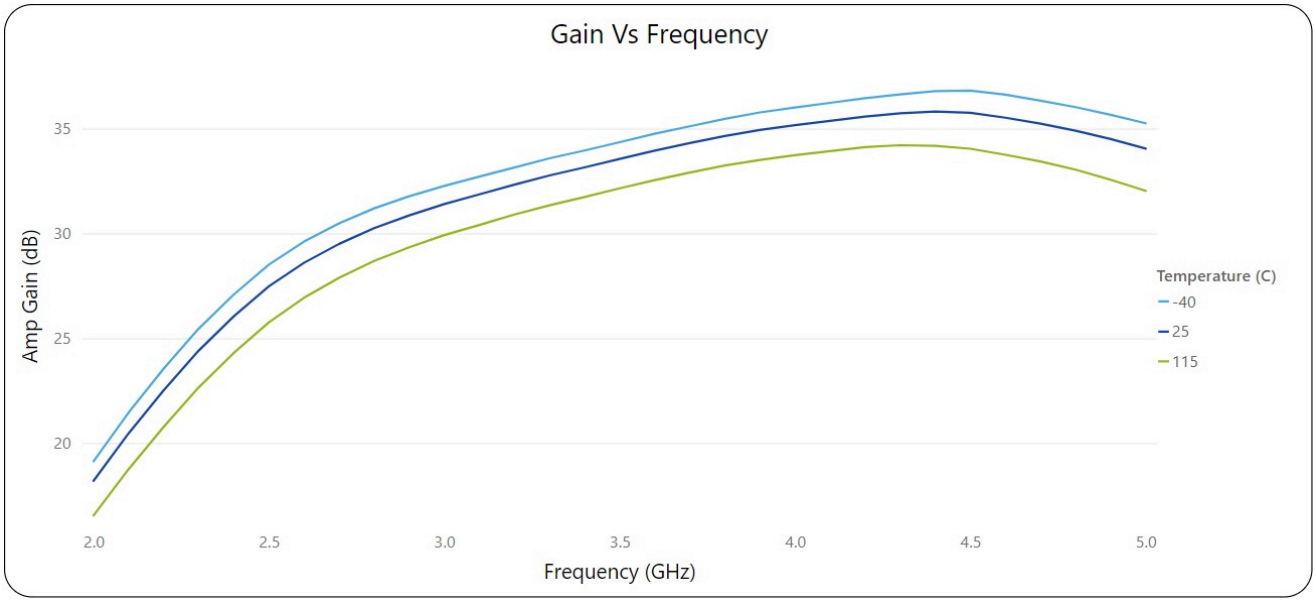


Figure 8. BTS6403C S_{21} Gain versus frequency over temperature (typical values). V_{cc} = 5 V, Pin = -30 dBm

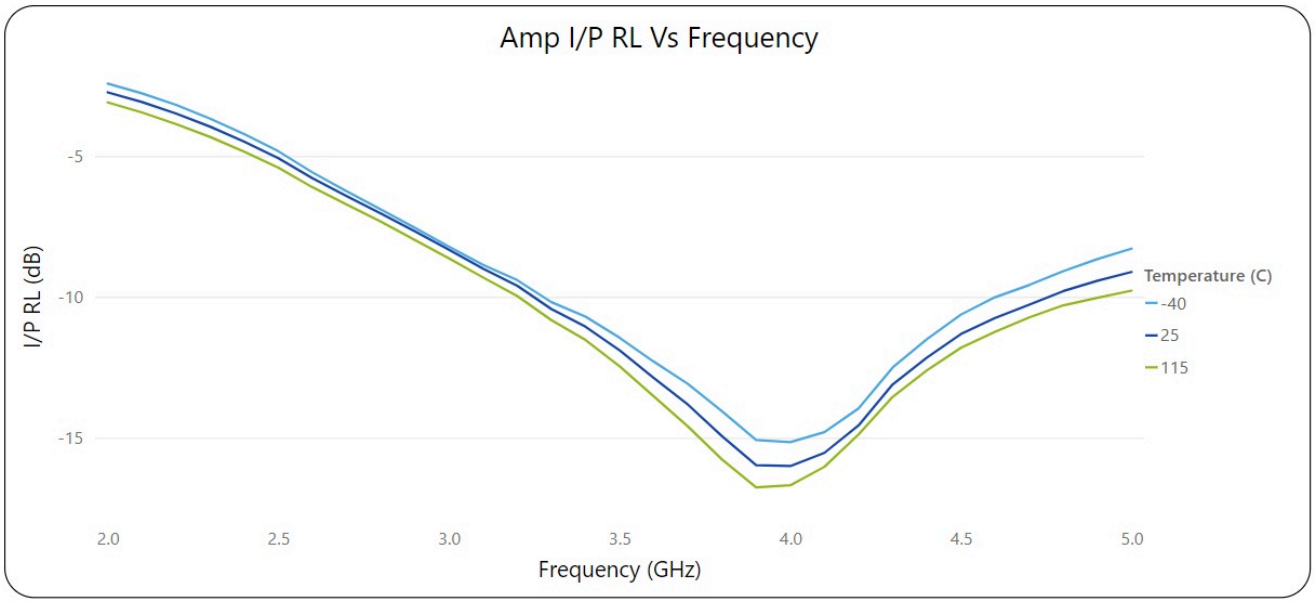


Figure 9. BTS6403C S_{11} versus frequency over temperature (typical values), V_{cc} = 5 V, Pin = -30 dBm

6.2.1 S-parameters...*continued*

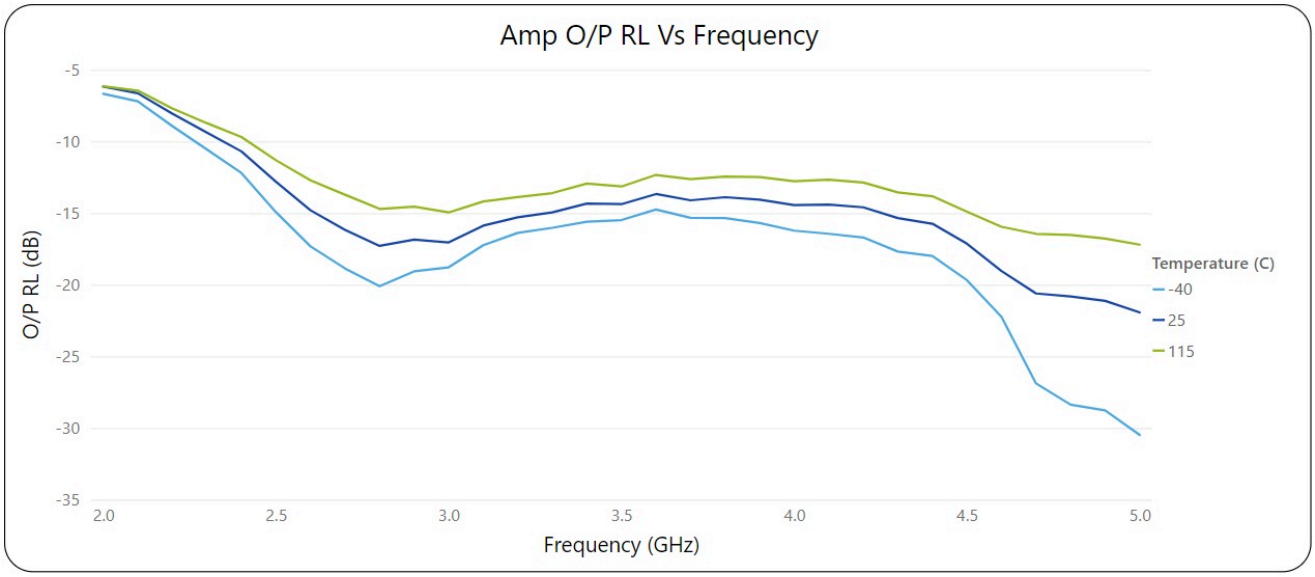


Figure 10. BTS6403C S_{22} versus frequency over temperature (typical values). V_{cc} = 5 V, Pin = -30 dBm

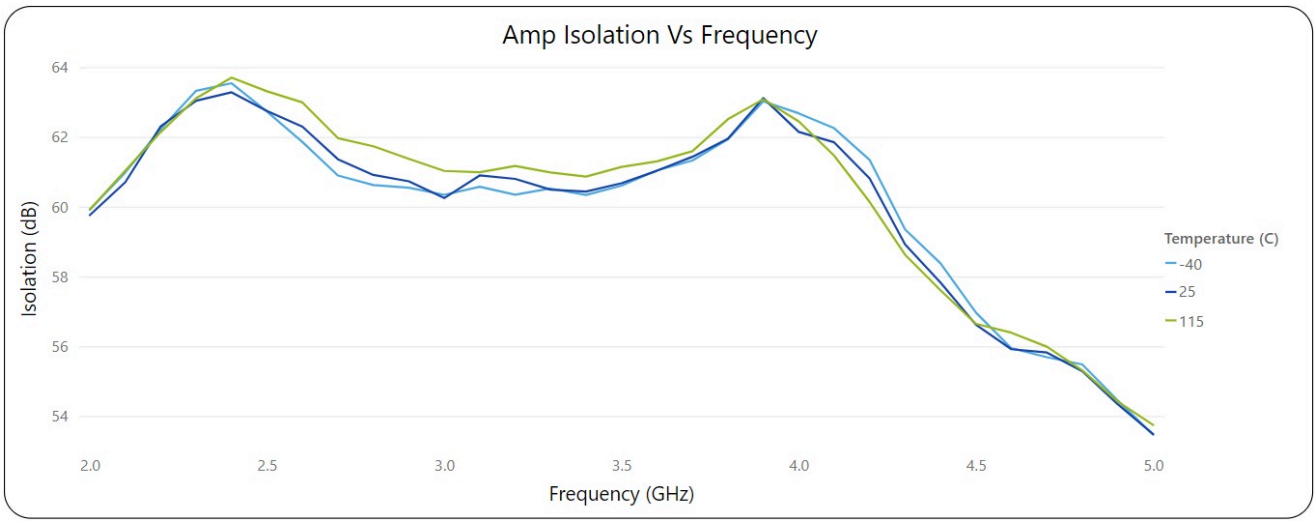


Figure 11. BTS6403C S_{12} versus frequency over temperature (typical values). V_{cc} = 5 V, Pin = -30 dBm

6.2.2 K-factor

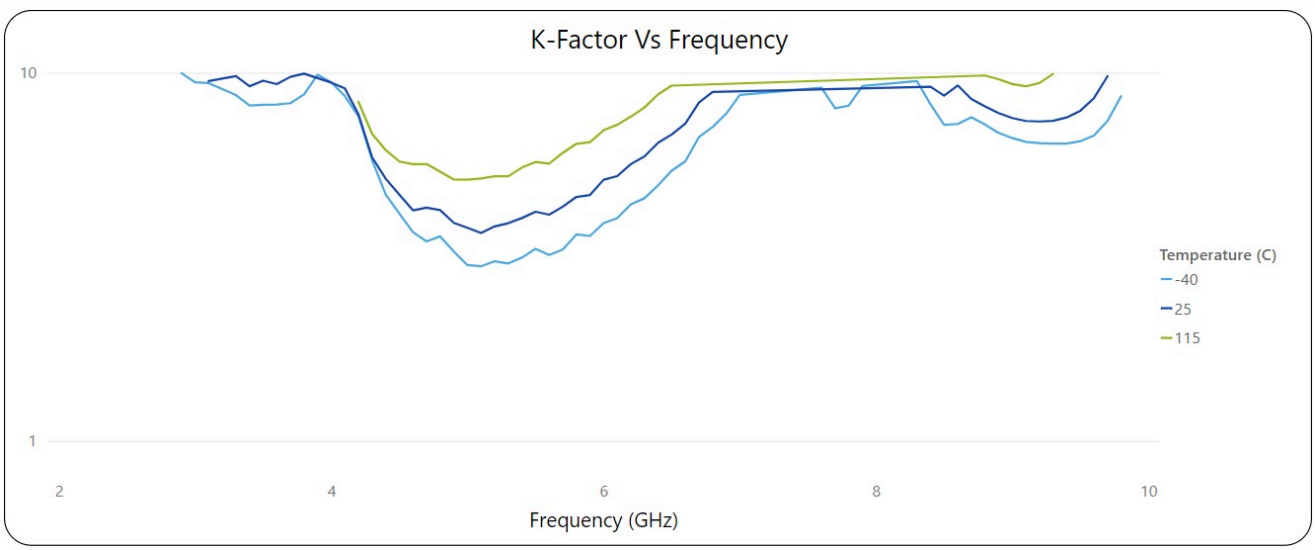


Figure 12. BTS6403C K - factor (typical value). V_{cc} = 5 V

6.2.3 Pout and Gain versus Pi

Curves have been measured using the set up shown in Fig 12.

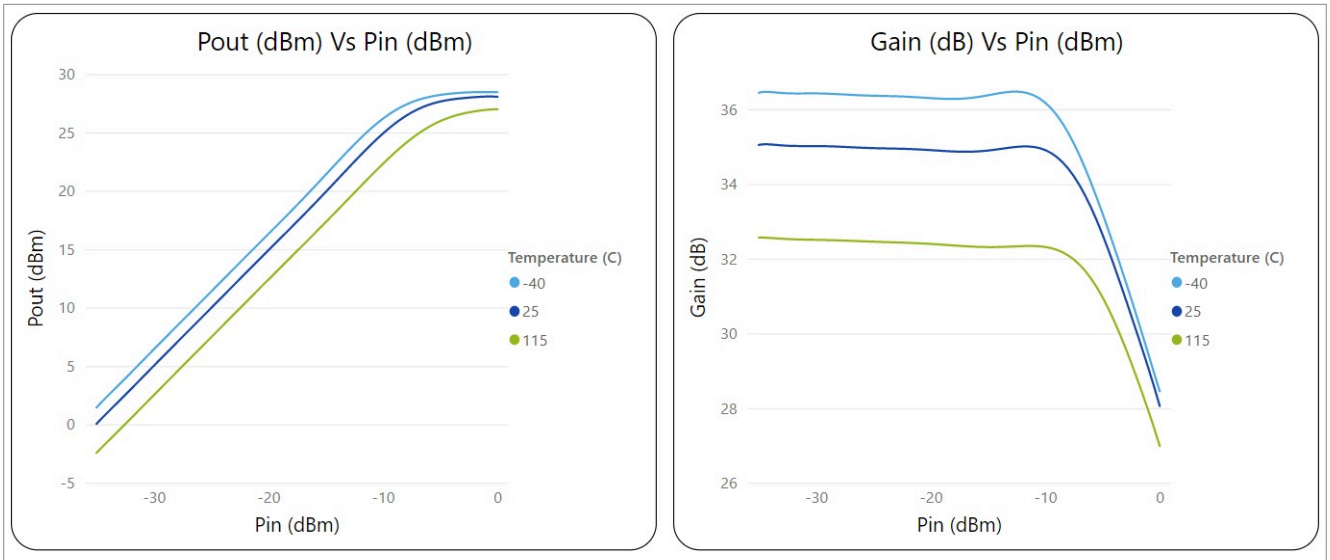


Figure 13. BTS6403C Pout and Gain versus input power (typical values). V_{cc} = 5 V

6.2.4 OP1dB and OP3dB (Saturated output power)

The saturated output power been measured using the set up shown in Figure 21.a

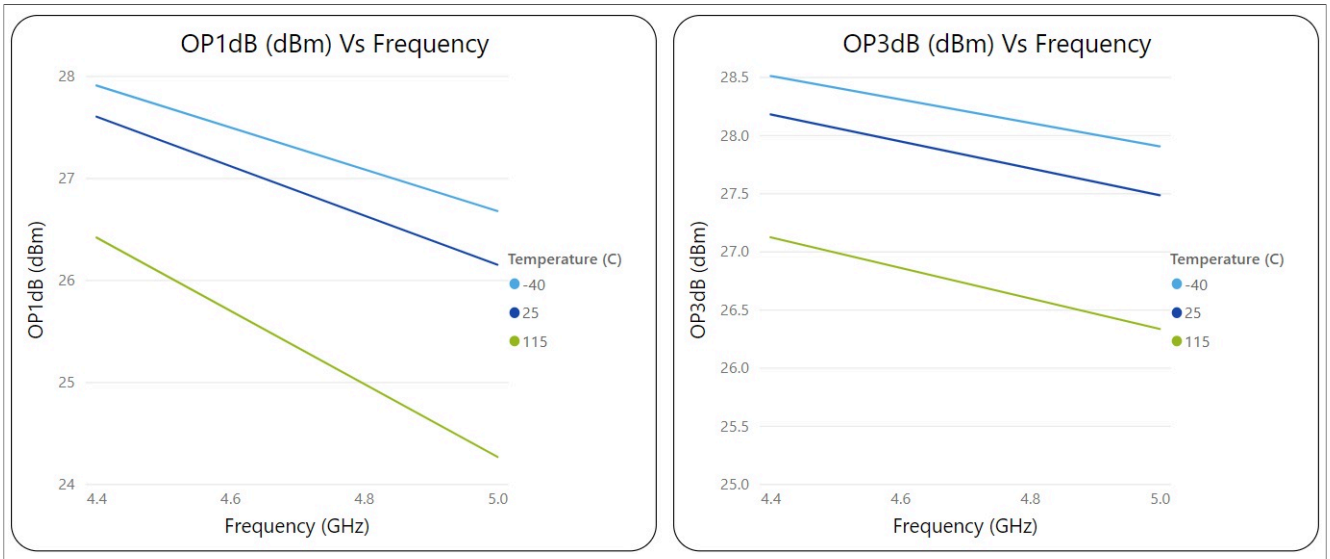


Figure 14. BTS6403C OP1dB vs Frequency (typical values). V_{cc} = 5 V

6.2.5 Noise Figure

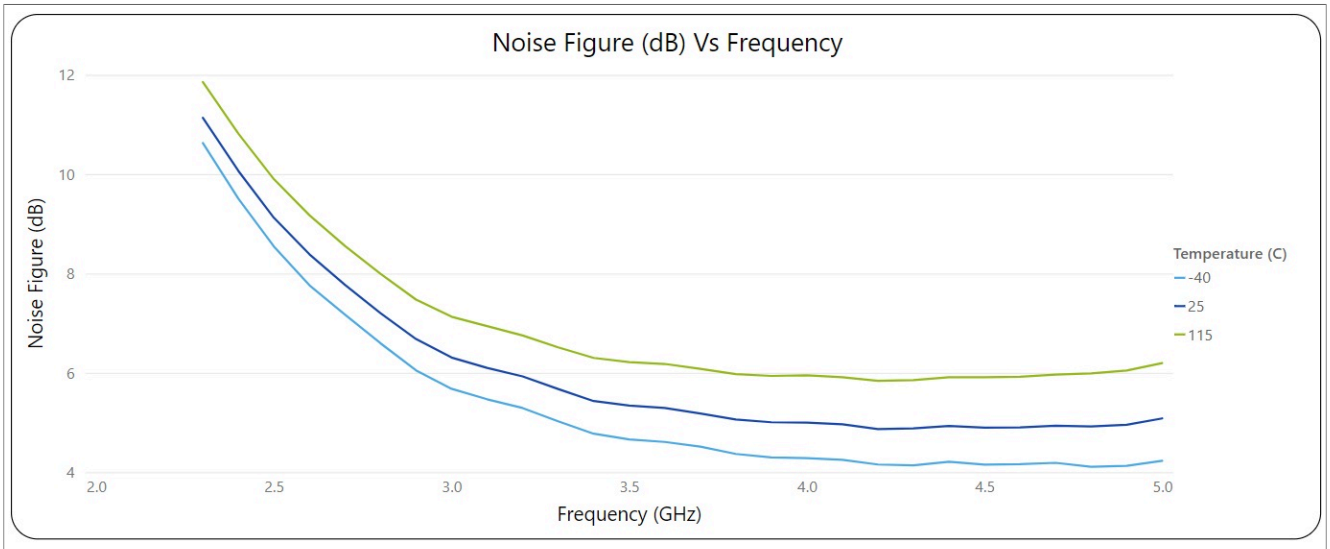


Figure 15. BTS6403C Noise figure vs Frequency (typical values). V_{cc} = 5 V

6.2.6 Third order intercept point

OIP3 is being measured using a setup like given in Figure 21.

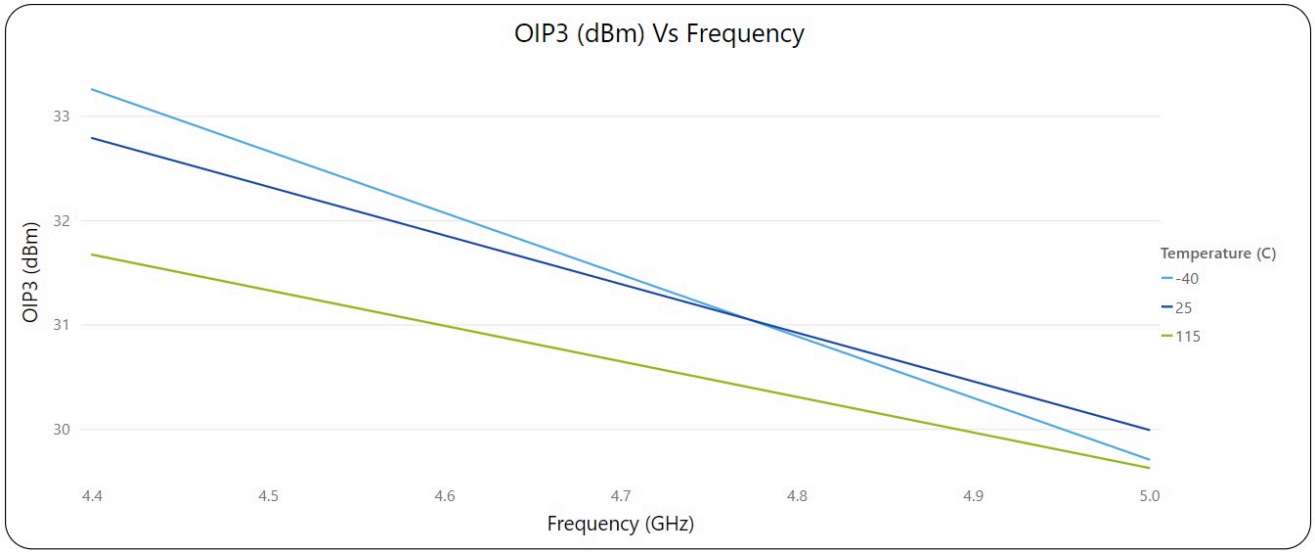


Figure 16. BTS6403C $IP3_o$ at 100 MHz spacing, output tone power ~15 dBm.

6.2.7 ACLR under DPD

In the TX line ups for MIMO Digital Pre-Distortion (DPD) is applied to linearize the final stages to gain efficiency while improving on linearity related parameters.

To what extend the BTS6403C needs to be pre-distorted depends on factors like applied output power and crest factor at the BTS6403C. As an example the BTS6403C was measured on ALCR at given Pout with and without applying DPD to note the differences.

The DPD engine is 62 coefficients internal developed platform, based on Volterra series.

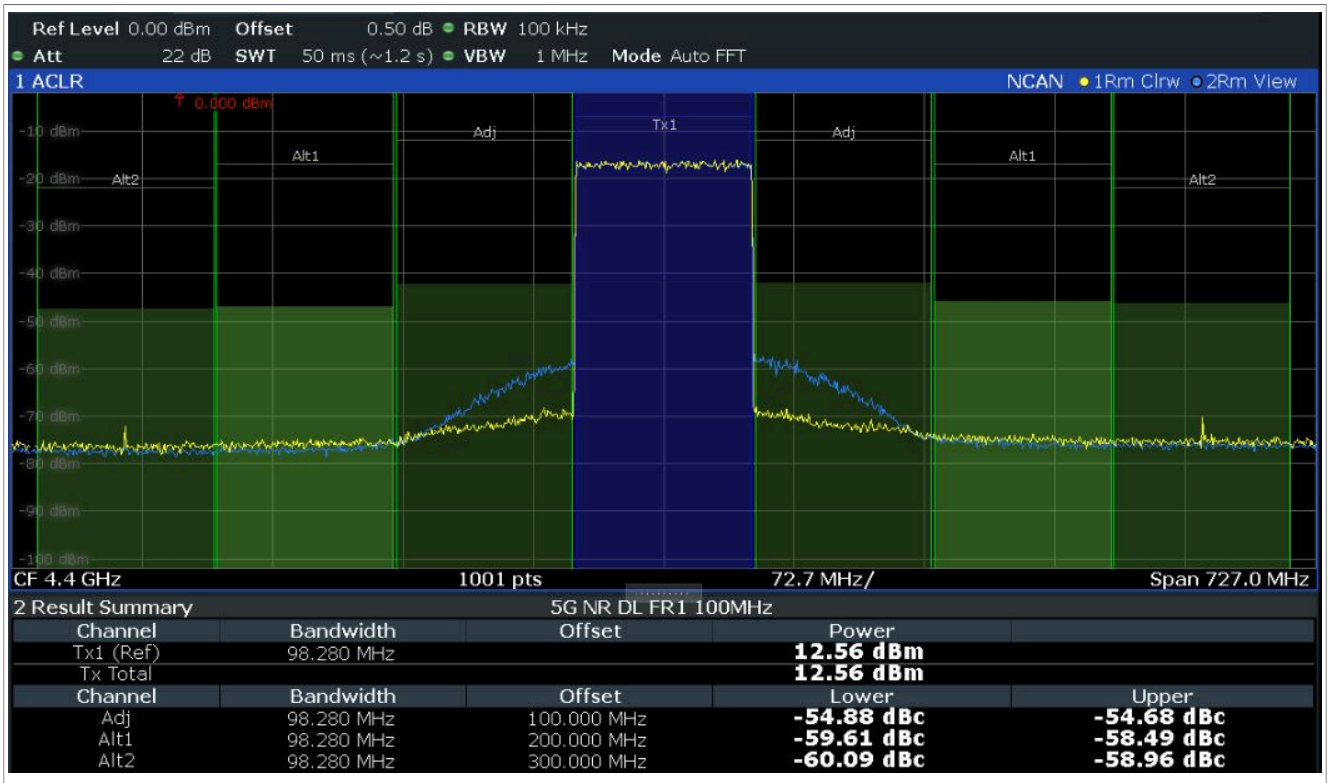


Figure 17. BTS6403C ACLR DPD vs none-DPD at 4.4 GHz center frequency and P_{out} 12.5 dBm, CF 10 dB.

6.2.7 ACLR under DPD...*continued*

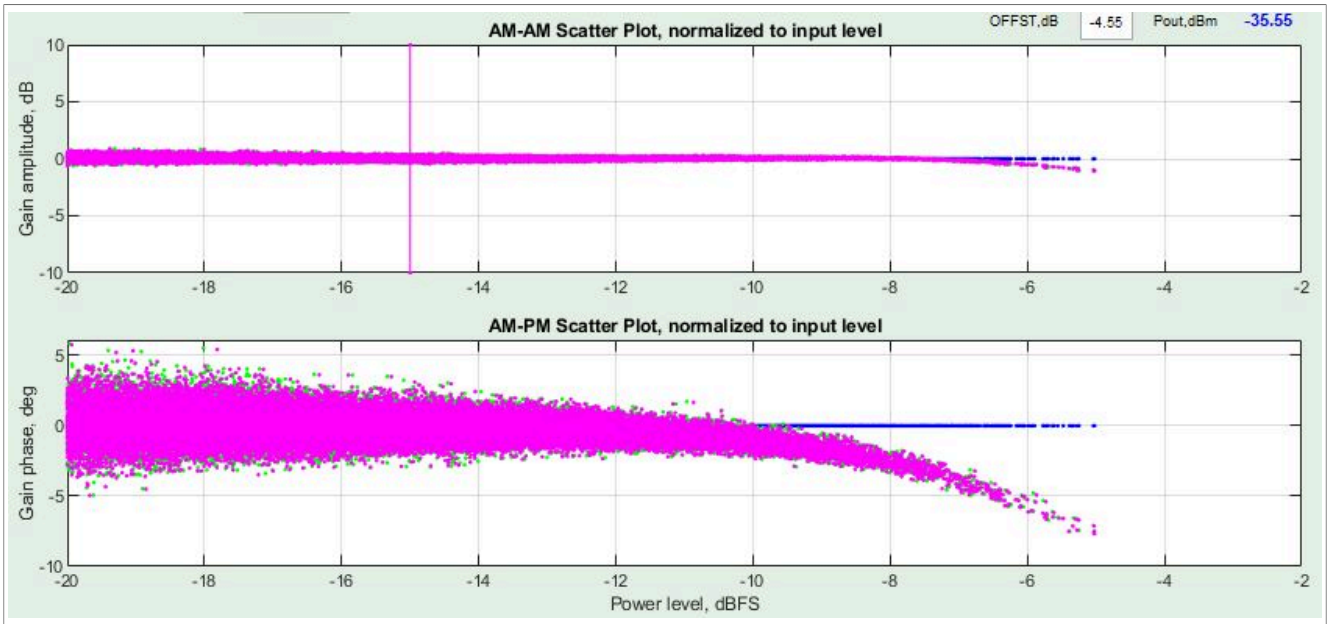


Figure 18. BTS6403C AMAM and AMPM at 4.4 GHz for 18 dBm peak Po = average 18 dBm, PAR 10 dB

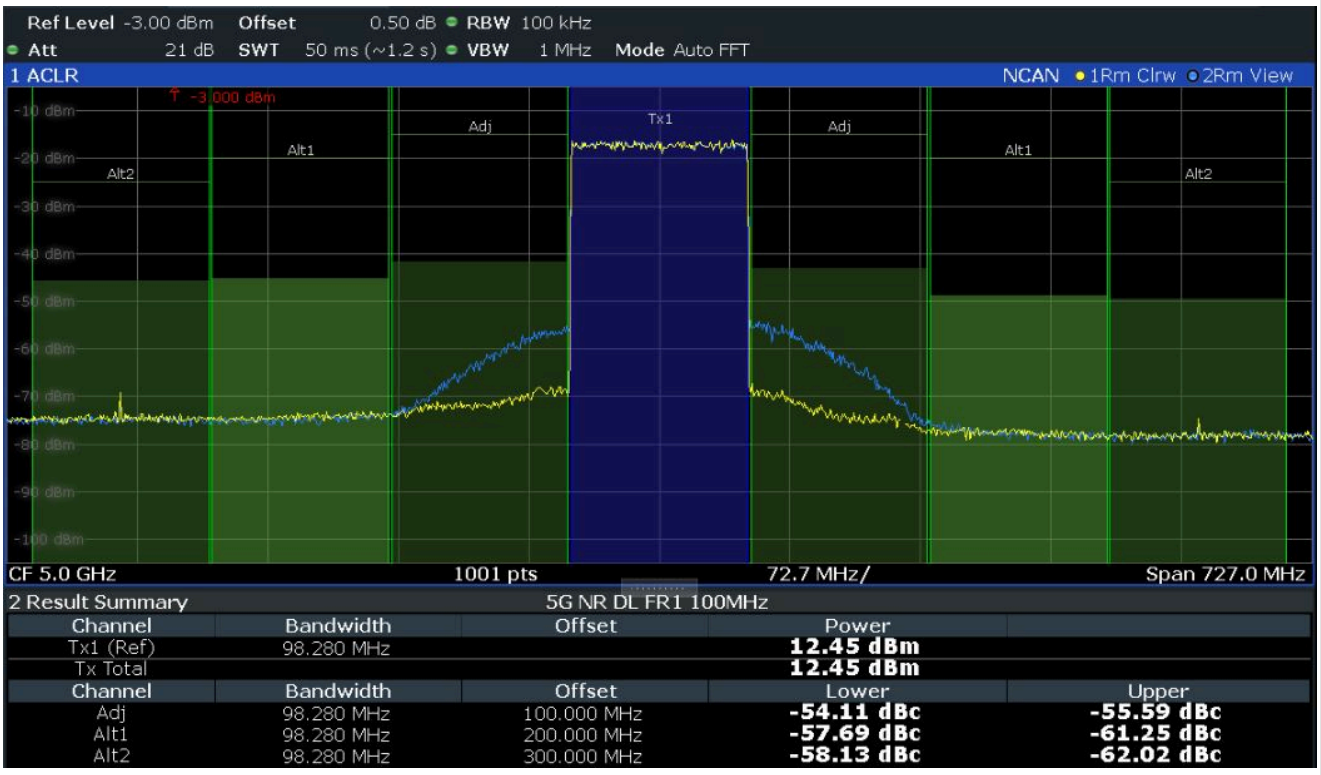


Figure 19. BTS6403C ACLR DPD vs none-DPD at 5.0 GHz center frequency and P_{out} 12.5 dBm, CF 10 dB.

6.2.7 ACLR under DPD...*continued*

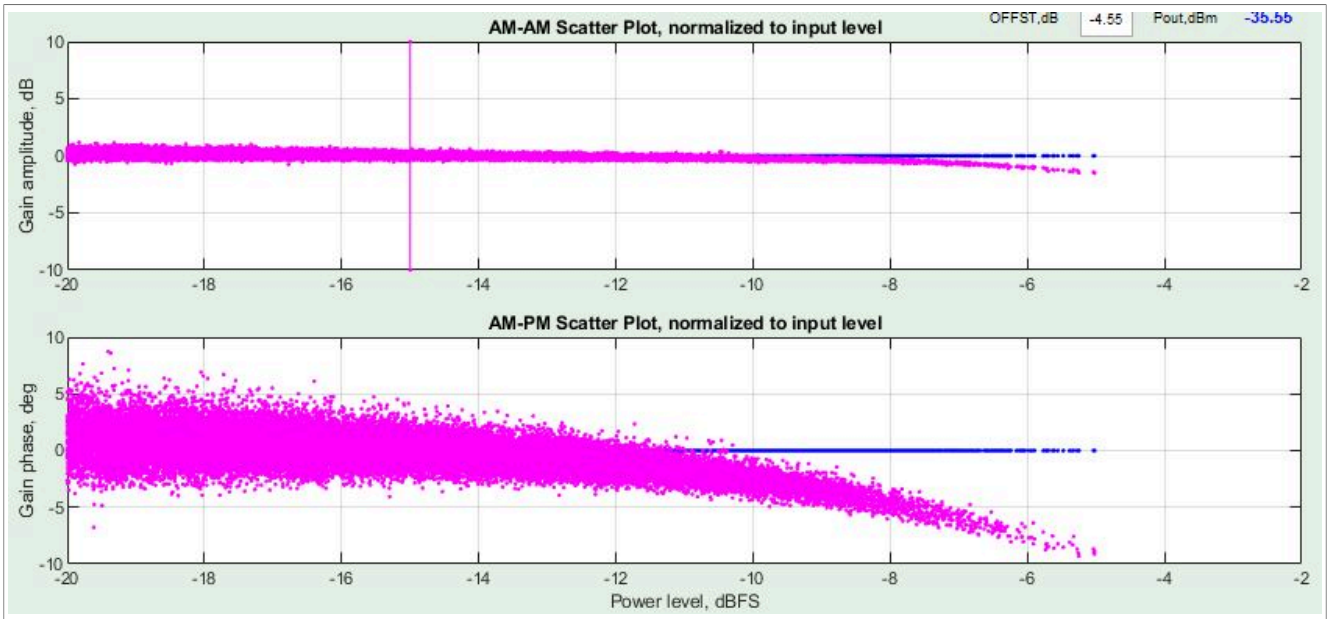


Figure 20. BTS6403C AMAM and AMPM at 5.0 GHz, P_{out} average 18 dBm, PAR 10 dB

6.3 Required Equipment

For the BTS6403C evaluation the following equipment is needed as a base-line:

- 1 DC power supply 5V, 200 mA (V_{cc1} and V_{cc2})
- 1 DC power supply 1.8V, 5mA (V_{en}) or a pulse generator in case pulsed measurements are required
- A suitable Balun
- A network analyzer for S-parameter measurements, and P1dB measurements (in case the NA is a 4 port version two ports could be defined as differential outputs, in such case the Balun is not required for Spa measurements and the differential mode related parameters can be evaluated)
- 2 RF generators up to 12 GHz + combiner for IP3 measurements
- A spectrum analyzer with NF option for IP3 and Noise figure measurements.
- High Quality RF cables with SMA/3.5mm RF connectors.
- DC currents meters.

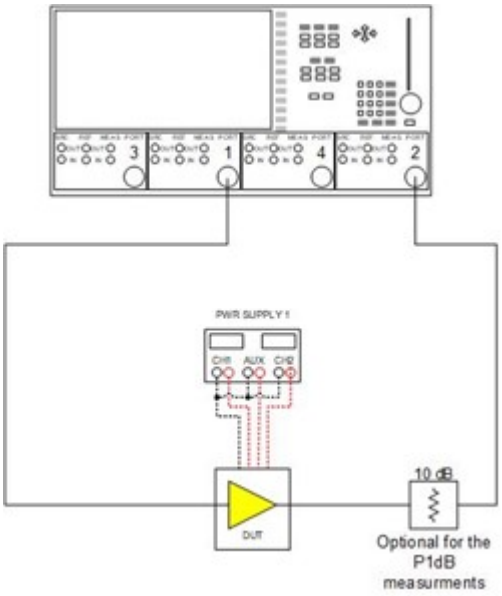
V_{cc1} and V_{cc2} are usually combined and fed to the 5V PSU. After switching on the power supply, the BTS6403C comes up in the quiescent current 1.8V enable voltage also needs to be applied preferable the supply start-up sequence is as follows.

First switch on V_{cc1} second V_{cc2} and third V_{en}. But this is not critical..

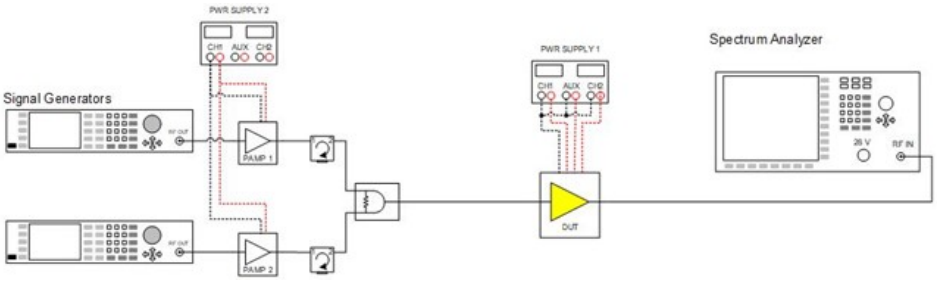
The typical current at 5V supply is 78 mA, in power-down mode V_{en}(0V) - 0.5 mA.

6.4 Connection and setup

1. Connect the EVB to a calibrated network analyzer see Fig 11, we advise the following settings for S-parameter measurements:
   a. Port power -30dBm
   b. IF Bandwidth 100Hz
2. The network analyzer can also be used for the 1 dB gain compression evaluation, for this we advise the following NWA setting
   a. Port 1 power sweep -30dBm up to -10dBm
   b. Port 2 20dB attenuation on the receiver port b2.
   c. IF Bandwidth 100Hz.
3. Gain and 1dB gain compression data can also be determined using an RF generator and spectrum analyzer.
4. Turn on the DC power supplies and it should read typical Icc = mA.
5. Nonlinear distortion measurements IP3 can be performed with a set-up like is depicted in Figure 21.The following settings are recommended to perform the IP3 evaluation.
   a. -20dBm for each fundamental tone.
   b. RBW and VBW of the spectrum analyzer 100 Hz
   c. Tone spacing 100 MHz



a: S-parameter and 1dB gain compression setup.



b: Third order intercept point measurement set-up

Figure 21. Evaluation measurement setups

7 EMC information

CAUTION

This product has not undergone formal EMC assessment. It is the responsibility of the user to ensure that any finished assembly complies with applicable regulations on EMC interference. EMC testing, and other testing requirements for CE is the responsibility of the user.

8 Revision history

Table 5. Revision history

Document ID	Release date	Description
AN13937 Rev. 1.1	15 April 2024	• Updated Legal information and brought to current standard
AN13937 Rev. 1.0	11 May 2023	• Initial release of application note

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Contents

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