AN13707

Hardware Design Guidelines for LPC553x/LPC55S3x Microcontrollers

Rev. 2 — 23 May 2024

Application note

Document information

Information	Content
Keywords	Hardware design guidelines, LPC553x
Abstract	This document guides hardware engineers to design and test their LPC553x/S3x controller-based designs. The document provides information about board layout recommendations and design checklists.

1   Introduction

This document helps the hardware engineers to design and test their LPC553x/S3x controller-based designs. The document provides information about board layout recommendations and design checklists to ensure first-pass success and avoid any board bring-up problems.

This document only focuses on LPC553x/S3x.

Note: LPC553x/S3x devices are not pin-to-pin compatible with other LPC55 series devices.

This guide is released with the relevant device-specific hardware documentation such as data sheets, reference manuals, and application notes available on www.nxp.com.

2   LPC553x/S3x family comparison

All LPC553x/S3x family is based on the Arm Cortex-M33 core, with PowerQuad Accelerator, enhanced timer, and analog features to support motor control applications. The 'S' in the middle of the part name means that this part provides more security features, such as TrustZone Support.

Table 1. LPC553x/S3x family core features

Type number	Flash/ KB	Total RAM/KB	CAN FD	USB	GPIO	Flex SPI	ADC channel	DAC outputs	Internal DAC	Comparator	Tamper pins	OP Amp	CRC/1/2/3	DMIC
LPC5536JBD100	256	128	Y	FS	66	Y	23	2	1	4	4	3	Y	Y
LPC5536JBD64	256	128	Y	-	39	Y	13	1	2	4	2	3	Y	y
LPC5534JBD100	128	96	Y	FS	66	Y	23	2	1	4	4	3	Y	Y
LPC5534JBD64	128	96	Y	-	39	Y	12	1	2	4	2	3	Y	y
LPC5534JHI48	128	96	Y	-	32	Y	10	-	1	4	2	3	Y	Y
LPC5536JHI48	256	128	Y	-	32	Y	10	-	1	4	2	3	Y	Y

Note: The last 18 pages (9 KB) are reserved on the 256 KB flash devices for the Protected Flash Region (PFR), resulting in 247 KB of internal flash memory for the user.

For more information, refer to the latest version of the Datasheet and Reference Manual (RM) from www.nxp.com.

3   Power supply

This section gives details of the power supply for the LPC553x/S3x series.

3.1 Introduction

LPC553x/S3x series require a single operating voltage supply on MCU VDD_MAIN/VDD_MAIN_PWR pins (1.8 V to 3.6 V), two main I/O supplies on VDDIO_1 (1.8 V to 3.6 V) and VDDIO_2 (1.08 V to 3.6 V) pins, and a separate Battery Supply (V_{BAT}) on VBAT pin (1.71 V to 3.6 V).

LPC553x/S3x internal core's voltage is supplied by an internal DC-DC regulator or selectable LDO such that the DC-DC converter can be bypassed.

Refer to *Using the DC-DC and LDO Features on the LPC553x/LPC55S3x Family* (document [AN13528](AN13528)) for details.
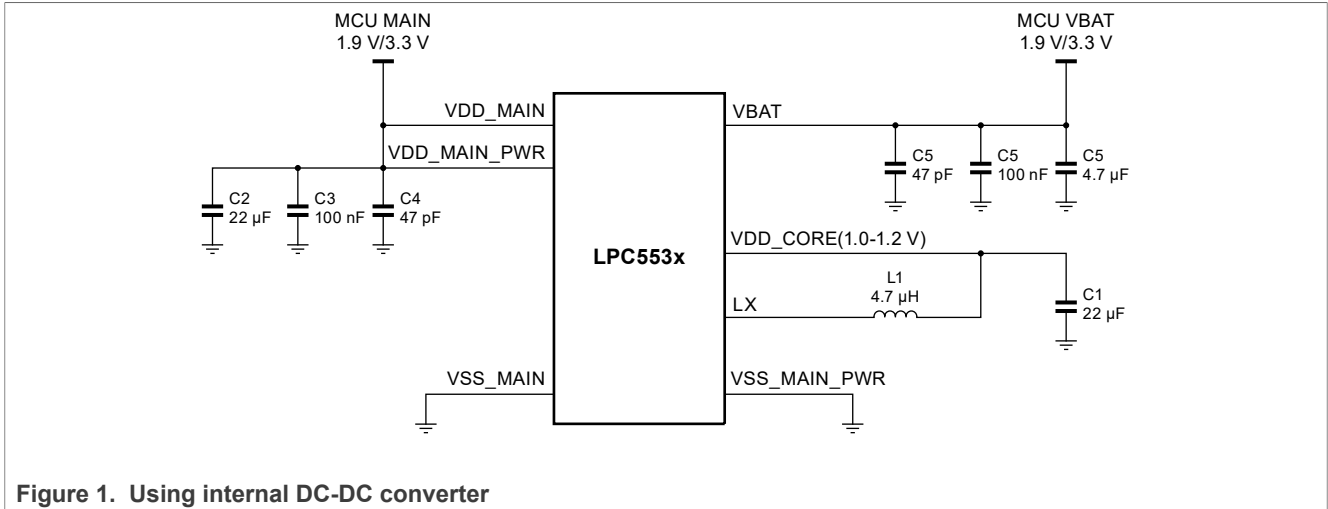
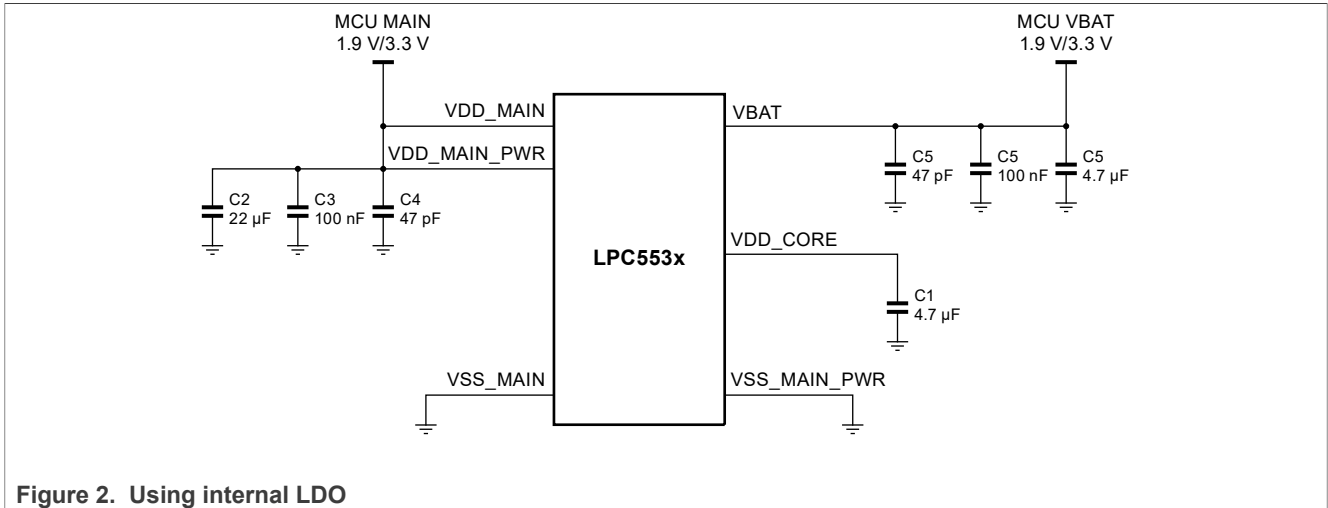**Figure 1. Using internal DC-DC converter**

Figure 2. Using internal LDO

3.2 Two I/O power supplies

LPC553x/S3x have two I/O supplies, VDDIO_1 and VDDIO_2.

VDDIO_1 supports 1.8 V to 3.6 V.

VDDIO_2 supports 1.08 V to 3.6 V.

Table 2. LPC553x/S3x power supply for pins

Pin	GPIO pins
VDDIO_1	PIO0_1 PIO0_7 to PIO0_8 PIO0_10 to PIO0_12 PIO0_15 to PIO0_17 PIO0_23 PIO0_27 PIO0_31 PIO1_0 PIO1_5 to PIO1_10 PIO1_19 to PIO1_24

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Table 2. LPC553x/S3x power supply for pins...*continued*

Pin	GPIO pins
	PIO2_0 to PIO2_1 RESETN
VDDIO_2	P0_0 P0_2 to P0_6 P0_9 P0_13 to P0_14 P0_18 to P0_22 P0_24 to P0_26 P0_28 to P0_30 P1_1 to P1_4 P1_11 to P1_18 P1_25 to P1_31

3.3 Separate VBAT

LPC553x/S3x's VBAT pin requires a separate power supply with the range from 1.71 V to 3.6 V.

3.4 Bulk and decoupling capacitors

The effectiveness of the bulk and the decoupling capacitors depends on the optimum placement and connection type. The bulk capacitors are used for a local power supply to the power pin, near the decoupling capacitors, and as close as possible to the assigned reference voltage pin. Decoupling capacitors make the current loop between supply, MCU, and reference ground as short as possible to reduce high-frequency transients and noises. Therefore, all decoupling capacitors must be placed as close as possible to the devices power supply pins. In two-layer and multilayer PCBs, the ground side of the decoupling capacitor must have a via to the pad, which goes directly down to the internal ground plane. The route distance between the capacitors to the power plane must be as short as possible.
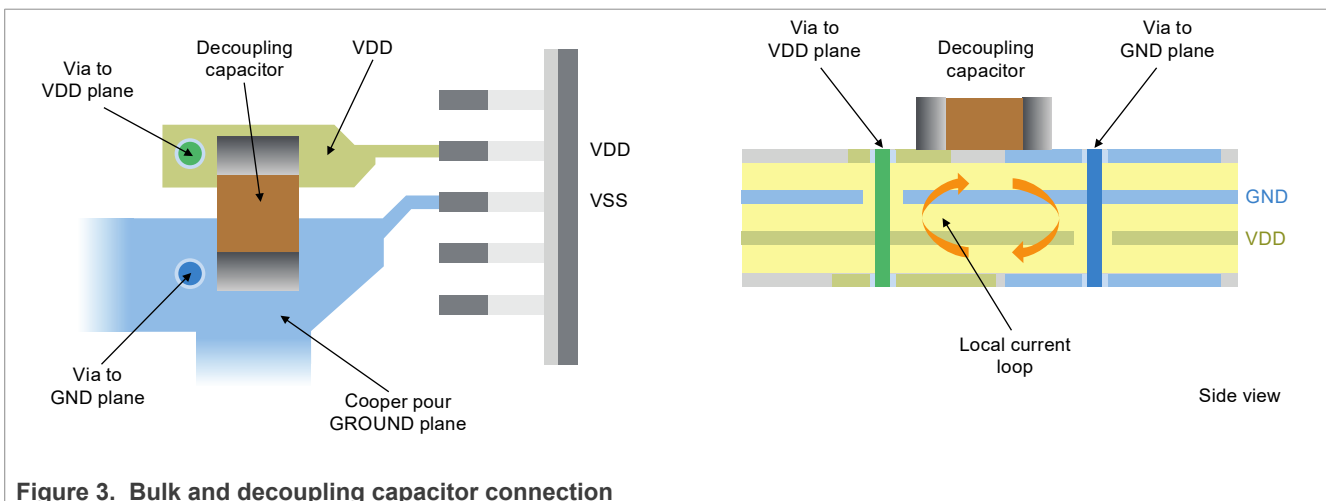

Figure 3. Bulk and decoupling capacitor connection

4 Clock circuitry

This section gives details of the clock circuitry.

4.1 Introduction

The LPC553x/S3x has the following clock sources:

- Internal Free Running Oscillator (FRO). This oscillator provides a selectable 96 MHz output, and a 12 MHz output (divided down from the selected higher frequency) that can be used as a system clock. The FRO is trimmed to +/- 1 % accuracy over the entire voltage and 0 °C to 85 °C. The FRO is trimmed to +/- 2 % accuracy over the entire voltage and -40 °C to 105 °C.
- 32 kHz Internal Free Running Oscillator FRO. The FRO is trimmed to +/- 2 % accuracy over the entire voltage and temperature range.
- Internal low-power oscillator (FRO 1 MHz) trimmed to +/- 15 % accuracy over the entire voltage and temperature range.
- Crystal oscillator with an operating frequency of 12 MHz to 32 MHz, and an option for the external clock input (bypass mode) for clock frequencies of up to 25 MHz.
- Crystal oscillator with 32.768 kHz operating frequency.
- PLL0 and PLL1 allow CPU operation up to the maximum CPU rate without the need for a high-frequency external clock. PLL0 and PLL1 can run from the internal FRO 12 MHz output the external oscillator, internal FRO 1 MHz output, or the 32.768 kHz RTC oscillator.
- Clock output function with a divider to monitor internal clocks.
- Frequency measurement unit for measuring the frequency of any on-chip or off-chip clock signal.
- Each crystal oscillator has one embedded capacitor bank, where each can be used as an integrated load capacitor for the crystal oscillators. Using APIs, the capacitor banks on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) leading to conserving board space and reducing costs.

Note: *For external crystal oscillator and RTC oscillator, LPC553x/S3x have a capacitor bank feature. It means that the stabilizing capacitors can be unsoldered on both 32 kHz and 16 MHz XTAL. We also suggest the user keep the two stabilizing capacitors as "DNP/Do Not Populate" on PCB.*

4.2 Capacitor bank

Each crystal oscillator has one embedded capacitor bank, which is always enabled, and its capacitance can be adjusted in certain range (IEC equivalent capacitive load: 6 - 10 pF). The capacitor bank can be used as integrated load capacitors for the crystal oscillators. It helps save external load capacitors of the crystal and therefore the system BOM cost.

For the capacitor bank usage, refer to *Understanding Cap Bank in LPC55(S)xx* (document AN13057).

4.3 Crystal oscillator

The crystal oscillator has one embedded capacitor bank that can be used as an integrated load capacitor for the crystal oscillators. The capacitor bank on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) between 6 to 10 pF (IEC equivalent). Simple APIs can be used to configure the capacitor bank based on the crystal Capacitive Load (CL) and measured PCB parasitic capacitances on the XIN and XOUT pins.

In the crystal oscillator circuit, only the crystal (XTAL) must be connected while the CX1 and CX2 on XTAL32M_P and XTAL32M_N pins can optionally be connected. No additional capacitance needs to be added to the PCB when the computation of the required Capacitance Load is less than 20 pF (10 pF equivalent IEC), When the aforesaid load is greater than 20 pF (10 pF equivalent IEC), additional capacitance is required. (see Figure 4.) For more information, refer to the Cap Bank API chapter in the *LPC553x/S3x Reference Manual* (document LPC553xRM).

In bypass mode, an external clock (maximum frequency of up to 25 MHz) can also be connected to XTAL32M_P if XTAL32M_N is left open. The external [0 – VH] square signal can be applied on the XTAL32M_P pin **from 0 V to 850 mV**.
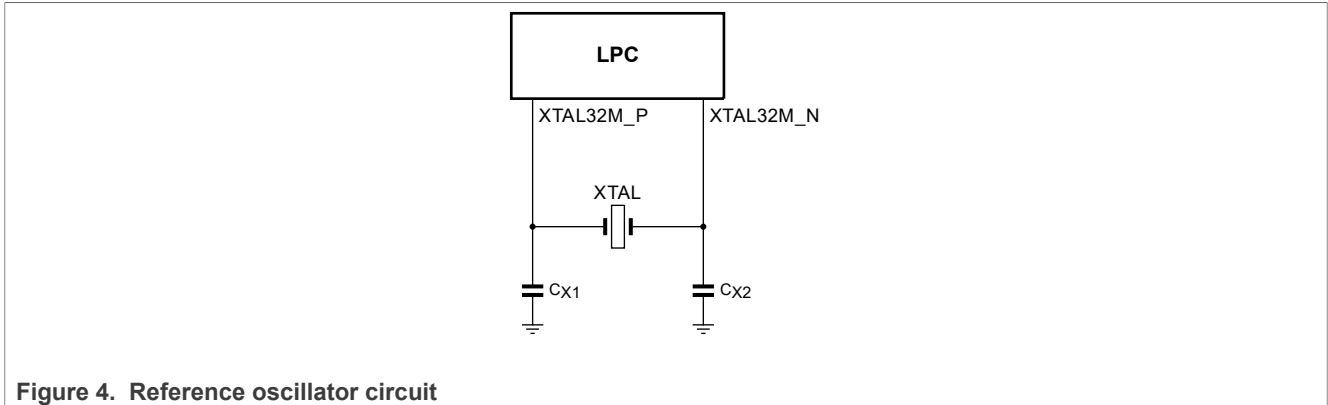
Figure 4. Reference oscillator circuit

Table 3. Components of the oscillator circuit

Symbol	Description
XTAL	Quartz Crystal / Ceramic Resonator
CX1	Stabilizing Capacitor
CX2	Stabilizing Capacitor

For best results, it is critical to select a matching crystal for the on-chip oscillator. Load Capacitance (CL), Series Resistance (RS), and Drive Level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic} + C_{capbank})$$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTAL32M_P and XTAL32M_N pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

$C_{capbank}$ – Cap Bank

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influence the optimal values of external load capacitors. Therefore, it is recommended to fine-tune the values of external load capacitors on the actual hardware board to get an accurate clock frequency. For fine-tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation. The load capacitors are dependent on the specifications of the crystal and the board capacitance. It is recommended to have the crystal manufacturer evaluate the crystal on the PCB.

4.3.1 Crystal Printed Circuit Board (PCB) design guidelines

• Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
• The length of traces in the oscillation circuit must be as short as possible and must not cross other signal lines.
• Ensure that the load capacitors CX1 and CX2, in case of third overtone crystal usage, have a common ground plane.
• Loops must be made as small as possible to minimize the noise coupled through the PCB and to keep the parasitic as small as possible.
• Lay out the ground (GND) pattern under the crystal unit.

• Do not lay out other signal lines under the crystal unit for multi-layered PCB.

4.4 RTC oscillator

The crystal oscillator has an embedded capacitor bank that can be used as an integrated load capacitor for the crystal oscillators. The capacitor banks on each crystal pin can tune the frequency for crystals with a Capacitive Load (CL) between 6 to 10 pF (IEC equivalent). Simple APIs can be used to configure the capacitor banks based on the crystal Capacitive Load (CL) and measured PCB parasitic capacitances on the XIN and XOUT pins.

In the RTC crystal oscillator circuit, only the 32.768 kHz crystal (XTAL) needs to be connected while the CX1 and CX2 on XTAL32K_P and XTAL32K_N pins (See Figure 5.) can also optionally be connected. No additional capacitance needs to be added to the PCB when the computation of the required capacitance load is less than 20 pF (10 pF equivalent IEC). When this load is greater than 20 pF (10 pF equivalent IEC), additional capacitance is required. Refer to the Cap Bank API chapter in the *LPC553x/S3x Reference Manual* (document LPC553xRM).

In bypass mode, an external clock (maximum frequency of up to 100 kHz) can also be connected to XTAL32K_P if XTAL32K_N is left open. An external [0 – VH] square signal can be applied on the XTAL32K_P pin with 1.1 V +/-10 %.

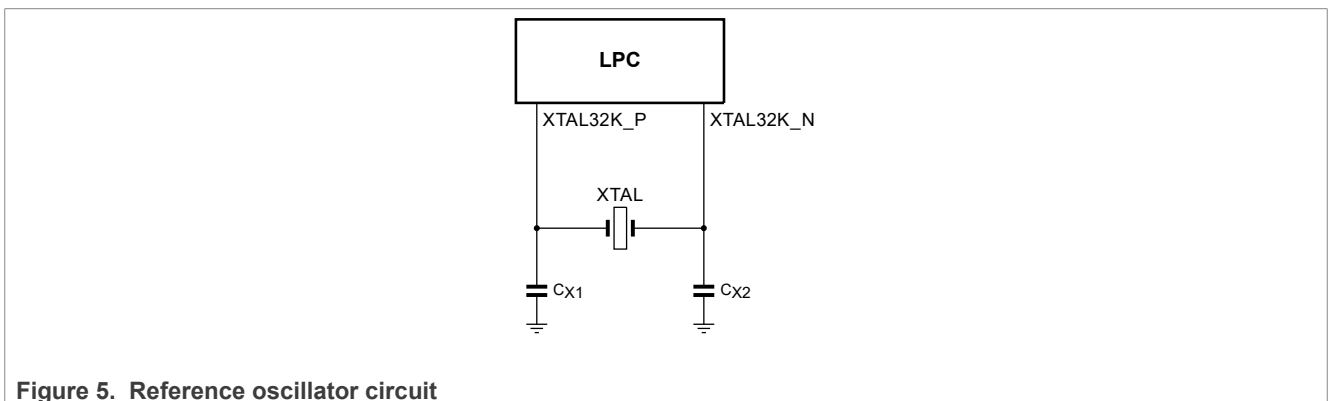An external **signal below 1.0 V or above 1.2 V cannot be applied**.

Figure 5. Reference oscillator circuit

For best results, it is critical to select a matching crystal for the on-chip oscillator. Load Capacitance (CL), Series Resistance (RS), and Drive Level (DL) are important parameters to consider while choosing the crystal. After selecting the proper crystal, the external load capacitor C_{X1} and C_{X2} values can also be generally determined by the following expression:

$C_{X1} = C_{X2} = 2C_L - (C_{Pad} + C_{Parasitic} + C_{capbank})$

Where:

C_L - Crystal load capacitance

C_{Pad} - Pad capacitance of the XTAL32K_P and XTAL32K_N pins (~3 pF).

$C_{Parasitic}$ – Parasitic or stray capacitance of external circuit.

$C_{capbank}$ – Cap Bank

Although $C_{Parasitic}$ can be ignored in general, the actual board layout and placement of external components influences the optimal values of external load capacitors. Therefore, it is recommended to fine-tune the values of external load capacitors on the actual hardware board to get the accurate clock frequency. For fine-tuning, output the RTC Clock to one of the GPIOs and optimize the values of external load capacitors for minimum frequency deviation.

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4.4.1 RTC Printed Circuit Board (PCB) design guidelines

- Connect the crystal and external load capacitors on the PCB as close as possible to the oscillator input and output pins of the chip.
- The length of traces in the oscillation circuit must be as short as possible and must not cross other signal lines.
- Ensure that the load capacitors CX1, CX2, and CX3, in case of third overtone crystal usage, have a common ground plane.
- Loops must be made as small as possible to minimize the noise coupled through the PCB and to keep the parasitic as small as possible.
- Lay out the ground (GND) pattern under the crystal unit.
- Do not lay out other signal lines under the crystal unit for multi-layered PCB.

4.5 Common suggestions for the PCB layout of the oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to the analog-board layout rules, see Figure 6.

- Send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum value of CXTAL and CEXTAL capacitors. The data sheet includes recommendations for the tank capacitors CXTAL and CEXTAL. These values together with the expected PCB, pin, and stray capacitors values must be used as an initial point.
- The crystal or resonator oscillator is sensitive to stray capacitance and noise from other signals. It must be placed away from high-frequency devices and traces to avoid and reduce the capacitive coupling between the XTAL and EXTAL pins and their PCB traces.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (Oscillator to CEXTAL and CXTAL to Oscillator) must be kept as short and symmetric tracing as possible. Therefore, both the capacitor's ground connections must always be closer to the VSS pin using the copper-poured ground plane and there must be several vias to the internal ground layer in the PCB for efficient grounding.
- Connect the EXTAL and XTAL pins to the required oscillator components only, and not to any other devices.

The following figure shows the recommended placement and routing for the oscillator layout.
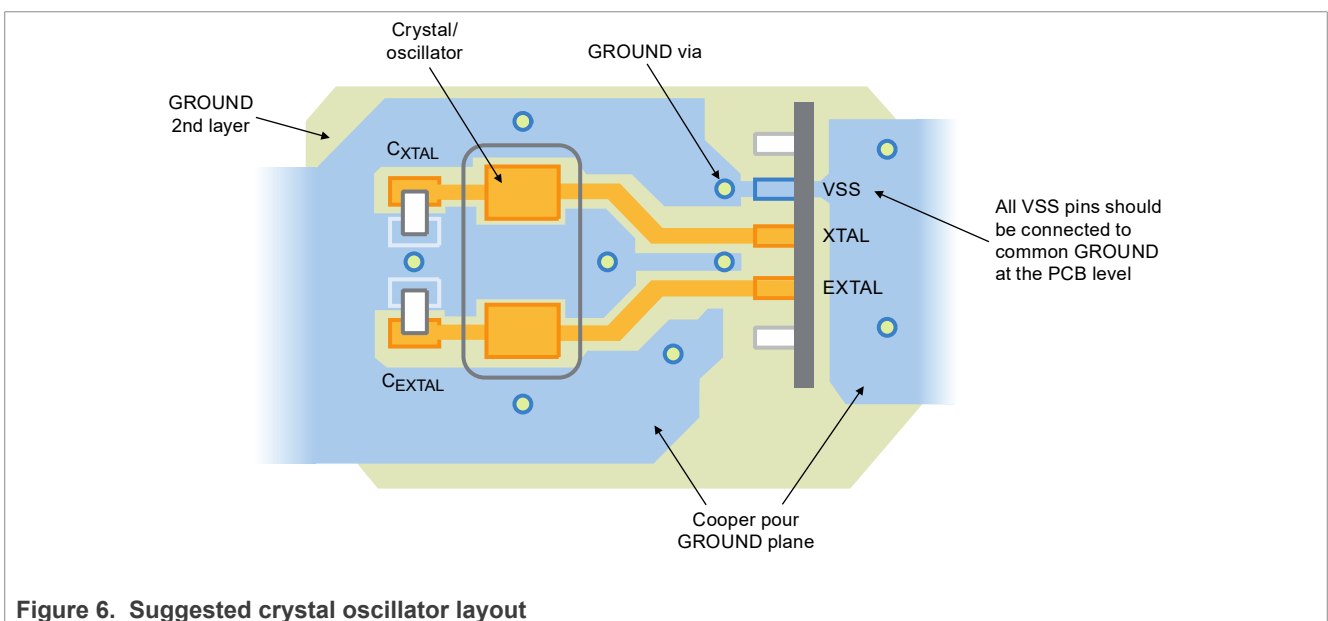

Figure 6. Suggested crystal oscillator layout

5   Boot mode configuration

This section gives information about boot mode selection and configuration.

5.1 Boot mode selection

The internal ROM memory is used to store the boot code called boot ROM. After a reset, the Arm processor starts its code execution from this memory. The boot ROM code is executed every time the part is powered-ON, is reset, or wakes up from a deep power-down mode of low-power modes.

Images can be stored either in the internal flash as the LPC553x/S3x has an internal flash for code and data storage or in the Serial NOR connected to the FLEXSPI controller. The code is then validated, and the boot ROM vectors to on-chip flash or the off-chip FLASH. Depending on the values of the CMPA bits, ISP pin, and the image header type definition, the bootloader decides whether to boot from the internal flash, off-chip flash, or run into ISP mode. The LPC553x/S3x reads the status of the ISP pins to determine the boot source. See Table 4.

Table 4. Boot mode and ISP download modes based on ISP pins

Boot mode	ISP1 (PIO0_7 pin)	ISP0 (PIO0_5 pin)	Description
Internal Flash boot	LOW	LOW	The LPC553x looks for a valid image from the internal flash; if there is no valid image, the LPC553x looks for a valid image in the recovery boot device if recovery boot is enabled (4:0, word 1 in CMPA) in CMPA. If it still fails, the LPC553x enters ISP boot mode based on DEFAULT_ISP_MODE bits.
ISP boot	LOW	HIGH	One of the serial interfaces (UART0, I2C1, HS_SPI, USB0-FS, CAN) is used to download the image from the host into the internal flash. The first valid probe message on USART, I2C, SPI, CAN, or USB locks in that interface
FLEXSPI boot	HIGH	LOW	The LPC553x looks for a valid image in the external flash; if there is no valid image, the LPC553x looks for a valid image in the recovery boot device if recovery boot is enabled (4:0, word 1 in CMPA) in CMPA. If it still fails, the LPC553x enters ISP boot mode based on DEFAULT_ISP_MODE bits.
AUTO boot	HIGH	HIGH	The LPC553x looks for a valid image in the internal flash; if there is no valid image, the LPC553x looks for a valid image in the external NOR flash; if no valid image, the LPC553x looks for a valid image in the recovery boot device if recovery boot is enabled d (4:0, word 1 in CMPA) in CMPA. If it still fails, the LPC553x enters ISP boot mode based on DEFAULT_ISP_MODE bits.

Table 5 shows the ISP pin assignments and is the default pin assignment used by the Boot ROM that cannot be changed.

Table 5. ISP pin assignment

ISP pin	Port pin assignment
ISP0	PIO0_5
ISP1	PIO0_7
USART_ISP mode	
FC0_TXD	PIO0_30
FC0_RXD	PIO0_29
I2C_ISP mode	
FC1_SDA	PIO0_13
FC1_SCL	PIO0_14

Table 5. ISP pin assignment...*continued*

ISP pin	Port pin assignment
SPI Flash Recovery mode	
FC0_TXD_SCL_MISO_WS	PIO0_30
FC0_RXD_SDA_MOSI_DATA	PIO0_24
FC0_CTS_SDA_SSELN0	PIO0_31
FC0_SCK	PIO0_28
HS_SPI_SCK	PIO1_2
HS_SPI_SSEL1	PIO1_1
HS_SPI_MISO	PIO1_3
HS_SPI_MOSI	PIO0_26
FC3_TXD_SCL_MISO_WS	PIO0_2
FC3_RXD_SDA_MOSI_DATA	PIO0_3
FC3_CTS_SDA_SSELN0	PIO0_4
FC3_SCK	PIO0_6
SPI ISP mode	
HS_SPI_SCK	PIO1_2
HS_SPI_SSEL1	PIO1_1
HS_SPI_MISO	PIO1_3
HS_SPI_MOSI	PIO0_26
USB0-FS ISP mode	
USB0_VBUS	PIO1_31(if [bit_22] @0x3FC14 is set to 1, use P0_22)
USB0_DP	Dedicated pin per package
USB0_DM	Dedicated pin per package
CAN ISP mode	
CAN_TXD	PIO0_30
CAN_RXD	PIO1_22
FlexSPI Pins	
FLEXSPI_SSEL	PIO0_21
FLEXSPI_CLK	PIO0_19
FLEXSPI_DQS	PIO0_25
FLEXSPI_CLK_N	PIO0_22
FLEXSPI_D0	PIO0_6
FLEXSPI_D1	PIO0_4
FLEXSPI_D2	PIO0_3
FLEXSPI_D3	PIO0_2
FLEXSPI_D4	PIO1_16
FLEXSPI_D5	PIO1_15

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Table 5. ISP pin assignment...*continued*

ISP pin	Port pin assignment
FLEXSPI_D6	PIO1_27
FLEXSPI_D7	PIO1_29

6 Debug and programing interface

When developing your circuit board based on LPC553x/S3x device, use a standard debug signal arrangement to make the connection to the debugger easier.

The JTAG functions TRST, TCK, TMS, TDI, and TDO are selected on pins PIO0_2 to PIO0_6 by hardware when the part is in boundary scan mode.

Note: The JTAG functions can only be used for boundary scan and CANNOT be used to debug LPC553x/S3x device.

The SWD/SWV pins are overlaid on top of the JTAG pins as follows:

Table 6. JTAG and SWD signal description

JTAG mode	SWD mode	Description	MCU port
TRST	-	JTAG Test Reset	PIO0_2
TCK	-	JTAG clock into the core	PIO0_3
TMS	-	JTAG Test Mode Select	PIO0_4
TDI	-	JTAG Test Data Input	PIO0_5
TDO	-	JTAG Test Data Output	PIO0_6
-	SWO	Serial Wire Debug Trace output	PIO0_8
-	SWCLK	Serial Wire Debug clock	PIO0_0
-	SWDIO	Serial Wire Debug I/O	PIO0_9
RESET	RESET	Reset MCU	Dedicate Pin
GND	GND	Ground	-

Note: External pull-up/down resistors for the JTAG signals can be added to increase debugger connection robustness.

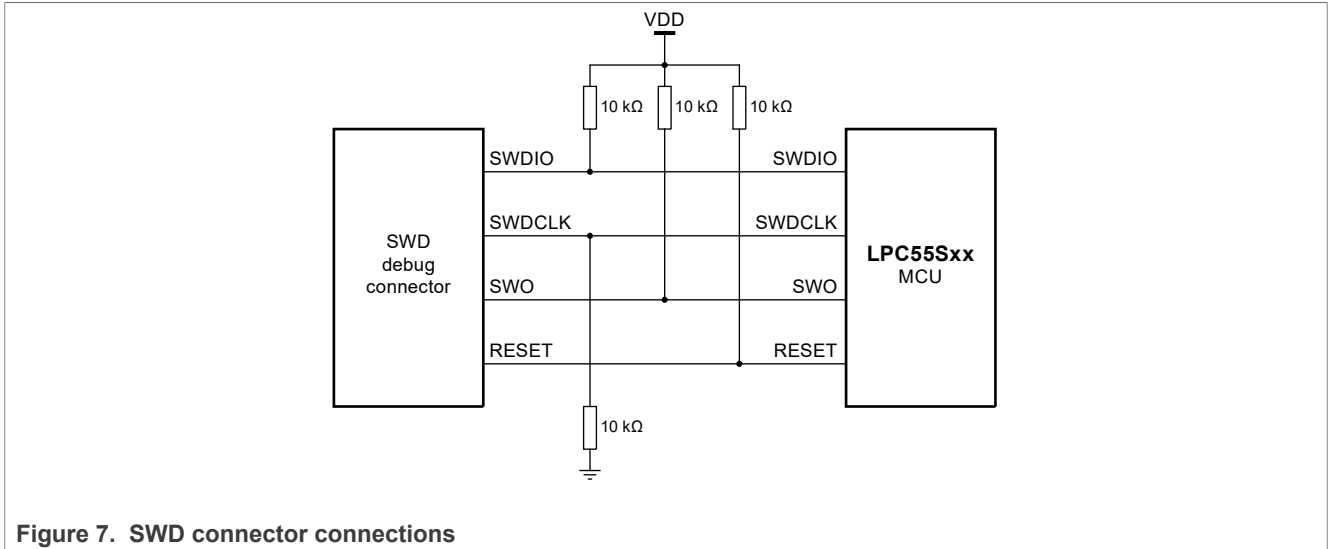Figure 7 shows the SWD signals between the debugger and LPC553x/S3x.

Figure 7. SWD connector connections

6.1 Debug connector pinouts

The JTAG interface on LPC553x/S3x's is only used for BSDL scan; however, the user can use a smaller 0.05" 10-pin connector (Samtec FTSH-105) to debug the device. Similar to the 20-pin Cortex Debug D ETM connector, both JTAG and Serial-Wire debug protocols are supported in the 10-pin version.

Note: *The JTAG functions TRST, TCK, TMS, TDI, and TDO, are selected on pins PIO0_2 to PIO0_6 by hardware when the part is in boundary scan mode. The JTAG functions cannot be used for debug mode.*
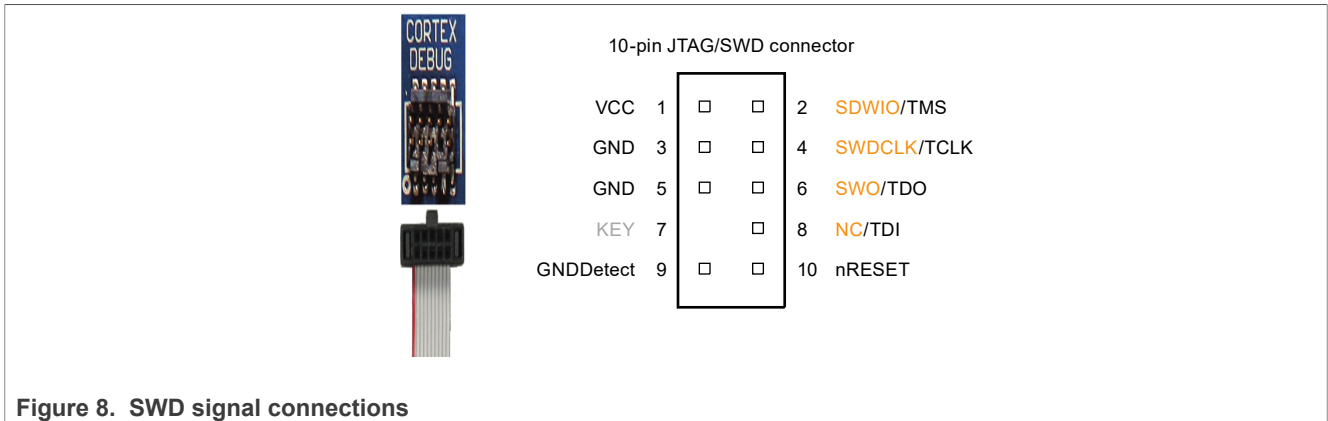
Figure 8. SWD signal connections

6.2 Boundary scan

JTAG/boundary scan is an interface containing four ports. The interface allows access to special embedded logic on most chips. JTAG/boundary can provide several functions that can contain any or all of the following:

- Probe-less device connectivity test.
- Logic programming for Flash memory, CPLD, and FPGA.
- Debug logic in microprocessors and microcontrollers used for software debugging, or test connections with peripheral devices at speed without embedded software.

For the boundary scan usage, refer to *How to Perform Boundary Scan for LPC55(S)xx Based on μTrace and Trace32* (document AN13507).

7 Communication modules

This section provides details about communication modules.

7.1 FlexSPI interface

LPC553x/S3x has one instance of the FlexSPI module (Serial Peripheral Interface), this FlexSPI host controller supports 1 port and up to 2 external devices. It supports Single/Dual/Quad/Octal mode data transfer (1/2/4/8 bidirectional data lines). FlexSPI is the most commonly used external memory interface.

For clock signal routing, refer to section "FlexSPI parameters" from the *LPC553x/S3x datasheet* (document LPC553x) and *LPC553x/S3x Reference Manual* (document LPC553xRM). If you are using a Serial flash device from Micron, refer to *Layout Guidelines – Serial NOR Flash Introduction* (document TN-25-09) from Micron.

PCB design recommendations to connect serial flash on LPC553x/S3x FlexSPI interface are given below:

1. Vcc power supply decoupling:
   For decoupling power supply VCC, two ceramic capacitors are recommended on the external memory device, one 4.7 µF and one 0.1 µF.
2. Decoupling capacitor routing length:
   Reducing decoupling capacitor routing length helps minimize total loop inductance. This measure includes the following:
   - Reduced VCC and VSS decoupling capacitor pad fanout trace length
   - Fan out trace width equal to or less than the capacitor pad width
   - Power and ground planes
   - Decoupling capacitor placement relative to the device
3. Decoupling capacitor placement:
   Decoupling capacitors must be as close as possible to VCC and VSS pads with priority as follows: Closest is 0.1 µF followed by 4.7 µF.
4. CLK signal routing:
   The following clock trace guidelines help minimize impedance variation:
   - To minimize impedance variation, maintain a straight clock trace as much as possible by using arc-shaped bends instead of right-angle bends
   - Maintain a short clock trace as much as possible, and match lengths between clock and data signals.
   - Use one signal layer to ensure constant transmission line impedance for the clock signal.
   - Place a ground plane next to the outer layer to minimize noise from other signals.
   - If an inner layer is used to route the clock trace, sandwich the inner layer between reference planes.
   - To minimize reflection, terminate clock signals or set up an appropriate driver strength, and keep the clock trace with controlled impedance (**typically 50 ohm trace impedance**).
   - To ensure signal quality, use point-to-point clock trace as much as possible.
   - To reduce crosstalk from other nearby signals, maintain space between the clock signal line and other signal lines as wide as possible. Moreover, take care to have dielectric height of more than three times the distance between two adjacent lines.
5. Data signal routing
   - Data signals must not be over the split plane.
   - Data signals must not be routed over via-anti pads.
   - Maintain a continuous reference plane for each data signal over its entire path.
   - If the signal reference plane changes from the ground plane to power plane, add capacitors near the via transition site to help support a good return path.
   - If the signal reference plane changes from one ground plane to another, ground vias must surround all signals (Two ground vias per clock via; one ground via per high-speed signal via).

• Keep stubs short to avoid reflections. Keep stub propagation delay to <20 % of the signal risetime.

7.2 USB interface

Use the recommendations below for the USB:

• Route the high-speed clocks and the DP and DM differential pair first.
• Route the DP and DM signals on the top (or bottom) layer of the board.
• The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90 Ω.
• Route the traces over the continuous planes (power and ground). They must not pass over any power/GND plane slots or anti-etch. When placing the connectors, make sure that the ground plane clear-outs around each pin have ground continuity between all pins.
• Maintain the parallelism (skew-matched) between DP and DM, and match the overall differential length difference to fewer than 5 mils.
• Maintain the symmetric routing for each differential pair.
• Do not route the DP and DM traces under the oscillators or parallel to the clock traces (and/or data buses).
• Minimize the lengths of the high-speed signals that run parallel to the DP and DM pair.
• Keep the DP and DM traces as short as possible.
• Route the DP and DM signals with a minimum number of corners. Use 45-degree turns instead of 90-degree turns.
• Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
• Provide the ground return vias within a 50-mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
• When the USB signals are not used, refer to Table 8.

7.3 CAN interface for CAN-FD module

LPC553x/S3x have a CAN-FD interface, the physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as the minimum and 140 Ω as the maximum). The use of shielded twisted-pair cables is necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for an unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an LPC553x/S3x microcontroller is shown in Figure 9.

Figure 9. CAN physical transceiver circuit
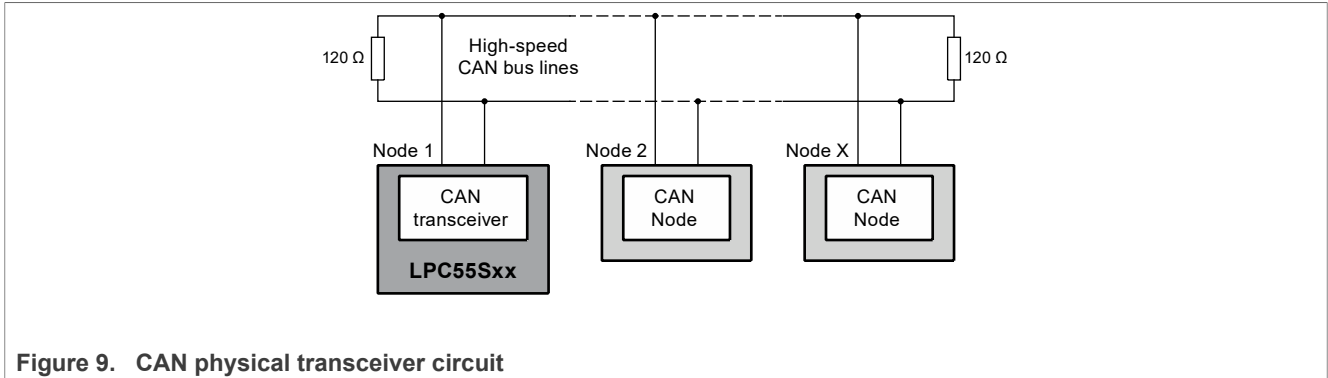
The LPC553x/S3x CAN-FD module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbit/s. Like most others CAN physical transceivers, CANH, and CANL are available for the designer to terminate the bus depending on the application. Figure 9 and Figure 10 show examples of the CAN node terminations.

Figure 10. CAN physical transceiver circuit
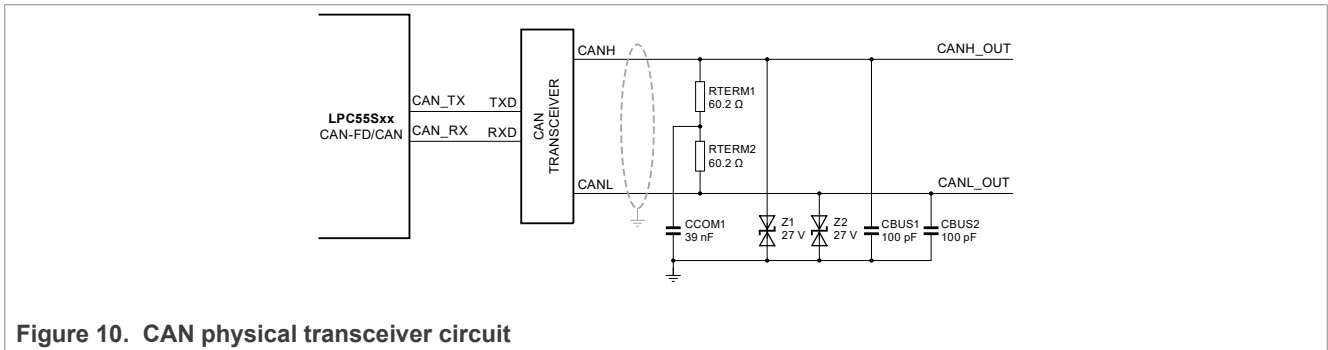
8 Analog

This section gives information about ADC impedance, OPAMP usage, and High-Speed Comparator (HSCMP) usage.

8.1 ADC impedance

LPC55(S)3x ADC with Hardware Trigger and ADC Calculator Tool (document AN13523) introduces the details of ADC and provides the ADC calculator tool to support users to define the max sampling rates that can be achieved depending on the input signal impedance characteristics.
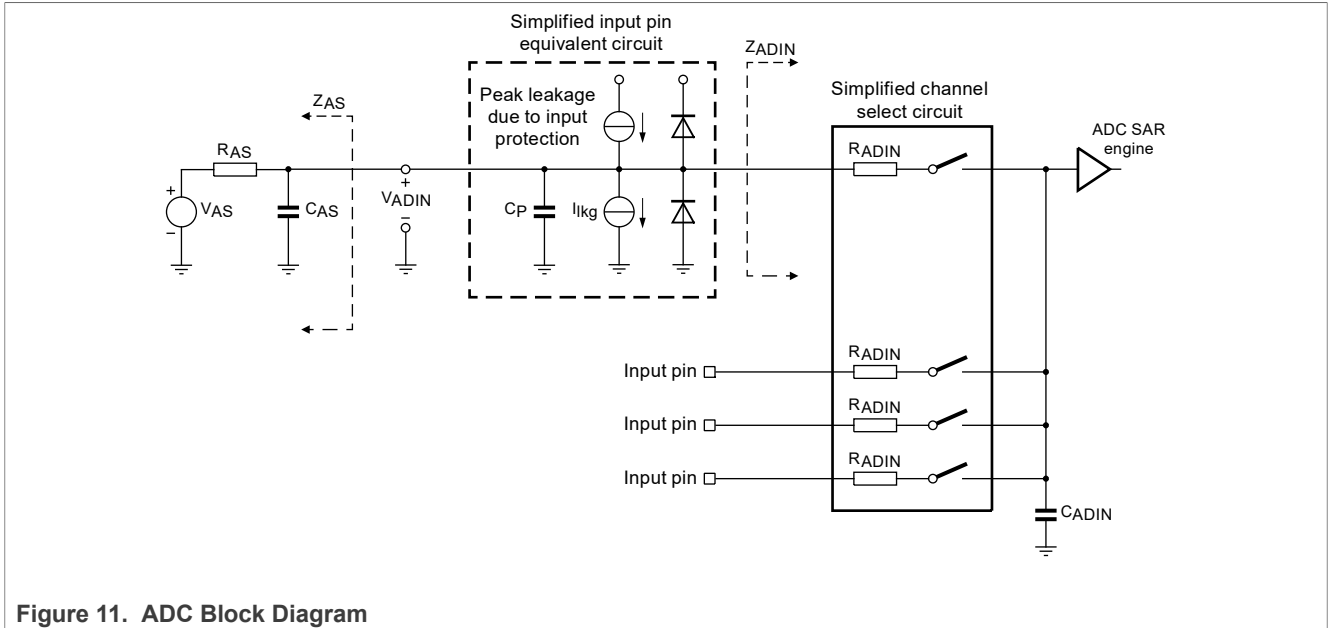
LPC553x/S3x ADC block diagram is shown on Figure 11:

Figure 11. ADC Block Diagram

Datasheet only shows the RADIN values as shown in Table 7:

Table 7. ADC input resistance

Symbol	Parameter	Conditions	Min	Typical	Max	Unit
Ri	Input resistance	Fast/Muxed ADC Input Channels (PIO0_1. PIO0_10. PIO0_11. PIO0_12, PIO0_15, PIO0_16, PIO01_0, PIO1_7)				
		VDDA = 1.8 V	-	-	1.6	kΩ
		VDDA = 3.0 V	-	-	1.1	kΩ
		Fast/Muxed/Internal ADC Input Channels (PIO1_9)				
		VDDA = 1.8 V	-	-	1.87	kΩ
		VDDA = 3.0 V	-	-	1.1	kΩ
		Standard/Muxed ADC Input Channels (PIO0_23, PIO0_31, PIO1_19. PIO1_20, PIO1_24, PIO2_0)				
		VDDA = 1.8 V	-	-	3.2	kΩ
		VDDA = 3.0 V	-	-	1.8	kΩ
		Fast/Dedicated ADC Input Channels (ADC1IN1A, ADC1IN1B)				
		VDDA = 1.8 V	-	-	0.3	kΩ
		VDDA = 3.0 V	-	-	0.3	kΩ
		Standard/Dedicated ADC Input Channels (ADC0IN4A, ADC0IN5A, ADC0IN5B, ADC1IN4A, ADC1IN5A, ADC1IN5B)				
		VDDA = 1.8 V	-	-	0.3	kΩ
		VDDA = 3.0 V	-	-	0.3	kΩ

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8.2 OPAMP usage

OPAMP is an electronic integrated circuit containing multi-stage amplifier circuit. Its input stage is a differential amplifier circuit. It has high input resistance and the ability to suppress zero drift.

For the OPAMP usage, refer to *OPAMP Usage on LPC553x/LPC55S3x* (document AN13508).

8.3 High-Speed Comparator (HSCMP) usage

The High-Speed Comparator (HSCMP) module provides a circuit to compare two analog input voltages. It includes a comparator (CMP), comparator input selectors, 8-bit DAC, and an analog mux for each comparator input.

LPC553x/LPC55S3x High-Speed Comparator - Evaluation of Basic Features (document AN13540) describes various design criteria that system designers must consider when implementing HSCMP designs with the LPC553x/S3x family of microprocessors.

9 Recommendations

The section gives general recommendations.

9.1 Pin descriptions

The section gives pin descriptions.

9.1.1 Pin pull-up/down and open-drain

All pins have all pull-ups, pull-downs, and inputs turned off at reset except PIO0_0, PIO0_2, PIO0_5, PIO0_9, PIO0_13, and PIO0_14 pins. It prevents power loss through pins before software configuration. Due to special pin functions, some pins have a different reset configuration. PIO0_5 and PIO0_12 pins have internal pull-up enabled by default, and PIO0_0, PIO0_2, PIO0_3, and PIO0_4 have internal pull-down enabled by default. PIO0_13 and PIO0_14 are true open-drain pins.

9.1.2 ADC pins

Some functions, such as ADC or comparator inputs, are available only on specific pins when digital functions are disabled on those pins. By default, the GPIO function is selected except on pins PIO0_0 and PIO0_9, which are the serial wire debug pins. It allows debugging to operate through the reset.

9.1.3 Wake-up pins

The external reset pin or wake-up pins can trigger a wake-up from deep power-down mode. For the wake-up pins, do not assign any function to this pin if it will be used as a wake-up input when using deep power-down mode. If not in deep power-down mode, a function can be assigned to this pin. If the pin is used for wake-up, it must be pulled HIGH externally before entering deep power-down mode. A LOW-going pulse as short as 50 ns causes the chip to exit deep power-down mode and wakes up the part.

9.1.4 JTAG function pins

JTAG functions TRST, TCK, TMS, TDI, and TDO, are selected on pins PIO0_2 to PIO0_6 by hardware when the part is in boundary scan mode. The JTAG functions cannot be used to debug the device.

9.2 Termination of unused pins

Table 8 shows how to terminate pins that are not used in the application. In many cases, unused pins must be connected externally or configured correctly by software to minimize the overall power consumption of the part.

Unused pins with GPIO function must be configured as outputs set to LOW with their internal pull-up disabled. To configure a GPIO pin as output and drive it LOW, select the GPIO function in the IOCON register, select output in the GPIO DIR register, and write a 0 to the GPIO PORT register for that pin. Disable the pull-up in the pin's IOCON register.

In addition, configure all GPIO pins that are not bonded out on smaller packages as outputs driven LOW with their internal pull-up disabled.

Table 8. Termination of unused pins

Pin	Default state	Recommended termination of unused pins
RESET	Input, pull-up	The reset pin can be left unconnected if the application does not use it
All PIOn_m (not open-drain)	Input, pull-up	Can be left unconnected if driven LOW and configured as GPIO output with pull-up or pull-down disabled by software.
PIOn_m (I2C open-drain)	Inactive No pull-up or down	Can be left unconnected if driven LOW and configured as GPIO output by software.
XTAL32M_P		Connect to the ground. When grounded, the RTC oscillator is disabled
XTAL32M_N		Can be left unconnected.
XTAL32K_P	-	Connect to the ground. When grounded, the RTC oscillator is disabled.
XTAL32K_N	-	Can be left unconnected.
VREFP	-	Tie to VDD_MAIN
VREFN	-	Tie to VSS
VDDA	-	Tie to VDD_MAIN
VSSA	-	Tie to VSS
USBn_DP	Float	Can be left unconnected
USBn_DM	Float	Can be left unconnected
USBn_3V3	Float	Tie to VDD_MAIN. If not using USB and using a 1.8 V supply, USBn_3V3 can be connected to 1.8 V
USB1_VBUS	Float	Tie to VDD_MAIN
USBn_VSS	Float	Tie to VSS

9.3 Printed circuit board

For technical reasons, use a multilayer printed circuit board (PCB) with a separate layer dedicated to the ground (VSS) and another dedicated to the VDD supply. It provides good decoupling and a good shielding effect. For many applications, economic reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for the ground and the power supply.

9.4 General board layout guidelines

This section gives general board layout guidelines.

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9.4.1 Stencil for HLQFP package

To design a "solder paste stencil", see Figure 12.

Use a stencil with a thickness of 0.125 mm; however, other thicknesses such as 0.150 mm may be suitable.

Make sure the size of the 4x inner square windows for exposed pad matches Figure 12 (4x1.25, circled in red).

If the exposed pad square windows size is not enough, the LPC553x/S3x I/O ground pad may not connect to GND. It will cause the MCU to become unstable after power-up.
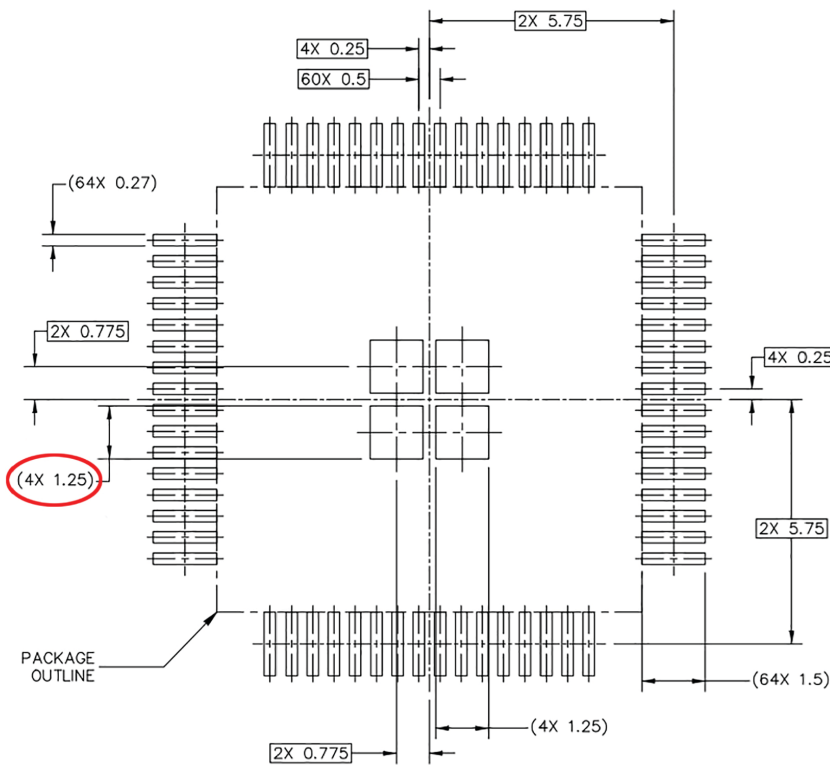
Figure 12. HLQFP soldering footprint guideline

9.4.2 Traces recommendations

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in Figure 13.

NOT CORRECT
Sharp corner causes
more reflection

CORRECT
Smooth corner
reduces reflections

Figure 13. Poor and correct way of bending traces in right angles
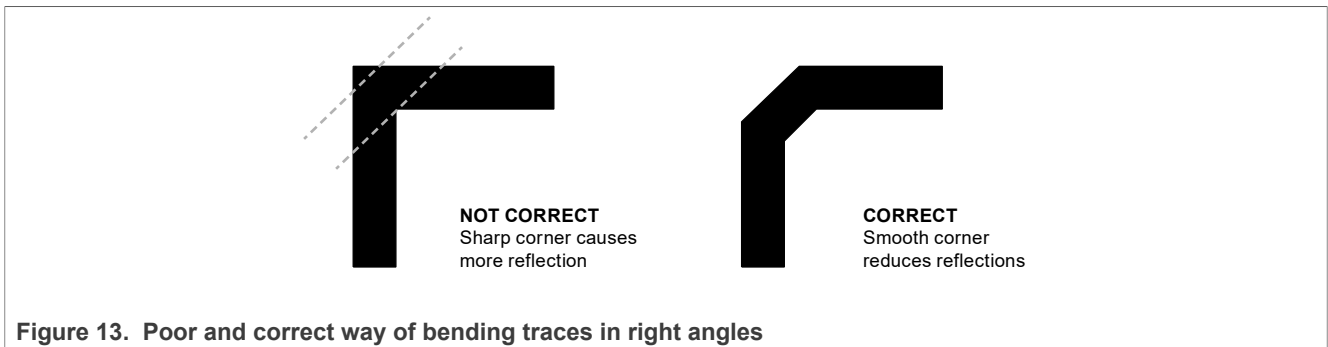
To minimize crosstalk not only between two signals on one layer, but also between adjacent layers, route them at 90° to each other. Complex boards must use vias while routing; you have to be careful when using them. These vias add additional capacitance and inductance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace.

9.4.3 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and therefore reduce the potential of the ground loop from the circuit back to the supply.

- Route high-speed signals above a solid and unbroken ground plane.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There must be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect this copper pour area to the ground plane through vias.

See correct grounding technique in Figure 14.

Figure 14. Eliminating floating metal/shape
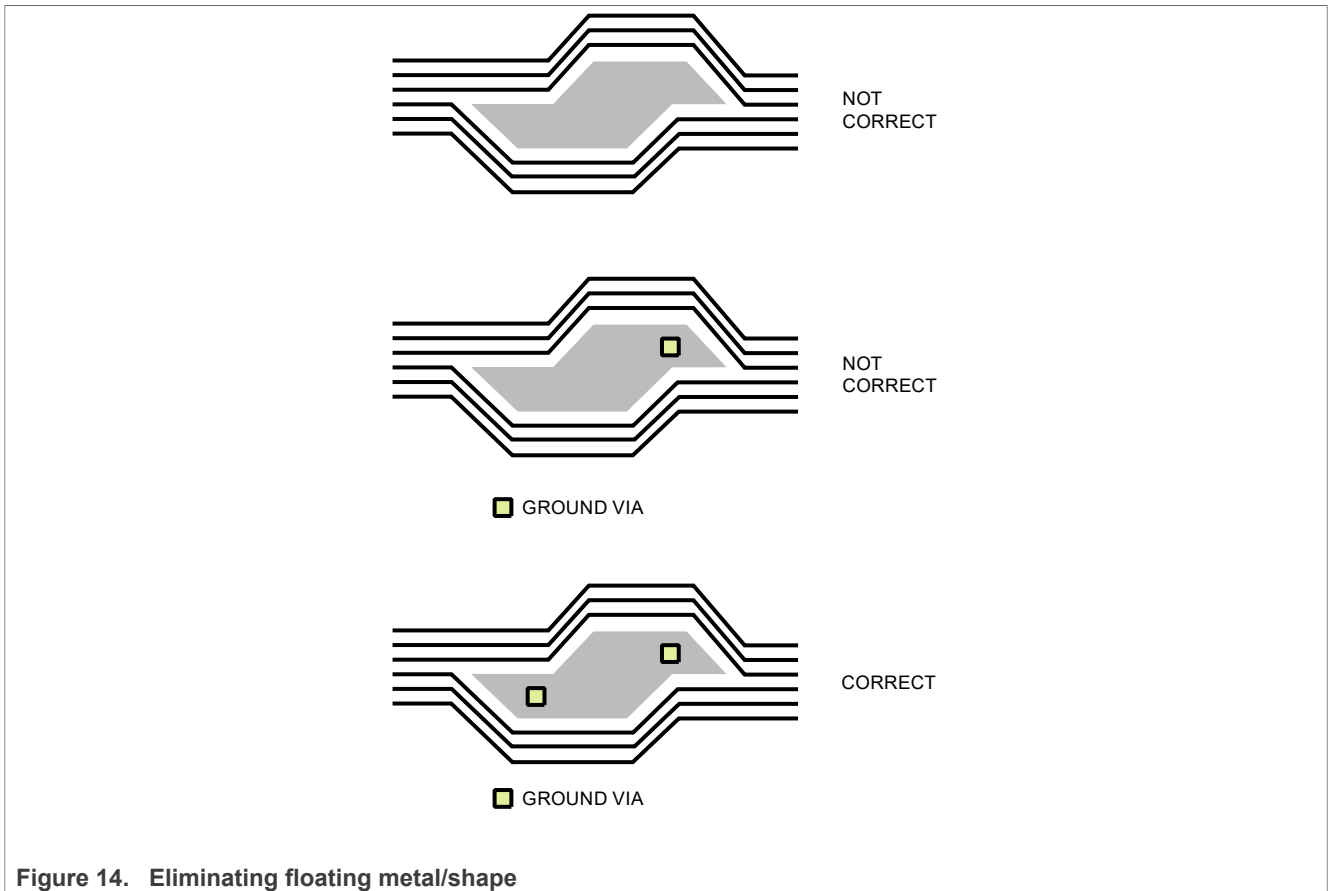
9.4.4 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is explained, each board and system experience this in its way. There are many PCB and component-related variables involved.

This application note does not go into the electromagnetic theory or explain the specifics of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: Conduction and Radiation.

	Propagation path
1	Conductor
2	Air
3	Air to conductor
4	Conductor to air
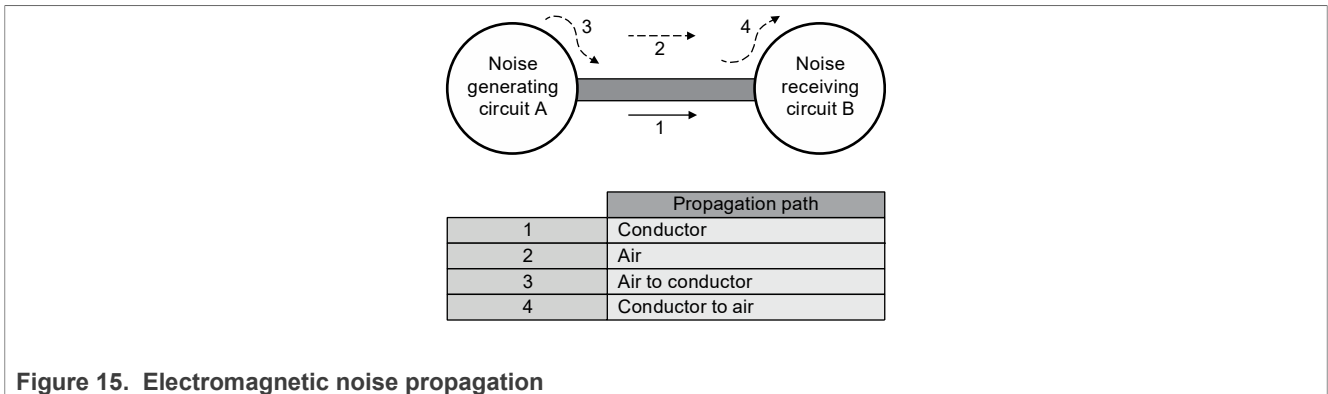
Figure 15. Electromagnetic noise propagation

The design considerations narrow down to:

- The radiated and conducted EMI from the board must be lower than the allowed levels by the standards you are following.
- The ability of the board to operate successfully counteracting the radiated and conducted electromagnetic energy (EMC) from other systems around it.

The EMI sources for a system consist of several components such as PCB, connectors, and cables. The PCB plays a major role in radiating high-frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy, for example, a large loop of signal and corresponding ground. The five main sources of radiation are digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, and PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy, which can fail the EMI test. This is a huge subject and there are many books, articles, and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.

However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors must have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

9.4.5 PCB layer stacking

To reach signal integrity and performance requirements, four-layer PCB is recommended for implementing Ethernet applications and systems. The following layer stack-ups are recommended for four, six, and eight-layer boards, although other options are possible.

Figure 16. PCB layer stacking
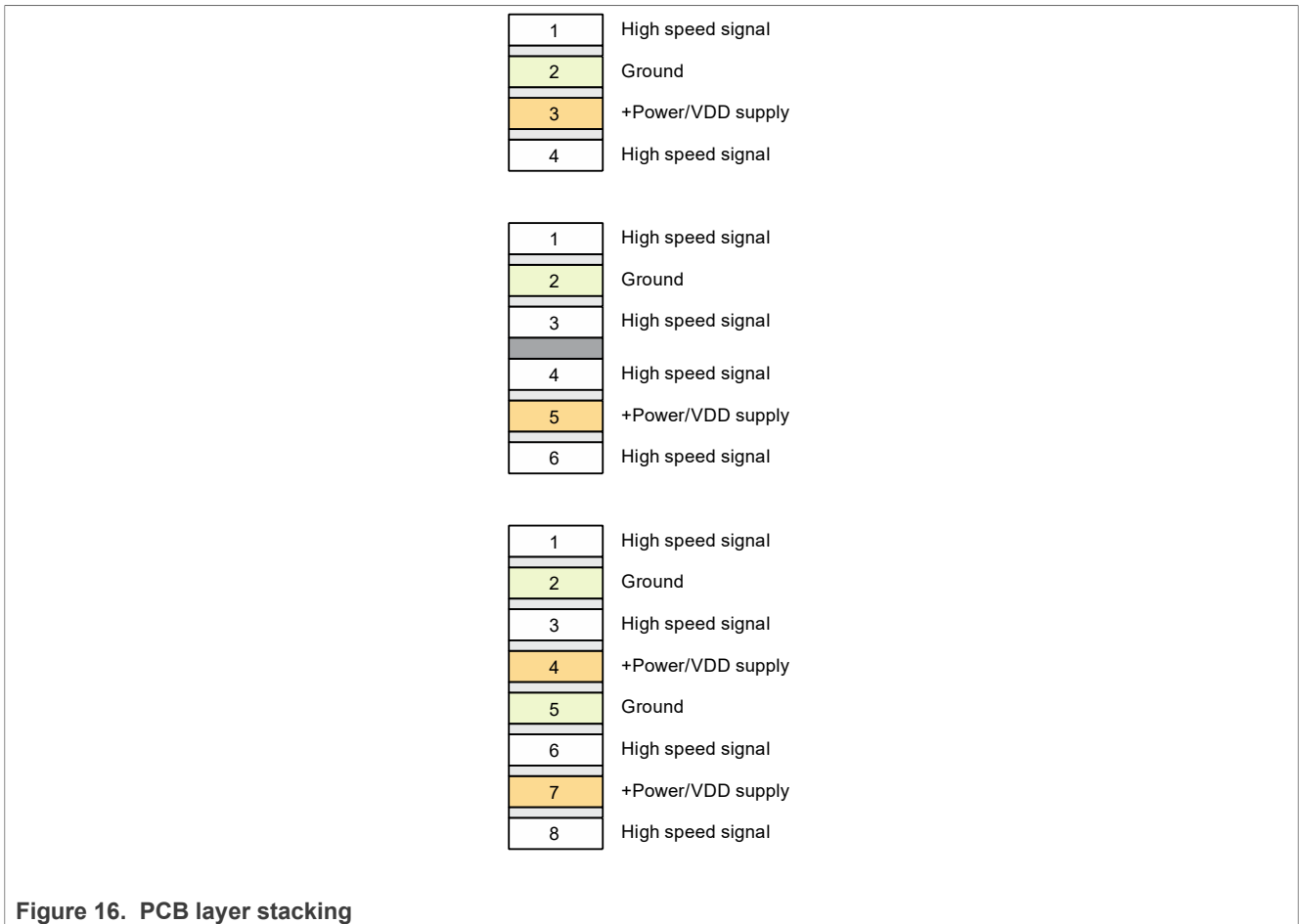
9.4.6 Injection current

All pins implement protection diodes that protect against electrostatic discharge (ESD). Often, both digital and analog pins must be connected to voltages that are higher than the operating voltage of the device pin.

The internal ESD diodes of the microcontroller are designed for short discharge pulses only, and they do not sustain a constant current over time. Therefore, the maximum continuous voltage that drops over them is specified in the DC electrical parameters and the maximum high input voltage must not be higher than VDD + 0.5 V, and the current injection must be limited as defined in the device data sheet. The DC injection marked as total ground current is in the *LPC553x/S3x Data Sheet* (document LPC553x).

In other words, the voltage and current of an input signal must be within the electrical parameter allowed. The outcome of violating these specifications causes unexpected behavior, stuck operation, or a major damage in the MCU.

10   References

1. *Hardware Design Guidelines for LPC55(S)xx Microcontrollers* (document AN13033)
2. *LPC553x/S3x Data Sheet* (document LPC553x)
3. *LPC553x/S3x Reference Manual* (document LPC553xRM)
4. *Using the DC-DC and LDO Features on the LPC553x/LPC55S3x Family* (document AN13528)
5. *LPC55(S)3x ADC with Hardware Trigger and ADC Calculator Tool* (document AN13523)

6. *OPAMP Usage on LPC553x/LPC55S3x* (document AN13508)
7. *LPC553x/LPC55S3x High-Speed Comparator - Evaluation of Basic Features* (document AN13540)
8. *Understanding Cap Bank in LPC55(S)xx* (document AN13057)
9. *How to Perform Boundary Scan for LPC55(S)xx Based on µTrace and Trace32* (document AN13507)
10. *Layout Guidelines – Serial NOR Flash PCB Design Recommendations* (document TN-25-09)

11 Revision history

Table 9. Revision history

Document ID	Release date	Description
AN13707 v.2	23 May 2024	Minor updates
AN13707 v.1	25 September 2023	Initial version

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