

# AN13415

## PCA9481A monolithic integrated high-voltage 2:1 switched capacitor direct battery charger

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Application note

### Document information

Information	Content
Keywords	PCA9481A 10A 2:1/1:2/1:1 mode switched capacitor
Abstract	This application note describes the details of customer applications including external components.



# 1 Abstract

Many mobile phones have adopted features requiring high system performance such as 5G, multiple cameras and high resolution LCDs with multi-processors, increasing the demand for higher battery capacity. These power-hungry features have created the need for users to charge their mobile phone batteries frequently and quickly.

Legacy inductor-based chargers are still widely used in mobile applications, but the high heat from induction charging limits higher charging power for the battery, unable to satisfy users requiring fast charging.

Switched-capacitor (SC) direct charging has been recognized as a good replacement of inductor-based chargers due to higher efficiency with lower heat dissipation. Fast direct chargers have become mandatory in many mobile phones including low-tier models.

PCA9481A achieves best-in-class SC direct charging in terms of efficiency with lower BOMs.

This application note describes the details of customer applications including external components.

# 2 PCA9481A charging application

## 2.1 50 W charging application at $IVBUS \leq 3 A$

Mobile device integrates USB Type-C receptacle basically, but most Type-C cables only support up to 3 A current delivery and E-mark chip should be mounted onto Type-C cable for greater than 3 A current. To achieve 50 W charging with exiting cable not mounted to an E-mark chip, higher input voltage is required. [Figure 1](#) provides the proper solution to charge a battery with a 3 A Type-C USB cable.

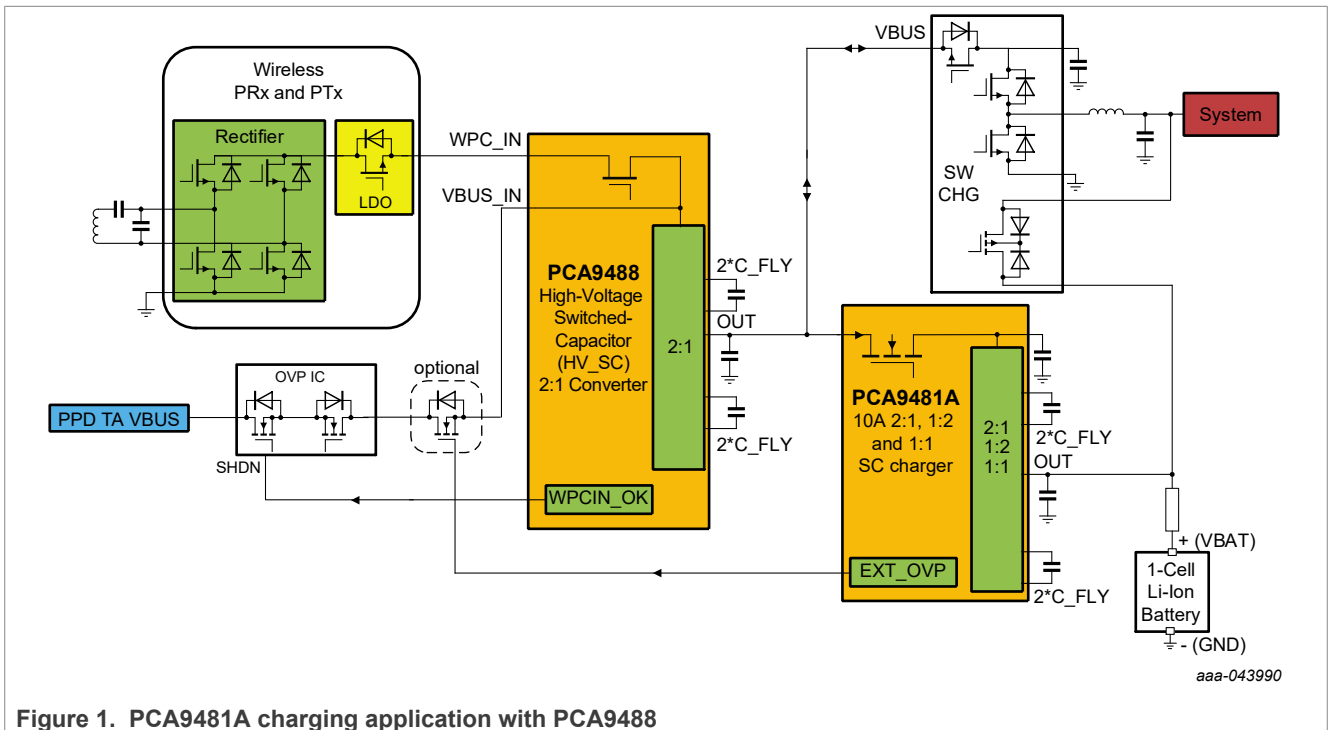


Figure 1. PCA9481A charging application with PCA9488

For 50 W charging with under 3 A input current, input voltage of 2 x 2:1 cascade SC converters should be 4 times higher than output voltage to achieve max 10 A output current. We recommend to use PCA9488 just before PCA9481A for half of the input current with a single SC 2:1 charger.

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PCA9481A is placed in parallel with an inductor-based switching charger that is operated during USB PD; controller cannot adjust input voltage and current according to battery condition, such as fully discharged battery. In this case, mobile AP can't be started up to implement USB PD.

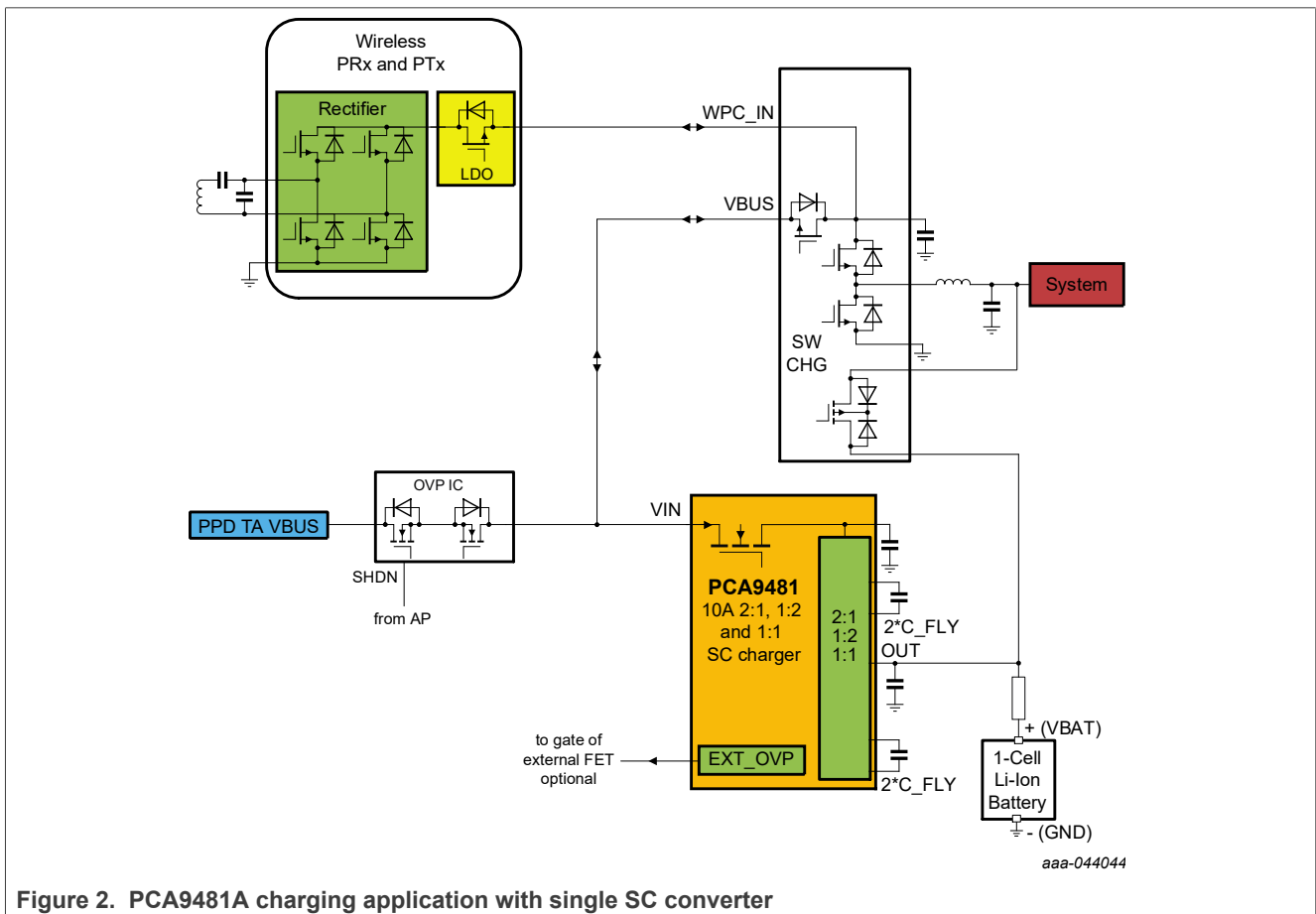
Output voltage of PCA9488 is 0.5x input voltage and output current is 2x input current. So VBUS should be 4x output voltage of PCA9481A, and current at VBUS is ¼ of output current of PCA9481A.

Optionally external FET between OVP and VBUS\_IN of PCA9488 could be the replacement of OVP IC depending on application requirement. NMOS and back-to-back can be selected.

2.2 50 W charging application without additional 2:1 converter

Input current of VBUS reaches 5 A which is half of max output current. Single PCA9481A can support 50 W charging without additional SC converter.

An example of the charging block is shown in [Figure 2](#)



### 3 PCA9481A reference schematic

#### 3.1 Reference schematic with external FET controlled by PCA9481A

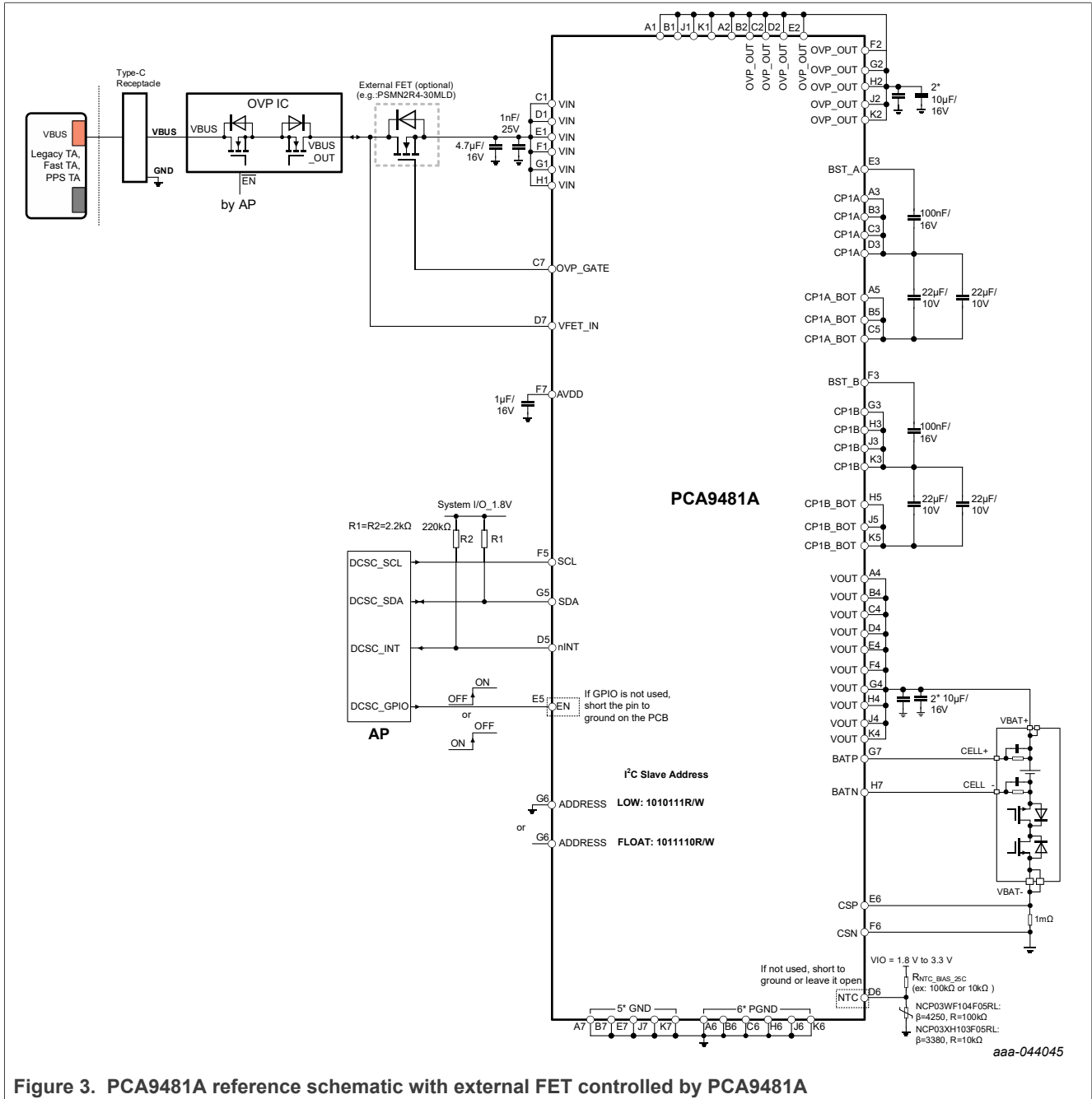


Figure 3. PCA9481A reference schematic with external FET controlled by PCA9481A

### 3.2 Reference schematic with OVP IC

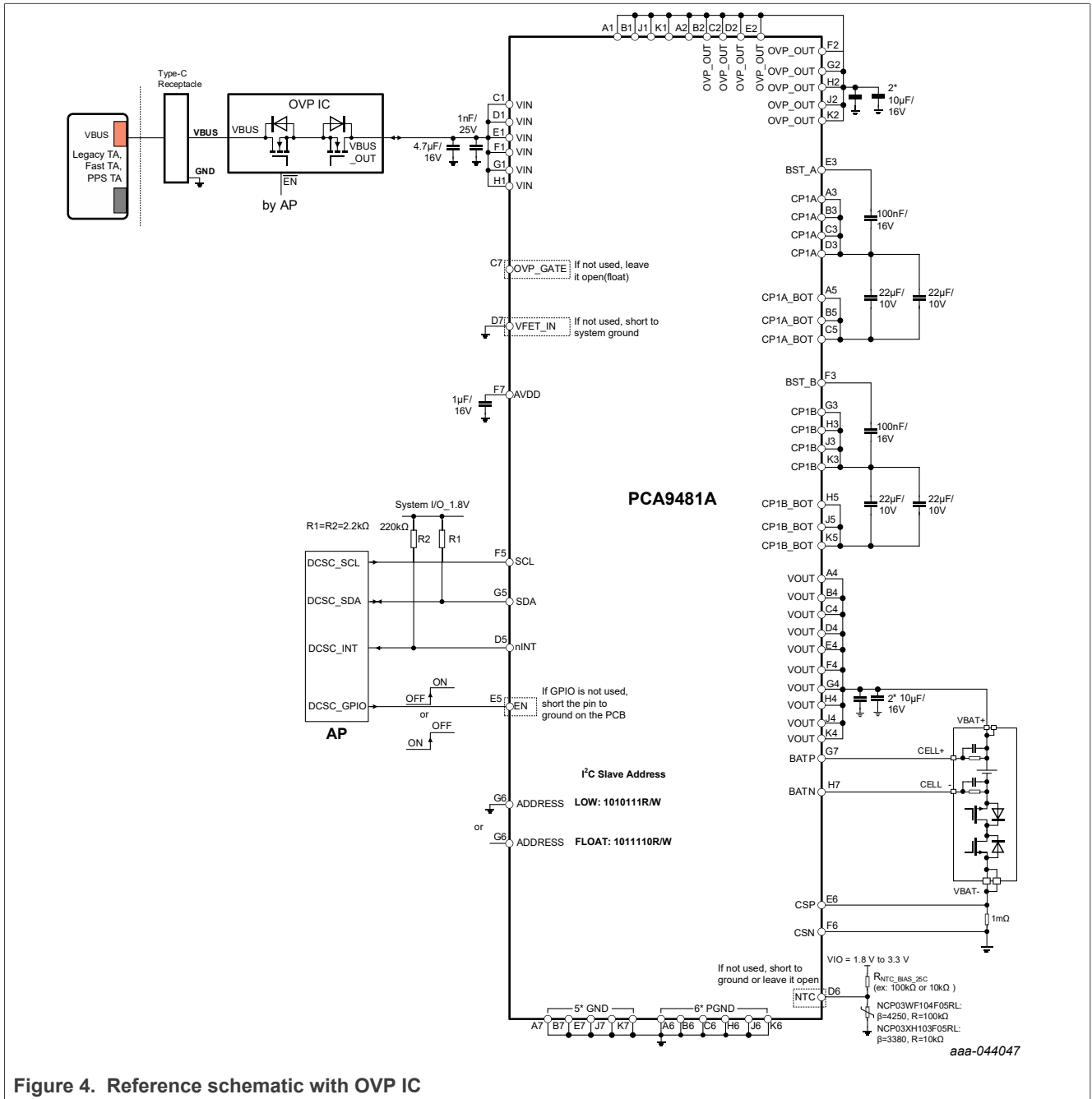


Figure 4. Reference schematic with OVP IC

### 3.3 I<sup>2</sup>C and other digital pins

PCA9481A provides the option of two I<sup>2</sup>C slave addresses determined by the ADDRESS pin setting as shown in [Table 1](#).

Table 1. I<sup>2</sup>C slave addresses

ADDRESS	Slave Address (Write) in hex	Slave Address (Read) In hex
LOW	AE	AF
FLOAT	BC	BD

I<sup>2</sup>C clock speed supports up to 1 MHz. SDA and SCL require a 2.2 kΩ pullup resistor.

EN pin is the digital pin to enabling device. The polarity of EN pin is selected in EN\_CFG in Register 0x18.

nINT is the open drain output requiring a 220 kΩ pullup resistor. It goes LOW when any unmasked interrupt bit is asserted.

nINT pin can be floating or open if not used.

### 3.4 NTC

The NTC input with AVDD pull-up voltage is connected to an external negative temperature coefficient (NTC) thermistor to monitor system temperature or NTC on battery package to monitor battery temperature. To utilize NTC function, set NTC\_EN bit to 1b. There are two registers to set a different temperature threshold such as hot/warm and cold/cool. If one of two programmed threshold is monitored, the device issues a corresponding interrupt signal.

### 3.5 AVDD

AVDD is the internal LDO output requiring a 1 μF/6.3 V bypass capacitor. Typical AVDD is 1.536 V. Minimum and maximum AVDD are 1.53 V and 1.54 V, respectively.

### 3.6 Input capacitor selection

In a switched capacitor converter application, large AC currents flow through the input/output capacitors. The input capacitor helps to keep the input voltage stable during switching operation.

A capacitor should be considered to flow the RMS current. Low ESR ceramic capacitors are highly recommended for this application. Larger size X7R MLCC capacitors are normally recommended. Capacitance derating needs to be considered at a DC bias voltage.

### 3.7 Flying capacitor selection

Large AC currents flow through the flying capacitors. Low ESR ceramic capacitors are highly recommended for this application. The flying capacitor must be selected to accommodate the maximum load current. Larger size X7R MLCC capacitors are normally recommended. Capacitance derating needs to be considered at a DC bias voltage.

In general, a recommended voltage ripple at C<sub>FLY</sub> is about 2 % of output voltage. If the max output voltage is 5 V, the ripple at C<sub>FLY</sub> is 100 mV. The value of C<sub>FLY</sub> can be obtained from the formula below in dual phase.

$$C_{FLY} (\mu F) = \frac{I_{OUT} (max)}{2 \times frequency \times \Delta V_{CFLY} (Voltage\ ripple)}$$

Where:

I<sub>OUT</sub> (max): A maximum output current

ΔV<sub>CFLY</sub>: voltage ripple on fly cap

Frequency: SC's operating frequency

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2 x 22 μF is fully verified in application, and can support 50 W charging in smartphone form factor without additional thermal dissipation measure.

3.8 Output capacitor selection

Large AC current flows through the flying capacitors and input/output capacitors. The average output current is given by the formula below.

$$I_{OUT} = 2 \times \text{Frequency} \times C_{FLY} \times \Delta V_{CFLY}$$

The total output voltage ripple is:

$$\Delta V_{OUT} = \frac{I_{OUT}}{2 \times \text{frequency} \times (C_{FLY} + C_{SC\_OUT})}$$

A voltage ripple at C<sub>VOUT</sub> should be determined by system requirement.

3.9 Bill of Materials (BOM)

Table 2 shows all of the components for the device.

Table 2. Bill of materials

Name	Value	Size	Part name / Maker	Note
C <sub>VIN</sub>	4.7 μF/16 V	1608	Murata, GRM188C71C475ME21	C <sub>EFF</sub> =1.4 μF at 10 V
	1 nF/25 V	0603	Murata, GRM033R61E102KA01	Optional for high frequency filter
C <sub>OVP_OUT</sub>	10 μF/16 V	1608	Murata, GRM188R61C106KAAL	Two capacitors. C <sub>EFF</sub> =1.7 μF for one capacitor at 10 V
C <sub>FLY</sub>	22 μF/16 V	1608	SEMCO, CL10A226MO7JZNC	Two capacitors. C <sub>EFF</sub> = 6.9 μF at 5 V
C <sub>BST</sub>	100 nF/16 V	0603	Murata, GRM033R61C104KE14	
C <sub>VOUT</sub>	22 μF/10 V	1608	SEMCO, CL10A226MP8NUNE	Two capacitors. C <sub>EFF</sub> = 5 μF at 4.5 V
C <sub>AVDD</sub>	1 uF/6.3 V	0603	Murata, GRM033D70J105ME01	C <sub>EFF</sub> = 0.88 μF at 1.5 V
R <sub>SENSE</sub>	1/2/5 mΩ			For battery current
R <sub>I2C</sub>	2.2 kΩ	0603		SCL and SDA
R <sub>nINT</sub>	220 kΩ	0603		
NTC	β=4250 or β=3380	0603	NCP03WF104F05RL or NCP03XH103F05RL	Place it if needed
External N-ch FET	30 V, 2.4 mΩ	2.225 x 0.19 x 0.85	PSMN2R4-30MLD / Nexperia	External N-FET in case of no stand-alone OVP IC used. The N-FET is not subject to the use of this N-FET. Another N_FET or back-to-back can be used.

4 Layout guides

The device has a dual phase converter with two flying capacitors on each phase. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Utilize 8-layer board for optimal layout, and assign one layer as solid ground plane near the device to minimize high-current path
2. Place flying capacitors as close to CP1A, CP1B, CP1A\_BOT and CP1B\_BOT bumps as possible. The trace shall be wide enough to carry the charging and discharging current and short to minimize trace resistance which affects efficiency directly.

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3. Place output capacitor as close as possible to VOUT bumps. Use as wide as possible on the 3<sup>rd</sup> layer to short VOUT from each phase
4. Place input capacitors as close as possible to VIN; input power trace should be routed to center of VIN pins
5. Place two OVP\_OUT capacitors next to device symmetrically
6. Decoupling capacitors shall be placed next to the device and make trace connection as short as possible
7. Ensure that there are sufficient thermal vias directly under bumps of the power FETs, power ground, connecting to copper on other layers

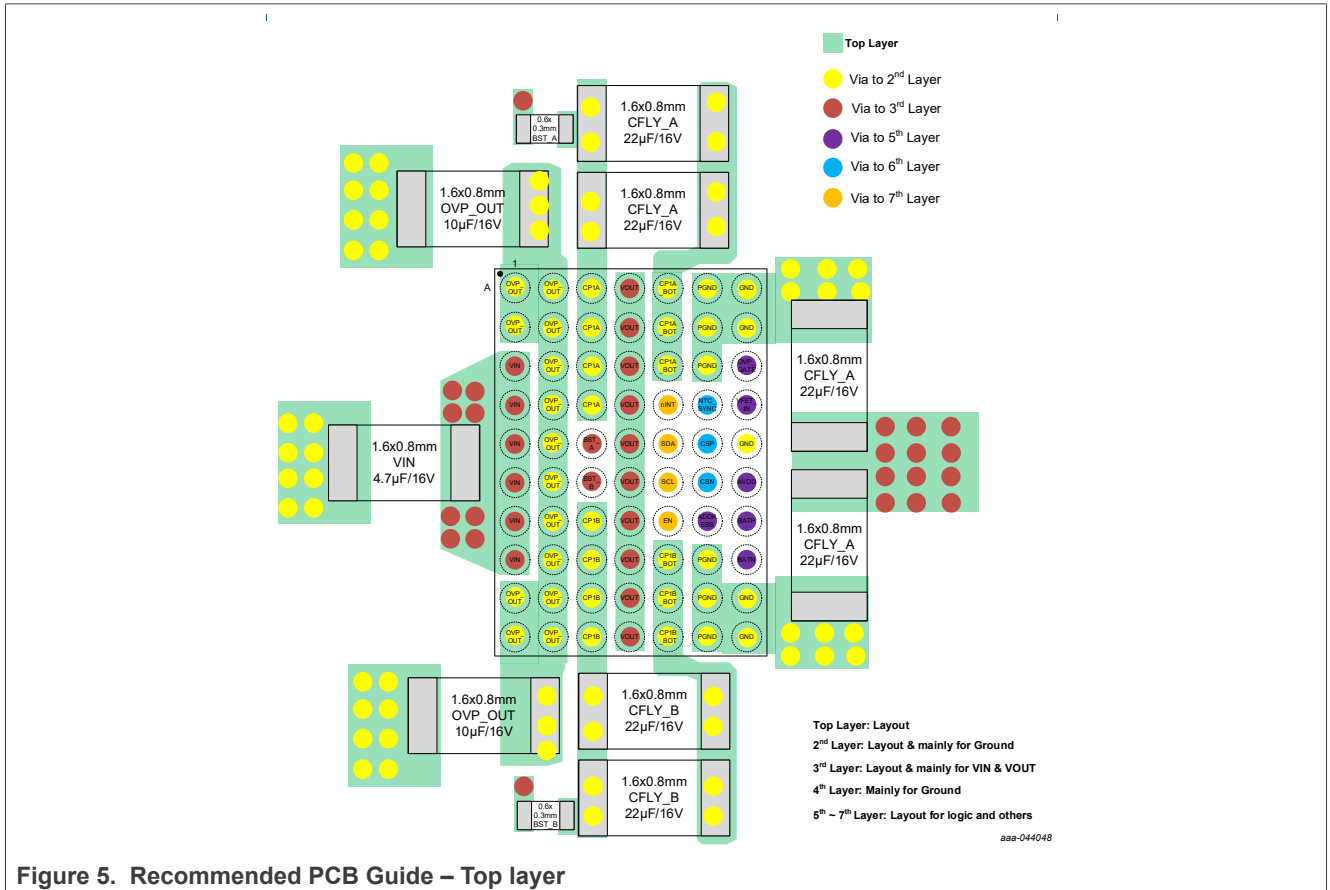


Figure 5. Recommended PCB Guide – Top layer



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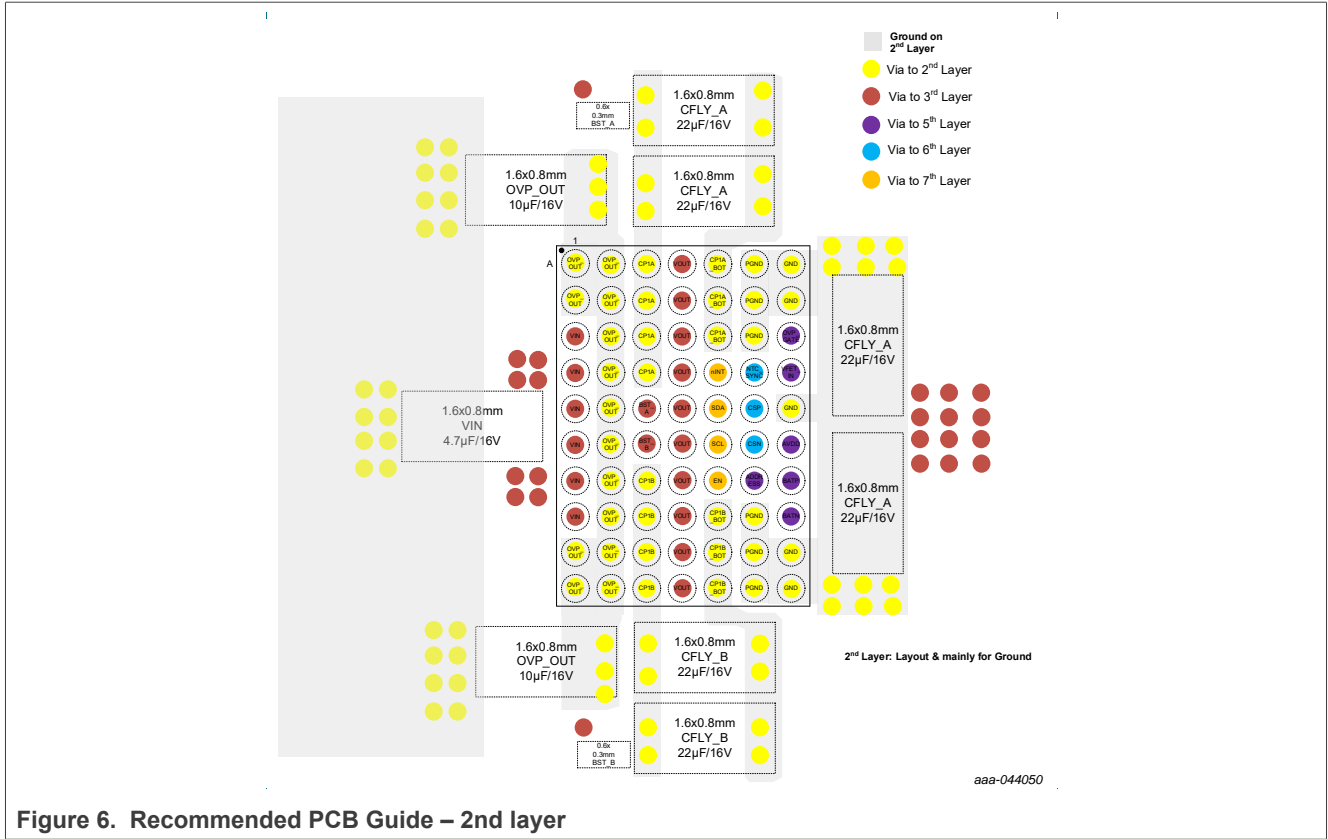


Figure 6. Recommended PCB Guide – 2nd layer

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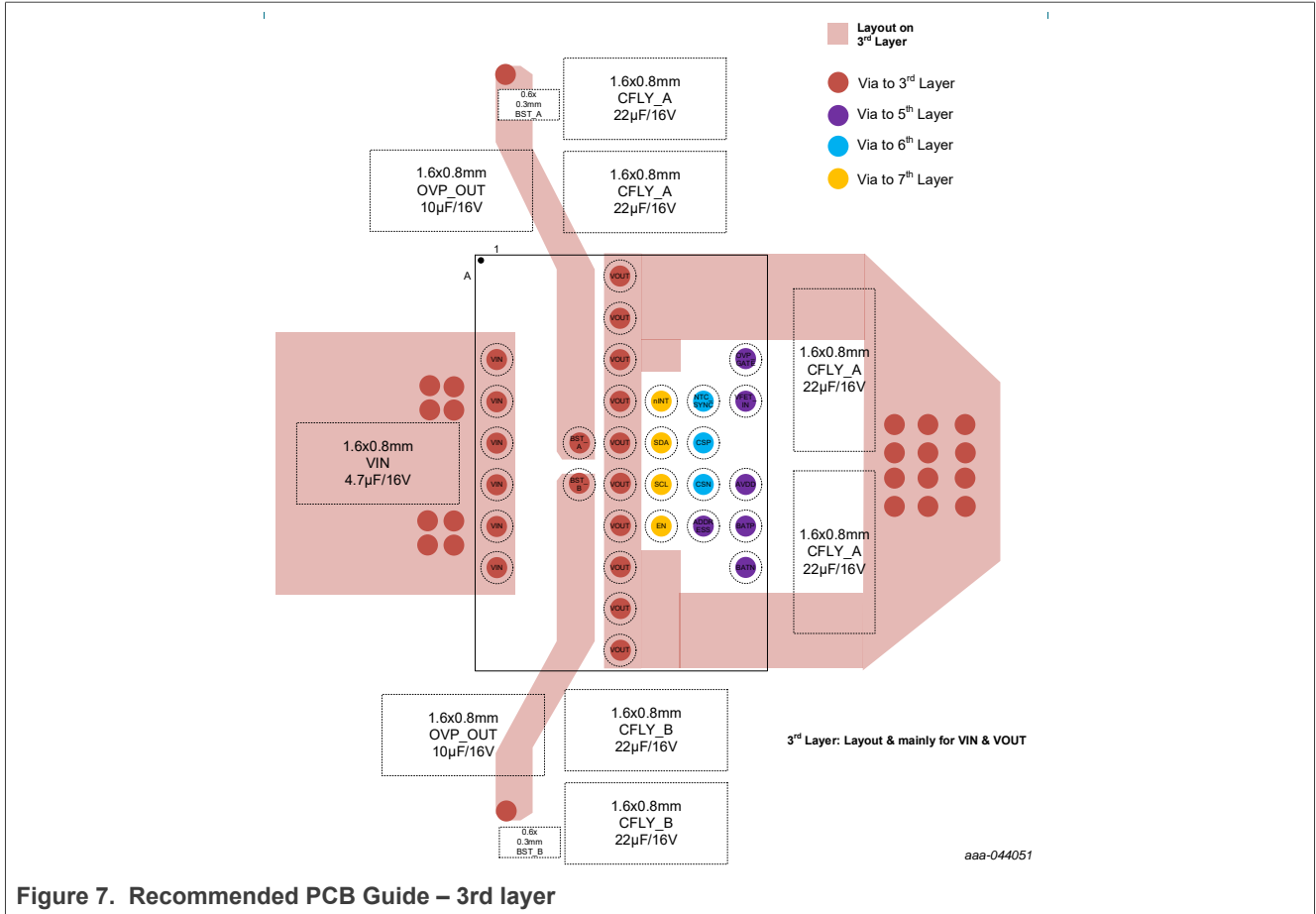


Figure 7. Recommended PCB Guide – 3rd layer

Revision history

Rev	Date	Description
v.2.3	20231120	<a href="#">Section 2.1</a> : "Output voltage of PCA9488 is 1.5x input voltage" corrected to "Output voltage of PCA9488 is 0.5x input voltage"; <a href="#">Section 5</a> moved to back of document to comply with NXPs document content standard
v.2.2	20230804	<a href="#">Section 3.5</a> : Added comment on min/max AVDD voltage
v.2.1	20230227	<a href="#">Section 3.3</a> : Added "nINT pin can be floating or open if not used."
v.2	20220718	Changed part number from PCA9481 to PCA9481A
v.1	20211020	Initial version

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