AN13367

i.MX 8M Nano Ultra Lite Power Consumption Measurement

Rev. 0 — 03 December 2021 Application Note

Contents

1 Introduction

This application note helps you design power management systems. It illustrates the current drain measurements of the i.MX 8M Nano Ultra Lite (UL) application processors taken on the NXP EVK platform through several use cases. You may choose the appropriate power supply domains for the i.MX 8M Nano processors and become familiar with the expected processor power consumption in various scenarios.

Because the data presented in this application note is based on empirical measurements taken on a small sample size, the presented results are not guaranteed.

2 Overview of i.MX 8M Nano UL voltage supplies

The i.MX 8M Nano UL processors have several power supply domains (voltage supply rails) and several internal power domains. Figure 1 shows the connectivity of these supply rails and the distribution of the internal power domains.

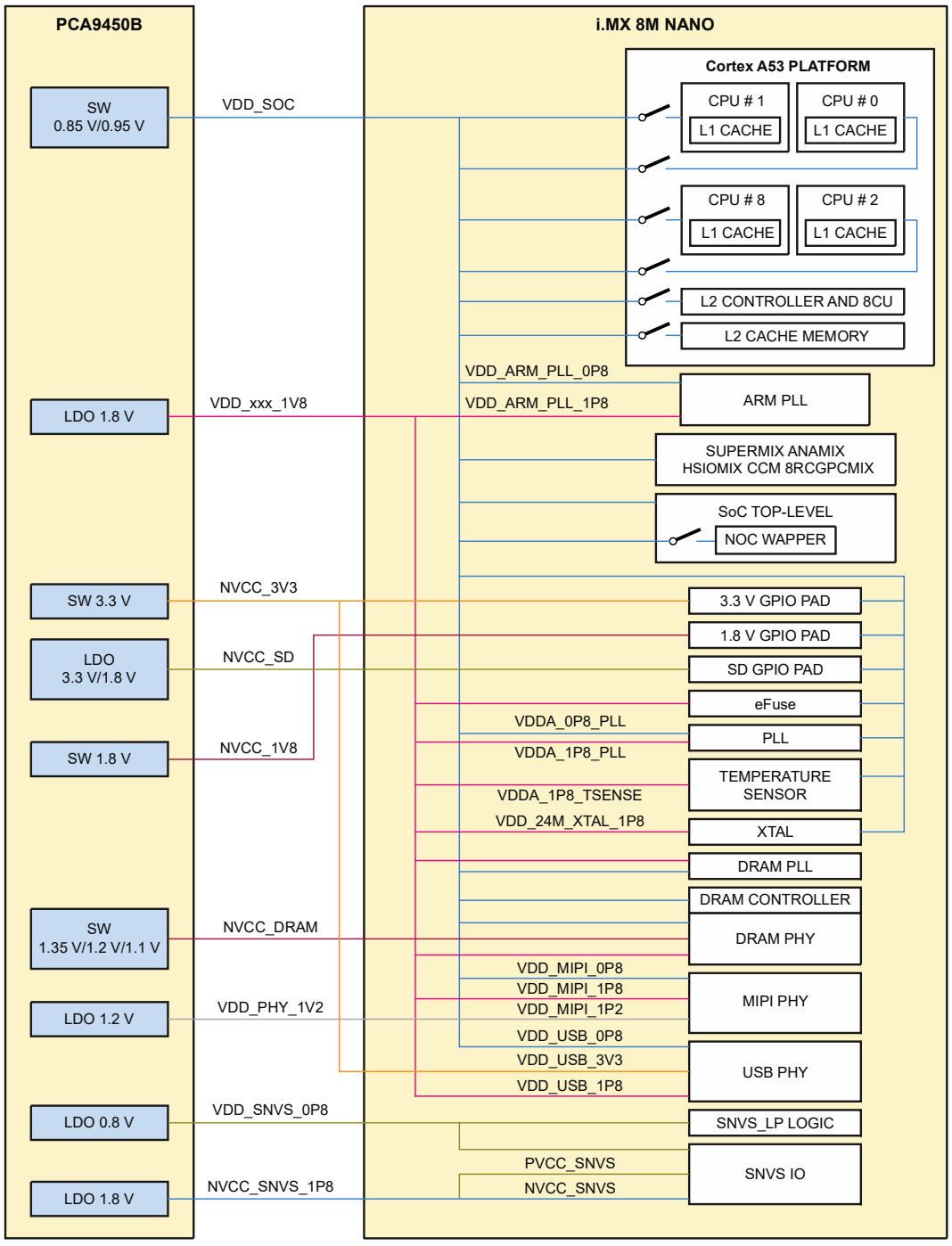

Figure 1. i.MX8M Nano UL power rails

NVCC_DRAM supplies both 8MN UL and DRAM parts. The power consumption data includes the DRAM IO power.

NOTE

For the recommended operating conditions of each supply rail and for a detailed description of the groups of pins that are powered by each I/O voltage supply, see the *i.MX 8M Nano data sheet for consumer products* (document IMX8MNCEC). For more information about the i.MX 8M Nano power rails, see the “Clocks and Power Management” section in the *i.MX 8M Nano Applications Processor Reference Manual* (document IMX8MNRM).

Figure 2 is a snippet from the i.MX 8M Nano UL DDR3L EVK Board schematic showing the power distribution.

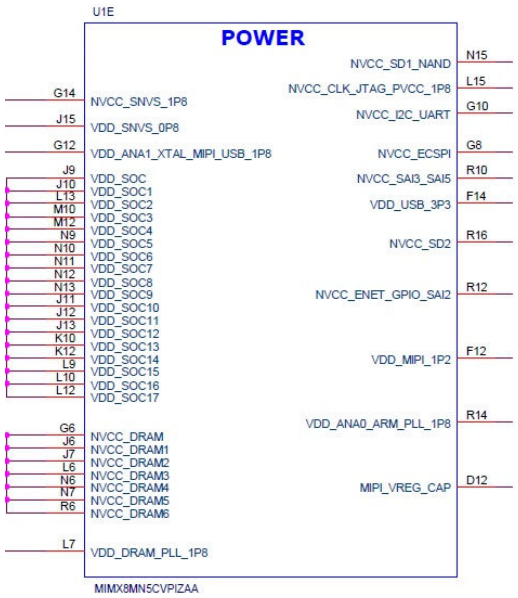

Figure 2. i.MX 8M Nano UL power schematic

3 Internal power measurement of the i.MX 8M Nano UL processor

Several use cases (described in Use-Case Configuration and Usage Guidelines) run on the EVK platform. The measurements are taken mainly for the following power-supply domains:

- VDD_SOC: Arm Cortex-A53 core supplies SoC logic, DRAM, PHY digital logic, and PLL power supply
- NVCC_DRAM: DRAM IO power supply (including an external DDR device)
- VDDA_1V8: 1.8 V power for Analog core

These supply domains consume the majority of the processor's internal power. For relevant use cases, the power of additional supply domains is added. However, the power of these supply domains does not depend on specific use cases, but on whether these modules are used or not. The power consumption of the SNVS is comparatively negligible (except for the Suspend mode).

The NVCC_* power consumption depends primarily on the board-level configuration and the components. Therefore, it is not included in the i.MX 8M Nano internal power analysis.

The power consumption of these supplies (in different use cases) is provided in Table 2 through to Table 30.

NOTE

Unless stated otherwise, all measurements were taken on a typical process silicon, at a room temperature (approximately 20 °C).

3.1 DDR I/O power

The DDR I/O is supplied from the NVCC_DRAM, which provides the power for the DDR I/O pads. The target voltage for this supply depends on the DDR interface used. The target voltages for the different DDR interfaces are:

- 1.35 V for DDR3L
- 1.2 V for DDR4
- 1.1 V for LPDDR4

The power consumption of the NVCC_DRAM supply is affected by various factors, including:

- The amount of activity on the DDR interface
- On-Die Termination (ODT): enabled/disabled, termination value, which is used for the DDR controller and the DDR memories
- Board termination for the DDR control and the address bus
- Configuration of the DDR pads (such as the drive strength)
- Board layout
- Load of the DDR memory devices

NOTE

Due to the factors specified in the previous paragraph, the measurements provided in the following tables vary from one system to another. The provided data is the average data but not the peak data. It is for guidance only and it should not be treated as a specification.

The measured current on the 8M Nano UL EVK Platform only includes the on-board DDR3L memory.

3.2 Voltage levels in the measurement process

The voltage levels of all the supplies (except for VDD_SOC) are set to typical voltage levels, as defined in the *i.MX 8M Nano Data Sheet for Consumer Products* (document IMX8MNCEC).

3.2.1 VDD_SOC voltage levels

The target voltage levels of the VDD_SOC may vary for different modes, according to the use cases. The modes are the nominal mode and the overdrive mode. There are several factors that contribute to the mode decisions, with the module load being the most important. The other factors are module latency requirements, thermal restrictions, and peripheral I/O performance requirements. The voltage levels used for the measurements are listed in Table 1.

Table 1. VDD_SOC voltage levels (for reference only)

Power rail	Vmin (V)	Vtyp (V)	Vmax (V)	Description
VDD_SOC	0.805	0.850	0.900	Nominal mode
	0.900	0.950	1.000	Overdrive mode

Most of the measurements are performed using these voltage levels and the power data that appears in this document is in accordance with these values. If the measurement is done at different voltage levels, the power consumption scales change with the voltage. In real applications, the software (with the hardware) automatically adjusts the voltage and frequency values based on the use case requirements.

The voltage used for the power calculation is the average voltage between those setpoints. It depends on the amount of time spent at each setpoint.

3.3 Temperature measurements

In some use cases, the die temperature is measured. The temperature measurements were done using the on-chip temperature sensor. When measuring the temperature, it is recommended to wait until the temperature stabilizes.

NOTE

The measured temperatures are for reference only and vary on different systems due to the differences in the board, enclosure, and heat spreading techniques. When using the same board type, the measured temperature may vary due to factors such as environment, silicon variations, and measurement errors.

3.4 Hardware and software used

The software versions used for the measurements are:

- i.MX 8M Nano UL DDR3L EVK Platform with the software release: L5.10.52_2.1.0.
- The measurements were performed using the 34470A 6½ digital multimeter.

3.5 Measuring points on the EVK platform

To measure the power consumption, do the rework first. Split the connection between the PMIC output inductor and the CPU and connect the NXP power consumption test tool in series. The power data is sampled by the tool and calculates the average current and power consumption.

4 Use cases and measurement results

The main use cases and subtypes that form the benchmarks for the i.MX 8M Nano UL internal power measurements on the EVK platform are described in the following sections.

NOTE

For all use cases, the platform boots from an SD card with the default dtb configuration in the U-Boot stage.

For the DDR3L EVK Board, check whether the default dtb file is *imx8mn-ddr3l-evk.dtb* for the DDR3L EVK Board: `printenv fdt_file`

If the default dtb file is not *imx8mn-ddr3l-evk.dtb*, set it as follows: `setenv fdt_file "imx8mn-ddr3l-evk.dtb" saveenv`

4.1 Low-power mode use cases

These use case scenarios were tested:

- Suspend mode
- IDLE_DEFAULT
- IDLE_DDRC_167MHz on DDR3L EVK Board

NOTE

For the DDR3L EVK Board, the IDLE_DDRC_167MHz sets the DDR PLL clock to 167 MHz and the DDR clock is 333 MHz. The DDR data rate is 2:1 for the DDR clock. For example, the DDR clock at 333 MHz means 666 MTS.

4.1.1 Suspend mode

This mode is called either “Dormant mode” or “Deep-sleep mode” in the Linux BSP. This is the lowest possible power state where the external supplies are still on.

The use case is as follows:

- The Arm platform is power-gated.
- The L2 cache peripherals are power-gated.
- The Arm Cortex-M7 is in the reset status.
- All PLL (Phase-Locked Loop) and CCM (Clock Controller Module) generated clocks are off.
- The CKIL (32 kHz) input is on.
- All modules are disabled.
- DDRC is in self-refresh status.

- The external high-frequency crystal and the on-chip oscillator are powered down (by asserting the SBYOS bit in the CCM).

Table 2 shows the measurement results when this use case is applied on the i.MX 8M Nano UL processor.

Table 2. Suspend mode

Supply Domain	L5.10.52_2.1.0		
	Voltage (V)	I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	14.6	19.7
VDDA_1V8	1.80	0.0	0.0
VDD_SOC_0V9	0.75	2.1	1.6
Total	-	-	21.28

NOTE

The die temperature was not logged, because it impacts the default governor (conservative) and sets the CPU clock frequency to 1.2 GHz.

For more details about this use case and settings, see Use-Case Configuration and Usage Guidelines.

4.1.2 IDLE_DEFAULT

The use case is as follows:

- The CPU frequency is set to 1200 MHz (default).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are off and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 3 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 3. IDLE_DEFAULT

Supply Domain	L5.10.52_2.1.0		
	Voltage (V)	I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	56.8	76.7
VDDA_1V8	1.80	11.4	20.5
VDD_SOC_0V9	0.85	282.3	240.3
Total			337.58
Die Avg Temperature (C)	-	-	40

For more details about this use case and settings, see Use-Case Configuration and Usage Guidelines.

4.1.3 IDLE_DDRC_167MHz on DDR3L EVK Board

The use case is as follows:

- The CPU frequency governor is set to `powersave` (the CPU frequency is set to the minimum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are off and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency is set to 167 MHz.

Table 4 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 4. IDLE_DDRC_167MHz for DDR3L EVK Board

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	43.1	58.2
VDDA_1V8	1.80	10.4	18.8
VDD_SOC_0V9	0.85	170.7	145.4
Total			222.44
Die Avg Temperature (C)	-	-	37

For more details about this use case and settings, see Use-Case Configuration and Usage Guidelines.

4.2 Audio_Playback

These use case scenarios were tested:

- Audio_Playback(gplay)
- Audio_Playback(gplay)_DDRC_167MHz on the DDR3L EVK Board

4.2.1 Audio_Playback(gplay)

The audio file used was an MP3 file with a 128-kbps bit rate and a 44-kHz sample rate, played using the following options:

```
gplay-1.0 $audio_file
```

The use case is as follows:

- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are off and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 5 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 5. Audio_Playback(gplay)

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	61.4	82.8
VDDA_1V8	1.80	13.3	23.9
VDD_SOC_0V9	0.85	293.6	249.8
Total			356.51
Die Avg Temperature (C)	-	-	41

1. The ambient temperature was approximately 20 ºC.

The *cat /sys/class/thermal/thermal_zone0/temp* was used to log the temperature while the audio file was playing.

For more details about this use case and settings, see Use-Case Configuration and Usage Guidelines.

4.2.2 Audio_Playback(gplay)_DDRC_167MHz on DDR3L EVK Board

For this use case, the DDRC clock frequency was set to 167 MHz, as specified in Use-Case Configuration and Usage Guidelines.

The audio file used was an MP3 file with a 128-kbps bit rate and a 44-kHz sample rate, played using the following option:

```
gplay-1.0 $audio_file
```

The use case is as follows:

- The CPU frequency governor is set to `powersave` (the CPU frequency is set to the minimum value).
- The Arm Cortex-A53 core is power-gated if the kernel is in the lowest level of idle.
- The Arm L2 cache and PLAT are powered on.
- The Arm Cortex-M7 is in the reset status.
- All the unused PLLs are OFF and the unused clocks are gated.
- The operating system is on.
- The DDRC frequency is set to 167 MHz.

Table 6 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 6. Audio_Playback(gplay)_DDRC_167MHz on DDR3L EVK Board

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	51.3	69.3
VDDA_1V8	1.80	12.4	22.3
VDD_SOC_0V9	0.85	202.4	172.6
Total			264.31
Die Avg Temperature(C)			39

1. The die temperature was approximately X °C (roughly). The ambient temperature was approximately 20 °C.

The *cat/sys/class/thermal/thermal_zone0/temp* was used to log the temperature while the audio file was playing.

4.3 Core benchmark

These use case scenarios were tested:

- 4-core Dhrystone
- 4-core Whetstone
- Coremark

4.3.1 4-core Dhrystone

Dhrystone is a synthetic benchmark used to measure the integer computational performance of processors and compilers. The small size of the Dhrystone benchmark enables it to fit into the L1 cache and minimizes accesses to the L2 cache and DDR.

In this use case, the Dhrystone test is performed by 4 Cortex-A53 cores (because Dhrystone is a single-thread benchmark, 4 instances were started). All Cortex-A53 cores ran the test in a loop at a frequency of 1400 MHz.

For the best performance, compile it as follows:

```
-Wall -O2 -fsigned-char -march=armv8-a -DPASS2
```

- The DDRC clock for DDR3L is 400 MHz.
- The NOC clock is 600 MHz.
- The AXI clock is 333 MHz.
- The AHB clock is 133 MHz.
- The IPG clock is 67 MHz.
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).

Table 7 shows the measurement results when this use case is applied on the i.MX 8M Nano UL processor.

Table 7. Dhrystone

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	55.1	74.4
VDDA_1V8	1.81	11.6	21
VDD_SOC_0V9	0.95	1186	1126.7
Total			1222.1
Die Avg Temperature(C)			61

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.3.2 4-core Whetstone

Whetstone is a benchmark similar to Dhrystone for integer and string operations. Whetstone is also a synthetic benchmark which primarily measures the floating-point arithmetic performance.

In this use case, the Whetstone test is performed by 4 Cortex-A53 cores (because Whetstone is a single-thread benchmark too, 4 instances were started). All Cortex-A53 cores run the test in a loop at a frequency of 1400 MHz.

For the best performance, compile it as follows:

```
-Wall -O2 -fsigned-char -march=armv8-a
```

- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC clock for DDR3L is 400 MHz.

Table 8 shows the measurement results when this use case is applied on the i.MX 8M Nano UL processor.

Table 8. Whetstone

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	55.9	75.4
VDDA_1V8	1.80	11.6	20.9
VDD_SOC_0V9	0.95	904	858.8
Total			955.1
Die Avg Temperature(C)			53

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.3.3 Coremark

Coremark is a modern, sophisticated benchmark that lets you accurately measure the processor performance and it is intended to replace the older Dhrystone benchmark. Arm recommends using Coremark over Dhrystone.

For the best performance, compile it as follows:

```
-O2 -DMULTITHREAD=4 -DUSE_PTHREAD  -lrt -lpthread
```

- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC clock for DDR3L is 400 MHz.

Table 9 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 9. Coremark

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	55.5	74.8
VDDA_1V8	1.80	11.7	21.1
VDD_SOC_0V9	0.95	971.6	923.02
Total			1018.92
Die Avg Temperature(C)			59

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.4 Memory

These use-case scenarios were tested:

- Memset

- Memcpy
- Stream

Memset and Memcpy are part of a perf-bench (a general framework for benchmark suites).

4.4.1 Memset

Memset is a suite for evaluating the performance of a simple memory set in various ways.

- The size of the memory buffers is set to 256 MB.
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 10 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 10. Memset

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.36	228.4	310
VDDA_1V8	1.80	11.6	20.9
VDD_SOC_0V9	0.96	511.1	491.8
Total			822.69
Die Avg Temperature(C)			48

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.4.2 Memcpy

Memcpy is a suite for evaluating the performance of a simple memory copy in various ways.

- The size of the memory buffers is set to 256 MB.
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 11 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 11. Memcpy

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.36	226.7	308
VDDA_1V8	1.80	11.6	20.9
VDD_SOC_0V9	0.96	515.3	495.4
Total			824.27
Die Avg Temperature(C)			48

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.4.3 Stream

The Stream benchmark is a simple synthetic benchmark program that measures the sustainable memory bandwidth (in MB/s) and the corresponding computation rate for simple vector kernels.

- The stream app release is L5.10.52_2.1.0.
- All phases are included (Copy, Scale, Add, and Triad).
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 12 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 12. Stream

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	131.4	177.6
VDDA_1V8	1.80	11.6	20.9
VDD_SOC_0V9	0.96	508.9	488.2
Total			686.68
Die Avg Temperature(C)			48

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.5 Storage – SD3.0 Card

These use-case scenarios were tested:

- DD_RD_SDCARD
- DD_WRT_SDCARD

4.5.1 DD_RD_SDCARD

- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.

(*echo 512 > /sys/block/<bdev>/queue/read_ahead_kb*)

- The DDRC frequency for DDR3L is set to 400 MHz.

Table 13 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 13. DD_RD_SDCARD

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	94.9	128.2
VDDA_1V8	1.80	11.4	20.6
VDD_SOC_0V9	0.86	371.2	319

Table continues on the next page...

Table 13. DD_RD_SDCARD (continued)

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
Total			467.85
Die Avg Temperature(C)			43

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.5.2 DD_WRT_SDCARD

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 14 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 14. DD_WRT_SDCARD

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	63.4	85.5
VDDA_1V8	1.80	11.4	20.6
VDD_SOC_0V9	0.85	311.5	265.8
Total			371.95
Die Avg Temperature(C)			43

1. The ambient temperature is approximately 20 ^{0}C.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.6 Storage – eMMC

These use-case scenarios were tested:

- DD_RD_eMMC
- DD_WRT_eMMC

4.6.1 DD_RD_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.
- (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 15 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 15. DD_RD_eMMC

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	126.2	170.6
VDDA_1V8	1.80	11.6	20.9
VDD_SOC_0V9	0.96	518	497.9
Total			689.44
Die Avg Temperature(C)			49

1. The ambient temperature is approximately 20 ^{0}C.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.6.2 DD_WRT_eMMC

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.
- (*echo 512 > /sys/block/<bdev>/queue/read_ahead_kb*)
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 16 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 16. DD_WRT_eMMC

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	124.8	168.6
VDDA_1V8	1.80	11.5	20.8
VDD_SOC_0V9	0.94	546.3	514.1
Total			703.45
Die Avg Temperature(C)			51

1. The ambient temperature is approximately 20 ^{0}C.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.7 Storage – USB 2.0

These use-case scenarios were tested:

- DD_RD_USB2.0
- DD_WRT_ USB2.0

4.7.1 DD_RD_USB2.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.
- (*echo 512 > /sys/block/<bdev>/queue/read_ahead_kb*)
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).

- The DDRC frequency for DDR3L is set to 400 MHz.

Table 17 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 17. DD_RD_ USB2.0

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	79.3	107.2
VDDA_1V8	1.80	16.9	30.5
VDD_SOC_0V9	0.85	344.1	293.8
Total			431.47
Die Avg Temperature(C)			44

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

4.7.2 DD_WRT_ USB2.0

- Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB. (`echo 512 > /sys/block/<bdev>/queue/read_ahead_kb`)
- The CPU frequency governor is set to `performance` (the CPU frequency is set to the maximum value).
- The DDRC frequency for DDR3L is set to 400 MHz.

Table 18 shows the measurement results when this use case is applied on the i.MX 8M Nano processor.

Table 18. DD_WRT_USB2.0

Supply Domain	Voltage (V)	L5.10.52_2.1.0	
		I (mA)	P (mW)
NVCC_DRAM_1V35	1.35	81.7	110.3
VDDA_1V8	1.80	19.3	34.8
VDD_SOC_0V9	0.85	339.5	289.8
Total			434.92
Die Avg Temperature(C)			44

1. The ambient temperature is approximately 20 ºC.

cat /sys/class/thermal/thermal_zone0/temp was used to log the temperature while the benchmark was running.

5 Reducing power consumption

The overall system power consumption depends on both the software optimization and how the system hardware is implemented. The following is a list of suggestions that may help to reduce the system power consumption:

- Apply the clock gating whenever the clocks or modules are not used by configuring the CCGR registers in the Clock Controller Module (CCM).
- Reduce the number of operating PLLs. This is applicable mainly in the Audio_Playback or Idle modes.

The core DVFS and system bus scaling are as follows: Applying the DVFS for Arm and scaling the frequencies of the NOC, AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of the VDD_SOC domains.

Additionally, due to a reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memory. This trade-off must be recognized for each mode to quantify the overall effect on the system power consumption.

- Put the i.MX 8M Nano into the low-power modes (STOP) whenever possible. See the “Clock Controller Module (CCM)” section in the *i.MX 8M Nano Applications Processor Reference Manual* (document IMX8MNRM) for details.
- DDR interface optimization:
  - Employ a careful board routing of the DDR memories, maintaining the PCB trace lengths as short as possible.
  - Use as increased ODT (On-Die Termination) setting as possible. The termination used greatly influences the power consumption of the DDR interface pins.
  - Use a proper output driver impedance for the DDR interface pins that provide good impedance matching. Select the lowest possible drive strength that provides the required performance to reduce the current flowing through the DDR I/O pins.
  - The use of the DDR memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

The various steps are shown below.

NOTE

All the programming steps below are performed in the Arm trusted firmware from the internal RAM.

5.1 Steps to be performed before entering Suspend (Deep-sleep) mode

1. Read the DBGCAM register in DDRC to make sure that the explicit transaction command queue is empty. Wait until the AXI port is idle.
2. Do the following:
   a. Put the DDR into self-refresh.
   b. Transition the DDR PHY into the LP3/IO retention state using the DFI frequency operation.
   c. Set the PwrOkIn signal in SRC to 0. This enables the data retention feature on the CKE and MEMRESET.
   d. Gate the DDRC’s CORE clock and APB clock.
   e. Enable the DDRMIX ISO to power-gate the DDRC and PHY.
3. Enter the Suspend mode.

5.2 Steps to be performed after exiting Suspend mode

1. Restore all the settings for the DDRC and PHY to the required values.
2. The system proceeds to the Run mode.

6 Use-case configuration and usage guidelines

NOTE

Before running a use case, run the *<configuration_script>.sh* scripts to configure the environment. These are *setup.sh, setup_default.sh, setup_video.sh*. See Important commands for details.

6.1 Suspend mode

In this use case, all clocks and PLLs are turned off, except for the 32 kHz clock, which is used to wake up the system.

1. Boot up the Linux image.
2. Run this command to put the system into the DSM mode:

```
echo mem > /sys/power/state
```

3. Measure the power and record the result.

6.2 System Idle mode

NOTE

No display was connected to the platform.

6.2.1 IDLE_DEFAULT

6.2.1.1 Clock configuration

The clock configuration in Table 19 is aligned with the L5.10.52_2.1.0 release.

Table 19. IDLE_DEFAULT clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1200
DDRC	400 for DDR3L EVK

6.2.1.2 PLL configuration

The PLL configuration in Table 20 is aligned with the L5.10.52_2.1.0 release.

Table 20. IDLE_DEFAULT PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1200
NOC	SYS_PLL3_OUT	600
MAIN_AXI	SYS_PLL2_333M	333
NAND_USDHC_BUS	SYS_PLL1_266M	266
AHB	SYS_PLL1_133M	133
IPG_ROOT	AHB_CLK_ROOT	67
DRAM_PLL	DRAM_PLL_REF	400
USDHC2	SYS_PLL1_400M	200
WDOG	OSC_24M	24
UART2	SYS_PLL1_400M	24

6.2.1.3 System setup

Disconnect everything except for the SD card.

Make sure that there are no displays connected to the platform.

1. Boot up the Linux OS.
2. Run *setup_default.sh* (see Important commands) to put the system to the system Idle mode.
3. Measure the power and record the result.

6.2.2 IDLE_DDRC_167MHz for DDR3L EVK Board

6.2.2.1 Clock configuration

The clock configuration in Table 21 is aligned with release L5.10.52_2.1.0.

Table 21. IDLE_DDRC_167MHz clock configuration

Clock name	Frequency (MHz)
NOC	120
AXI	24
AHB	22.2
CPU	1200
DDRC	167

6.2.2.2 PLL configuration

The PLL configuration in Table 22 is aligned with release L5.10.52_2.1.0.

Table 22. IDLE_DDRC_167MHz PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1200
NOC	SYS_PLL3_OUT	120
MAIN_AXI	SYS_PLL2_333M	24
AHB	SYS_PLL1_133M	22.2
IPG_ROOT	AHB_CLK_ROOT	11.1
DRAM_PLL	DRAM_PLL_REF	167
WDOG	OSC_24M	24
UART2	OSC_24M	24

6.2.2.3 System setup

Disconnect everything except for the SD card.

Make sure that there are no displays connected to the platform.

1. Boot up the Linux OS.

2. Run *DDRC_167MHz_setup.sh* (see Important commands) to put the system to the system idle mode.
3. Measure the power and record the result.

6.3 Audio_Playback

6.3.1 Clock configuration

The clock configuration in Table 23 is aligned with release L5.10.52_2.1.0.

Table 23. Audio_Playback clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1200
DDRC	400 for DDR3L

6.3.2 PLL configuration

The PLL configuration in Table 24 is aligned with release L5.10.52_2.1.0.

Table 24. Audio_Playback PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1200
NOC	SYS_PLL3_OUT	600
MAIN_AXI	SYS_PLL2_333M	333
NAND_USDHC_BUS	SYS_PLL1_266M	266
AHB	SYS_PLL1_133M	133
IPG_ROOT	AHB_CLK_ROOT	67
DRAM_PLL	DRAM_PLL_REF	400
USDHC2	SYS_PLL1_400M	200
SAI2	AUDIO_PLL1	24.576
UART2	SYS_PLL1_400M	24

6.3.3 Audio_Playback(gplay)

The audio file used was an MP3 file with a 128-kbps bit rate and a 44-kHz sample rate, played using the following options:

1. Boot up the Linux OS.
2. Run *setup_default.sh* (see Important commands).
3. Run *gplay_audio.sh* and measure:

```
audio_file='Mpeg1L3_44kHz_128kbps_s_Ed_Rush_Sabotage_mplayer.mp3'
gplay-1.0 $audio_file
```

4. Start the die temperature recording (see Important commands).
5. Measure the power and record the result.

6.3.4 Audio_Playback(gplay)_DDRC_167MHz on DDR3L EVK Board

The audio file used was an MP3 file with a 128-kbps bit rate and a 44-kHz sample rate, played using the following options:

1. Boot up the Linux OS.
2. Run *DDRC_167MHz_setup.sh* (see Important commands).
3. Run *gplay_audio.sh* and measure:

```
audio_file='Mpeg1L3_44kHz_128kbps_s_Ed_Rush_Sabotage_mplayer.mp3'
gplay-1.0 $audio_file
```

4. Start the die temperature recording (see Important commands).
5. Measure the power and record the result.

6.4 Core benchmark

NOTE

No display was connected to the platform.

6.4.1 Clock configuration

The clock configuration in Table 25 is aligned with release L5.10.52_2.1.0.

Table 25. Core benchmark tests clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1400
DDRC	400 for DDR3L

6.4.2 PLL configuration

The PLL configuration in Table 26 is aligned with release L5.10.52_2.1.0.

Table 26. Core benchmark tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1400
NOC	SYS_PLL3_OUT	600

Table continues on the next page...

Table 26. Core benchmark tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
MAIN_AXI	SYS_PLL2_333M	333
AHB	SYS_PLL1_133M	133
IPG_ROOT	AHB_CLK_ROOT	66.7
DRAM_PLL	DRAM_PLL_REF	400
WDOG	OSC_24M	24
UART2	OSC_24M	24

6.4.3 Core Dhrystone

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run *setup.sh* (see Important commands).
3. Run *dhrystone_loop.sh* and measure:

```
while [ "1" == "1" ]
do
sudo taskset -c 0 ./dhrystone/gcc_dry2 &
sudo taskset -c 1 ./dhrystone/gcc_dry2 &
sudo taskset -c 2 ./dhrystone/gcc_dry2 &
sudo taskset -c 3 ./dhrystone/gcc_dry2
done
```

4. Start the die temperature recording (see Important commands).
5. Measure the power and record the result.

6.4.4 Core Whetstone

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run *setup.sh* (see Important commands).
3. Run *whetstone_loop.sh* and measure:

```
while [ "1" == "1" ]
do
sudo taskset -c 0 ./whetsSP &
sudo taskset -c 1 ./whetsSP &
sudo taskset -c 2 ./whetsSP &
sudo taskset -c 3 ./whetsSP
done
```

4. Start the die temperature recording (see Important commands).
5. Measure the power and record the result.

6.4.5 Coremark

1. Boot up the Linux image and boot the board to the SD rootfs.
2. Run *setup.sh* (see Important commands).

3. Run *Coremark_loop.sh* and measure:

```
while true; do
 ./Coremark.exe > /dev/null 2>&1
done
```

4. Start the die temperature recording (see Important commands).
5. Measure the power and record the result.

6.5 Memory

NOTE

No display was connected to the platform.

Three use cases were used for the power measurements. Before running a benchmark, the governor must be set to `performance` (see Important commands):

```
cpufreq-set -g performance
```

```
echo 1 > /sys/class/graphics/fb0/blank
```

After setting the governor, run the respective use case in a loop and start the power measurements and temperature logging at the desired time interval (1 minute is recommended) according to Important commands.

6.5.1 Clock configuration

The clock configuration in Table 27 is aligned with release L5.10.52_2.1.0.

Table 27. Memory tests clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1400
DDRC	400 for DDR3L

6.5.2 PLL configuration

The PLL configuration in Table 28 is aligned with release L5.10.52_2.1.0.

Table 28. Memory tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1400
NOC	SYS_PLL3_OUT	600
MAIN_AXI	SYS_PLL2_333M	333
AHB	SYS_PLL1_133M	133

Table continues on the next page...

Table 28. Memory tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
IPG_ROOT	AHB_CLK_ROOT	66.7
DRAM_PLL	DRAM_PLL_REF	400
WDOG	OSC_24M	24
UART2	OSC_24M	24

6.5.3 Memset

1. Run *setup.sh* (see Important commands).
2. Run *memset_loop.sh*:

```
while true; do
perf bench -f simple mem memset -l 20000 -s 256000KB
done
```

3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

6.5.4 Memcpy

1. Run *setup.sh* (see Important commands).
2. Run *memcpy_loop.sh*:

```
while true; do
perf bench -f simple mem memcpy -l 20000 -s 256000KB
done
```

3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

6.5.5 Stream

Make sure stream libraries are added to *LD_LIBRARY_PATH.*

1. Run *setup.sh* (see Important commands).
2. Run *streamcpy_loop.sh*:

```
export LD_LIBRARY_PATH=`pwd`:$LD_LIBRARY_PATH
while true; do
./stream
done
```

3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

6.6 Storage – SD3.0 card

An SD card was used to run the benchmarks.

6.6.1 Clock configuration

The clock configuration in Table 29 is aligned with release L5.10.52_2.1.0.

Table 29. SD3.0 card tests clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1200
DDRC	400 for DDR3L

6.6.2 PLL configuration

The PLL configuration in Table 30 is aligned with release L5.10.52_2.1.0.

Table 30. SD3.0 card tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1200
NOC	SYS_PLL3_OUT	600
MAIN_AXI	SYS_PLL2_333M	333
AHB	SYS_PLL1_133M	133
IPG_ROOT	AHB_CLK_ROOT	66.7
DRAM_PLL	DRAM_PLL_REF	400
WDOG	OSC_24M	24
UART2	OSC_24M	24
USDHC2	SYS_PLL1_400M	200
NAND_USDHC_BUS	SYS_PLL1_266M	266
I2C1	OSC_24M	24

6.6.3 DD_RD_SDCARD

1. Run *setup.sh* (see Important commands).
2. Copy *dd_read_SD10.sh* on the SD card partition and run it (see below).
3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

```
#!/bin/sh
emmc_index=$(ls /dev/mmc*rpmb | head -1 | awk -F '/dev/mmcblk' '{print $2}' | awk -F 'rpmb' '{print
$1}')
emmc_device=mmcblk$emmc_index
sd_device=$(cat /proc/partitions | grep mmcblk | grep -vi "p" | grep -vi "$emmc_device" | tail -n 1 |
```

```
awk '{print $4}')
i=0
while true; do
    time -p dd if=/dev/$sd_device of=/dev/null bs=4096 count=1024000
done
```

6.6.4 DD_WRT_SDCARD

1. Run *setup.sh* (see Important commands).
2. Copy *dd_write_SD10.sh* on the SD card partition and run it (see below).
3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

```
#!/bin/bash
#!/bin/sh
emmc_index=$(ls /dev/mmc*rpmb | head -1 | awk -F '/dev/mmcblk' '{print $2}' | awk -F 'rpmb' '{print
$1}')
emmc_device=mmcblk$emmc_index
sd_device=$(cat /proc/partitions | grep mmcblk | grep -vi "p" | grep -vi "$emmc_device" | tail -n 1 |
awk '{print $4}')
i=0
while true; do
    time -p dd if=/dev/zero of=/dev/$sd_device bs=4096 seek=2621440 count=1024000 conv=fsync
done
```

6.7 Storage – eMMC

A partition was created on the eMMC and benchmarks were run on it. For the eMMC test clock and PLL configuration, see Table 32.

6.7.1 Clock configuration

The clock configuration in Table 31 is aligned with release L5.10.52_2.1.0.

Table 31. eMMC Tests Clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1400
DDRC	400

6.7.2 PLL configuration

The PLL configuration in Table 32 is aligned with release L5.10.52_2.1.0.

Table 32. eMMC Tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1400

Table continues on the next page...

Table 32. eMMC Tests PLL configuration (continued)

Clock root	Source selected	Frequency (MHz)
NOC	SYS_PLL3_OUT	600
MAIN_AXI	SYS_PLL2_333M	333
AHB	SYS_PLL1_133M	133
IPG_ROOT	AHB_CLK_ROOT	66.7
DRAM_PLL	DRAM_PLL_REF	400
WDOG	OSC_24M	24
UART2	OSC_24M	24
USDHC2	SYS_PLL1_400M	200
USDHC3	SYS_PLL1_400M	400
NAND_USDHC_BUS	SYS_PLL1_266M	266

6.7.3 DD_RD_eMMC

1. Run setup.sh (see Important commands).
2. Copy dd_read_emmc.sh on the "sdcard rootfs" and run it.
3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

```
#!/bin/sh
emmc_index=$(ls /dev/mmc*rpmb | head -1 | awk -F '/dev/mmcblk' '{print $2}' | awk -F 'rpmb'
'{print $1}')
while true; do
time -p dd if=/dev/mmcblk${emmc_index} of=/dev/null bs=4096 count=1024000
done
```

6.7.4 DD_WRT_eMMC

1. Run setup.sh (see Important commands).
2. Copy dd_write_emmc.sh on the "sdcard rootfs" and run it.
3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

```
#!/bin/sh
emmc_index=$(ls /dev/mmc*rpmb | head -1 | awk -F '/dev/mmcblk' '{print $2}' | awk -F 'rpmb'
'{print $1}')
while true; do
time -p dd if=/dev/zero of=/dev/mmcblk${emmc_index} bs=4096 seek=2621440 count=1024000
conv=fsync
done
```

6.8 Storage – USB2.0

A USB 2.0 was used to run the benchmarks.

6.8.1 Clock configuration

The clock configuration in Table 33 is aligned with release L5.10.52_2.1.0.

Table 33. USB 2.0 partitions tests clock configuration

Clock name	Frequency (MHz)
NOC	600
AXI	333
AHB	133
CPU	1200
DDRC	400 for DDR3L EVK

6.8.2 PLL configuration

The PLL configuration in Table 34 is aligned with release L5.10.52_2.1.0.

Table 34. USB 2.0 partitions tests PLL configuration

Clock root	Source selected	Frequency (MHz)
ARM_PLL	ARM_PLL_REF	1200
NOC	SYS_PLL3_OUT	600
MAIN_AXI	SYS_PLL2_333M	333
AHB	SYS_PLL1_133M	133
IPG_ROOT	AHB_CLK_ROOT	66.7
DRAM_PLL	DRAM_PLL_REF	400
WDOG	OSC_24M	24
UART2	OSC_24M	24
USDHC2	SYS_PLL1_400M	200
USB_BUS	SYS_PLL2_500M	500
USB_PHY_REF	SYS_PLL1_100M	100
NAND_USDHC_BUS	SYS_PLL1_266M	266
I2C1	OSC_24M	24

6.8.3 DD_RD_USB2.0

1. Run *setup.sh* (see Important commands).
2. Copy *dd_read_usb.sh* on the "sdcard rootfs" and run it.
3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

```
#!/bin/sh
umount /dev/sda
```

```
while true; do
    time -p dd if=/dev/sda of=/dev/null bs=4096 count=1024000
done
```

6.8.4 DD_WRT_USB2.0

1. Run *setup.sh* (see Important commands).
2. Copy *dd_write_usb.sh* on the "sdcard rootfs" and run it.
3. Start the die temperature recording (see Important commands).
4. Start the power measurement and record the data.

```
#!/bin/sh
umount /dev/sda
while true; do
    time -p dd if=/dev/zero of=/dev/sda bs=4096 seek=4096 count=1024000 conv=fsync
done
```

6.9 Important commands

1. Before running a use case, run the *<configuration_script>.sh* scripts to configure the environment. These are *setup.sh, setup_default.sh,* and *DDRC_167MHz_setup.sh* (see below).
   - *setup.sh:* The CPU frequency is set to the maximum value (1400 MHz) to achieve the best performance. Disable the Ethernet, stop the Weston service, and blank the display. Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.

     ```
     #!/bin/bash
     systemctl stop weston.service
     cpufreq-set -g performance
     echo 1 > /sys/class/graphics/fb0/blank
     partitions=`lsblk |awk '$1 !~/-/{print $1}' |grep 'blk\|sd'`
     for partition in $partitions; do
             echo 512 > /sys/block/$partition/queue/read_ahead_kb
     done
     eth_int=`ifconfig -a|grep 'eth'|awk {'print $1'}`
     for eth in $eth_int;do
      ifconfig $eth down
     done
     ```

   - *setup_default.sh*: The CPU frequency is set to the default value (1200 MHz). Disable the Ethernet, stop the Weston service, and blank the display. Set the maximum amount of data that the kernel reads ahead for a single file to 512 kB.

     ```
     #!/bin/bash
     systemctl stop weston.service
     echo 1 > /sys/class/graphics/fb0/blank
     partitions=`lsblk |awk '$1 !~/-/{print $1}' |grep 'blk\|sd'`
     for partition in $partitions; do
             echo 512 > /sys/block/$partition/queue/read_ahead_kb
     done
     eth_int=`ifconfig -a|grep 'eth'|awk {'print $1'}`
     for eth in $eth_int;do
      ifconfig $eth down
     done
     ```

- *DDRC_167MHz_setup.sh* is used on the DDR3L EVK Board. After running the below shell scripts, you see in the logs that the DDRC frequency switches between the high bus mode (600 MHz) and the low bus mode (167 MHz) due to the DDR DVFS. The CPU frequency is set to the minimum value (1200 MHz). Both the DDR DVFS and CPU powersave aim at saving power. Disable the Ethernet, stop the Weston service, and blank the display.)

```
#!/bin/bash
systemctl stop weston.service
echo 1 > /sys/class/graphics/fb0/blank
cpufreq-set -g powersave
rmmod brcmfmac
#echo 8 > /proc/sys/kernel/printk;
eth_int=`ifconfig -a|grep 'eth\|can\|sit'|awk {'print $1'}`
for eth in $eth_int;do
 ifconfig $eth down
done
sleep 5
```

2. In the U-Boot console:
   - `printenv` displays the environment variables.
   - `setenv` updates the environment variables.
   - `setenv <name> <value> ...` sets the environment variable “name” to “value ...”.
   - `setenv <name>` deletes the environment variable “name”.
   - `saveenv` saves the updates to the environment variables.
   - `bootargs` passes the kernel command lines to the kernel.
3. In the Linux OS console:
   - `cat /proc/cmdline` displays the command line.
   - `cat /sys/devices/virtual/thermal/thermal_zone0/temp` displays the temperature on the screen (the chip should be calibrated).

     NOTE

     The die temperature value was logged (written) externally (not on the SD card) for not impacting power consumption.
4. `cat /sys/kernel/debug/clk/clk_summary` displays all clocks on the screen.

7 Revision history

Table 35 summarizes the changes done to this document since the initial release.

Table 35. Revision history

Revision number	Date	Substantive changes
0	03 December 2021	Initial release

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