AN13162

i.MX RT500 Power Managment

Rev. 0 — 02/2021

Application Note

1 Introduction

The i.MX RT500 family offers a rich set of peripherals and very low power consumption. This application note describes how to use the power management in i.MX RT500. This document does not replace the datasheet or the reference manual.

Contents

2 Power rails

Figure 1 shows a high-level diagram with some of the power domains in the i.MX RT500.

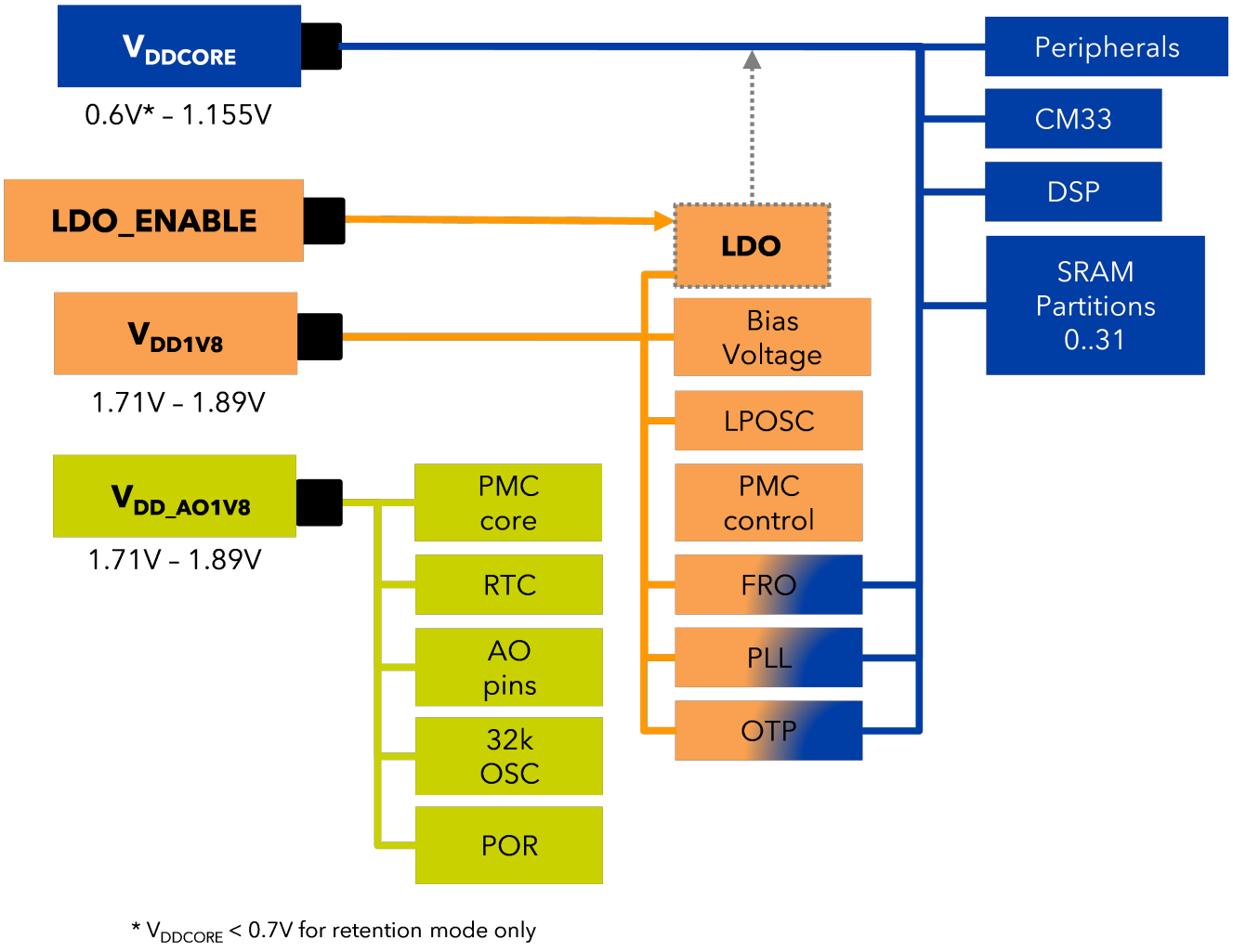

Figure 1. i.MX RT500 power domains

2.1 VDDCORE

V_{DDCORE} is the input supply for the core logic, DSP, peripherals, and memories.

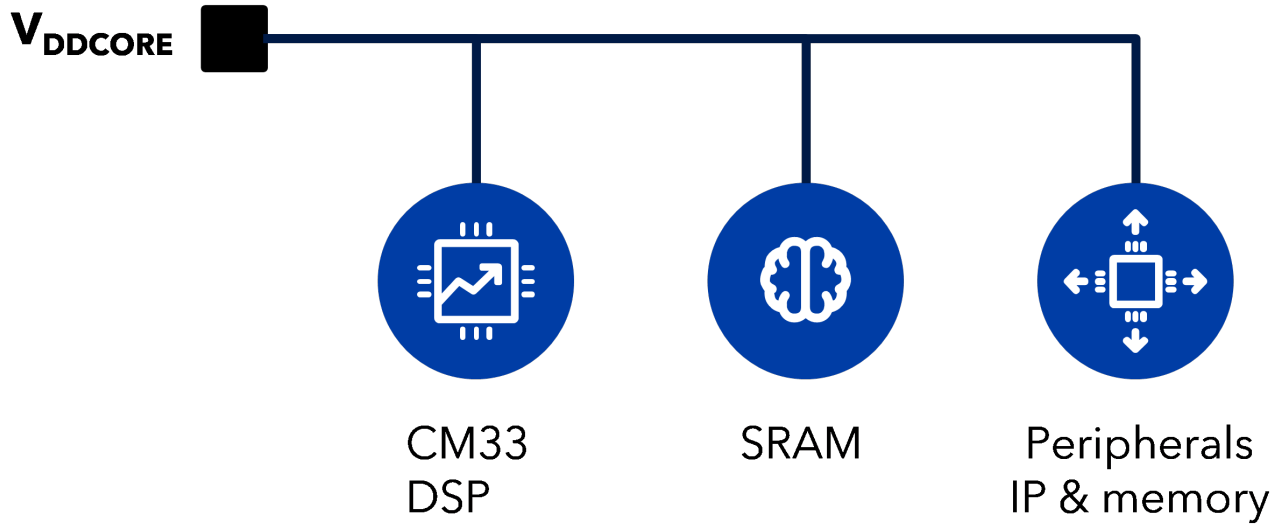

Figure 2. V_{DDCORE} loads

V_{DDCORE} has adjustable voltage from 0.6 V to 1.15 V. The minimum V_{DDCORE} voltage level in the active mode is determined by the core frequency before the CPU clock divider, as shown in Table 1. V_{DDCORE} voltages below 0.7 V are for retention mode only.

Table 1. - min V_{DDCORE} voltage in active mode

Frequency	min V_{DDCORE}
60 MHz	0.7 V
100 MHz	0.8 V
192 MHz	0.9 V
230 MHz	1.0 V
275 MHz	1.1 V

Although the i.MX RT500 low-power target frequency is 200 MHz, it can operate at up to 275 MHz. However, the higher frequency increases the current consumption.

2.2 VDD1V8

2.2.1 VDD1V8

VDD1V8 is a 1.8 V voltage supply for on-chip analog functions other than the ADC and comparator. It is the power supply for the Power Management Controller (PMC) module; that includes bandgap, POR, temperature sensor, and core low-voltage and high-voltage detection.

2.2.2 VDD1V8_1

V_{DD1V8} provides the 1.8 V voltage supply for the on-chip digital logic.

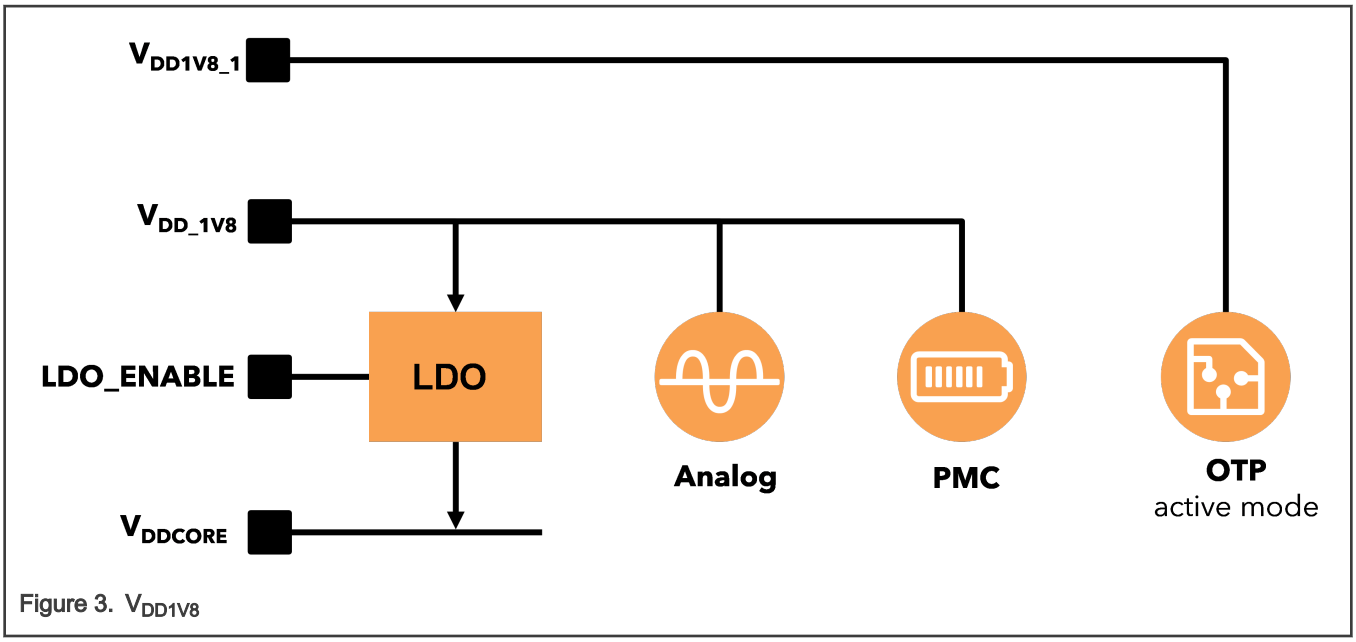

Figure 3. V_{DD1V8}

2.3 VDD_AO1V8

The always-on power domain powered by V_{DD_AO1V8} includes the RTC, always-on POR, and the RESET, LDO_ENABLE, PMIC_IRQ, PMIC_MODE0, and PMIC_MODE1 pins.

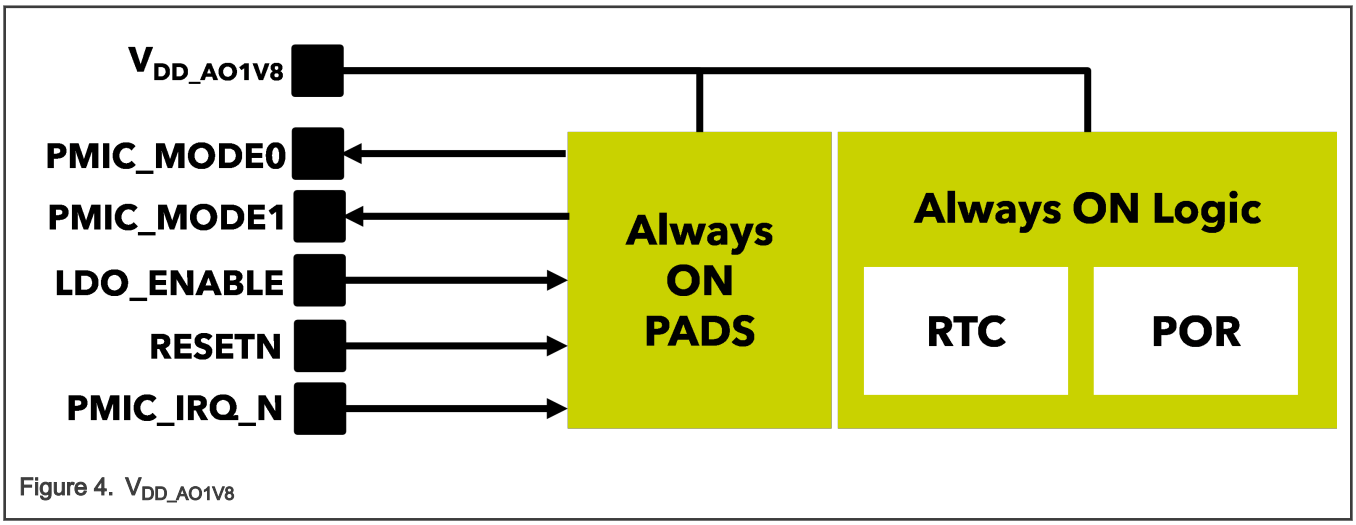

Figure 4. V_{DD_AO1V8}

2.4 VDD_IO

2.4.1 VDDIO_0 VDDIO_1 VDDIO_2 VDDIO_4

These GPIOs provide a supply voltage of up to 1.8 V.

2.4.2 VDDIO_3

This GPIO provides a supply voltage of up to 3.6 V.

3 i.MX RT500 power modes

The i.MX RT500 module implements five basic power modes: Active, Sleep, Deep Sleep, Deep Powerdown, and Full Powerdown.

The following sections explain the difference between the power modes using the following decoding bullets:

- ↑ ON
- ↓ Software selection ON, OFF, or Low Power
- ↘ OFF

3.1 Active

This is the default mode after RESET.

- ↑ The clocks to the CPU, memories, and peripherals are enabled.

3.2 Sleep

- ↓ Stops the clock to the CPU, a.k.a. the system clock.
- ↓ Suspends the instruction execution until RESET or an interrupt occurs.
- ↘ The peripherals can be clocked and continue to operate.
- ↘ The peripherals may generate interrupts to resume the CPU operation.
- ↘ The SRAM that was not shut down maintains its content.
- ↑ The CPU state registers and peripheral registers are maintained.
- ↑ The pins' logic levels remain static.

3.3 Deep Sleep

This mode is configurable and can potentially turn off almost the whole on-chip power consumption, with the cost of longer wake-up times.

- ↓ The shutdown of the CPU clock.
- ↓ The power consumed by the analog peripherals and the dynamic power used by the processor.
- ↘ The peripherals, if not configured, receive no internal clocks.
- ↘ The individual blocks may be in the on, low-power, or off states; as defined in the software.
- ↘ The device features can be automatically disabled.
- ↘ The SRAM that was not shut down maintains its content.
- ↘ This runs the selectable peripherals.
- ↘ The analog blocks are powered down by default, but they can be configured by software.
- ↑ The device registers maintain their content.

3.4 Deep Powerdown

- ↓ This shuts off the entire chip's clock and power.
- ↓ The SRAM and register content is not retained.
- ↓ All functional pins are tri-stated as long as they are supplied externally.
- ↑ The RTC is on through V_{DD_AO1V8}.

3.5 Full Deep Powerdown

- ↓ External supplies are powered OFF
- ↑ V_{DD_AO1V8} is ON

4 Power optimization techniques

Table 2 and Table 3 show the various clock and peripherals that can be software-configured in reduced power modes like Sleep, Deep Sleep, or Deep Power Down.

Table 2. Clocks in reduced power modes

Clock	Sleep	Deep Sleep	Deep Powerdown
1 MHz LPOSC	SW configured	SW configured	OFF
192 MHz FRO	SW configured	SW configured	OFF
XTAL OSC	SW configured	SW configured	OFF
System PLL	SW configured	SW configured	OFF
Audio PLL	SW configured	SW configured	OFF
RTC OSC	SW configured	SW configured	SW configured

Table 3. Peripherals in reduced power modes

Peripheral	Sleep	Deep Sleep	Deep Powerdown
SRAM memory	SW configured	SW configured	OFF
SRAM periphery	SW configured	SW configured	OFF
ADC	SW configured	SW configured	OFF
ACMP	SW configured	SW configured	OFF
MIPI	SW configured	SW configured	OFF
DSP	SW configured	SW configured	OFF
Boot ROM	ON	OFF	OFF

4.1 SRAM

The i.MX RT500 provides up to 5 MB of centrally-located SRAM divided into a collection of 32 partitions, each in size of 32 KB, 64 KB, 128 KB, or 256 KB.

Each block of memory consists of a periphery and the actual memory array. Each partition has independent power switches that can be turned on/off depending on how much RAM must to be kept alive. Save power by turning off the periphery of one or more RAMs while retaining the contents of those RAMs for later use. Table 4 lists the SYSCTL0 registers associated with SRAM.

Table 4. SRAM power-off

Active	Sleep or Deep Sleep	Power Switch
PDRUNCFG2	PDSLEEPCFG2	Memory Array
PDRUNCFG3	PDSLEEPCFG3	Periphery

After configuring the memory array and periphery, call the power library POWER_ApplyPD API to activate the changes.

The i.MX RT500 can clock-gate SRAM access. While these registers' primary purpose is to block access to a particular master, an alternate effect prevents the associated clock from propagating. Clock gating the SRAM access can result in a power reduction for unused partitions.

SYSCTL0☐AHB_SRAM_ACCESS_DISABLE
SYSCTL0☐AXI_SRAM_ACCESS_DISABLE
SYSCTL0☐DSP_SRAM_ACCESS_DISABLE

NOTE

When the periphery from an SRAM partition is powered down, the corresponding bits in the AHB, AXI, and DSP SRAM access should also be set to save power.

The SRAM partition physical location results in current consumption variations. Consider the code locality. Note that the current increases as the SRAM partition number increases. Figure 5 shows the current consumption vs the memory partitions: CM33 active, V_{DD_CORE} = 1 V, T = 25 °C, FBB, 192 FRO. All other SRAM memory arrays are off, the periphery is off, and the SRAM clock is gated.

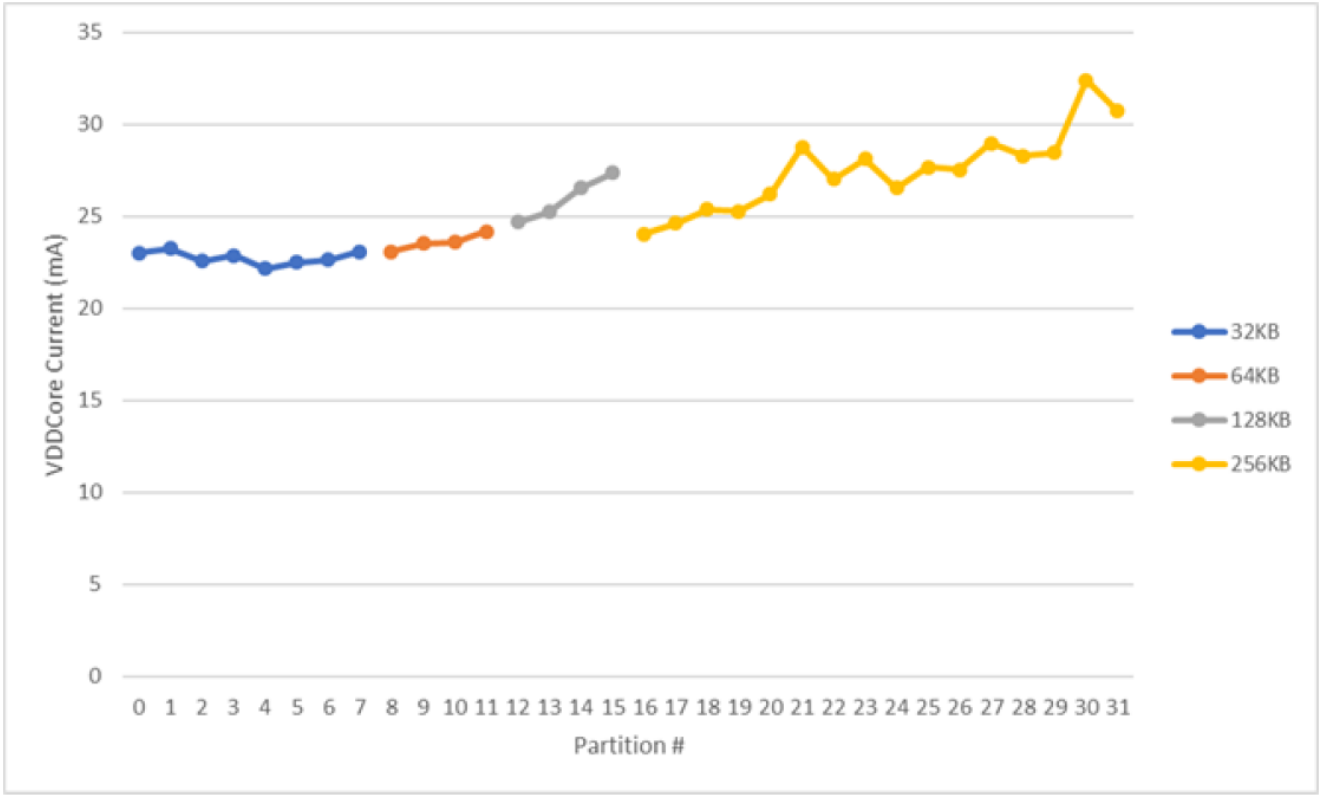

Figure 5. SRAM current consumption vs memory partitions

4.2 PMIC_MODEn pins

There are two ways to switch PMIC configurations: using the dedicated PMIC-I2C interface or through the PMIC_MODE0 and PMIC_MODE1 pins.

Using the PMIC_MODE pins provides voltage changes for low-power modes, such as Deep Sleep or Deep Powerdown.

Table 5. PMIC_MODE configuration

SYSCTL0			Power Mode	V_{DDCORE}	V_{DD1V8}	V_{DD_AO1V8}	V_{DD_IO3}
	PMIC_MODE1	PMIC_MODE0		SW1	SW2	LDO1	LDO2
PDRUNCFG0	0	0	Active / Sleep	1V	1.8V	1.8V	3.3V
PDSLEEPCFG0	0	1	Deep Sleep	0.6V	1.8V	1.8V	3.3V
PDSLEEPCFG0	1	0	Deep Powerdown	0V	1.8V	1.8V	3.3V
PDSLEEPCFG0	1	1	Full Deep Powerdown	0V	0V	1.8V	0V

When entering the Deep Powerdown or Full Deep Powerdown modes, the PMIC_MODE bit values from the PDSLEEPCFG0 register are latched into the always-on domain to maintain the state of the output.

4.3 Body Bias

The i.MX RT500 offers three different body bias modes for greater power optimization flexibility: Normal Body Bias (NBB), Reverse Body Bias (RBB), Forward Body Bias (FBB). The variation of three bits in the PDRUNCFG0/PDSLEEPCFG0 register determines the body bias mode.

Table 6. Body Bias

Mode	SYSCTL0			
	Register	RBB_PD	FBB_PD	RBBSRAM_PD
NBB	PDRUNCFG0	1	1	1
RBB	PDSLEEPCFG0	0	1	0
FBB	PDRUNCFG0	0	1	1

Table 7 shows when it is best to use Body Bias modes and how to set them through the power library.

Table 7. Body Bias power library

Mode	When to use	Power Library API
NBB	Very low frequencies < 60 MHz @ 0.7 V	POWER_EnterNbb
RBB	Only in the Deep Sleep mode	POWER_EnterDeepSleep
FBB	All other use cases	POWER_EnterFbb

The power library API complies with the specific process required when switching between Body Bias modes. The FBB is the default mode out of RESET and it should be the return state after waking from the Deep Sleep mode. When using the RBB, the SRAMRBB_PD and RBB_PD bits must be part of the "exclude_from_pd" array.

4.4 Clocks

4.4.1 PLLs

Disable any unused PFD outputs using the SYSPLL0PFD bits shown in Table 8.

Table 8. PLL PFD clock gate

CLKCTL0□SYSPLL0PFD			
b31	b23	b15	b7
PFD3	PFD2	PFD1	PFD0

4.4.2 FRO

Disable the clock to unused FRO divider outputs via the FRODIVOEN.

Table 9. FRODIVEN clock disable

CLKCTL0□FRODIVOEN

Table continues on the next page...

Table 9. FRODIVEN clock disable (continued)

b4	b3	b2	b1	b0
FRO/16	FRO/8	FRO/4	FRO/2	FRO/1

4.4.3 Oscillators

Configure the main crystal XTAL oscillator in the high-gain CLKCTL0_SYSOSCCTL0_LP_ENABLE=0b mode for high-noise environments or with jitter-sensitive applications. Otherwise, use the CLKCTL0_SYSOSCCTL0_LP_ENABLE=1b low-power mode.

4.4.4 kHz

Disable the 32-kHz oscillator when it is unused by changing the CLCKTL0_OSC32KHZCTL0_ ENA32KHZ=0b RTC_CTRL_RTC_OSC_PD=1b bits.

4.4.5 Automatic clock gating

i.MX RT500 can automatically clock-gate various AHB peripherals and SRAMs through the registers shown in Table 10.

Table 10. Automatic clock gate

SYSCTL0							
AUTOCLKGATEOVERRIDE0	DMAC1	DMAC0	CASPER	CRC	AHB2APB1	-	-
AUTOCLKGATEOVERIDE1	SRAM						
CLKGATEOVERRIDE0	PMC	ACMP	MU	ADC	USBPHY	SDIO1	SDIO0

4.4.6 Unused peripherals

Table 11 shows the peripherals that allow to shut-off the clock tree entirely when xxxFCLKSEL_SEL=7.

Table 11. Shut OFF clock selector

CLKCTL0□xxxFCLKSEL_SEL			
FLEXSPI0	FLEXSPI1	SCT	USBHS
SDIO0	SDIO1	ADC0	UTICK
WDT0	SYSTICK	-	-

4.5 Pad range

i.MX RT500 has five pad groups (V_{DDIO_0} to V_{DDIO_4}) and each has a set of GPIOs associated with it, as shown in the datasheet.

The V_{DDIO_3} voltage range levels range from 1.7 V to 3.6 V. This rail has a detector to sense the voltage value from a 1.8 V or 3.3 V range, but it consumes extra power. Match the current-voltage at V_{DDIO_3}. If the application needs voltage sensing, select "kPadVol_Continuous".

Table 12. Power library pad voltage range options

V_{DDIO_4}	V_{DDIO_3}	V_{DDIO_2}	V_{DDIO_1}	V_{DDIO_0}
kPadVol_171_198	kPadVol_Continuous kPadVol_171_198 kPadVol_300_360	kPadVol_171_198	kPadVol_171_198	kPadVol_171_198

To apply the pad rage settings to the PMC□PADVRANGE register, use the following power library code.

```
power_pad_vrange_t vrange = {
                              .Vdde0Range = kPadVol_171_198,
                              .Vdde1Range = kPadVol_171_198,
                              .Vdde2Range = kPadVol_171_198,
                              .Vdde3Range = kPadVol_300_360,
                              .Vdde4Range = kPadVol_171_198
                            };
POWER_SetPadVolRange(&vrange);
```

4.6 Power OFF switches

When the DSP, MIPI PHY, or ROM OTP are powered off, the OTPSWREN bit must be 1.

4.7 VDDCORE

When the core is running, the V_{DDCORE} regulator must be in the High Power mode. When it is in a power state different from the active one, it is recommended to configure the low-power mode at the V_{DDCORE} regulator and LVD.

Table 13. V_{DDCORE} regulator low power

SYSCTL0□PDSLEEPCFG0	
b4	VDDCOREREG_LP
b9	LVDCORE_LP

5 Power mode entry

5.1 Deep Sleep

The CM33 can only enter the Deep Sleep mode. Perform the following steps to enter the Deep Sleep mode:

1. Enable the potential Deep Sleep wake-up source.
2. Call the POWER_EnterDeepSleep API.

5.2 Deep Power Down (DPD)

The SYSCTL block is in the V_{DDCORE} domain, so the whole register content is lost when entering the DPD, including the bits that control the external PMIC (PMIC_MODE) and the V_{DDCORE} supply during the WFI (DEEP_PD).

When entering the Deep Power Down mode, the DEEP_PD and PMIC_MODE bit values from PDSLEEPCFG0 are latched into the always-on domain to maintain the Deep Power Down mode and the state of the MODE output pins.

6 Power mode exit

6.1 Sleep

The Sleep mode exits automatically when an interrupt enabled by the NVIC arrives at the processor or when a reset occurs. After a wake-up caused by an interrupt, the device returns to its original power configuration defined by the PDRUNCFG and PSCCTL registers' contents. If a reset occurs, the MCU enters the default configuration in the Active mode.

6.2 Deep Sleep

Table 14 lists all the Deep Sleep wake-up sources possibilities.

Table 14. Deep Sleep wake-up sources

Deep Sleep wake-up event	Comment
PINT	-
DMIC	-
HWWAKE	DMIC subsystem & certain flexcomm
SDIO	-
Flexcomm USART	Slave mode or 32 kHz
Flexcomm SPI	Slave mode
Flexcomm I2C	Slave mode
Flexcomm I2S	Slave mode
I3C	Slave mode
USB	Activity that needs a clock
RTC	Alarm or Wake timer
Micro-tick timer	Use for ultra-low-power wakeup
OS event timer	-
Watchdog interrupt	WDT0 only
Watchdog RESET	WDT0 only
RESET pin	-
DMA	-
PowerQuad	-
DSP	-

Table continues on the next page...

Table 14. Deep Sleep wake-up sources (continued)

Deep Sleep wake-up event	Comment
HASH-AES	-
CASPER	-
ADC	-
ACMP	-

6.3 Deep Power Down and Full Deep Power Down

The wake-up sources are as follows:

- ↑ Pin RESET
- ↑ RTC times out

The chip goes through the entire RESET process upon wakeup.

- ☐ The PMC turns on the on-chip voltage regulator. When the core voltage reaches the POR trip point, a system RESET is triggerred and the chip boots.
- ☐ All registers are in their reset state.
- ☐ To determine if the device is waking up from the Deep Power Down mode or the Full Power Down mode, read and clear the PMC☐FLAGS register.

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