AN13102

How to Get Best ADC Accuracy for LPC800

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1 Introduction

LPC800 serial has a 12-bit successive approximation analog to digital converter. In the application design, the ADC accuracy is the most important factor.

To evaluate the ADC accuracy, the following static characteristic parameters are used:

- EO - offset error. See Figure 1.

  The offset error (EO) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve.

- EG - gain error or the full-scale error voltage. See Figure 1.

  The gain error (EG) is the difference between the straight line fitting the actual transfer curve after removing offset error and the straight line which fits the ideal transfer curve.

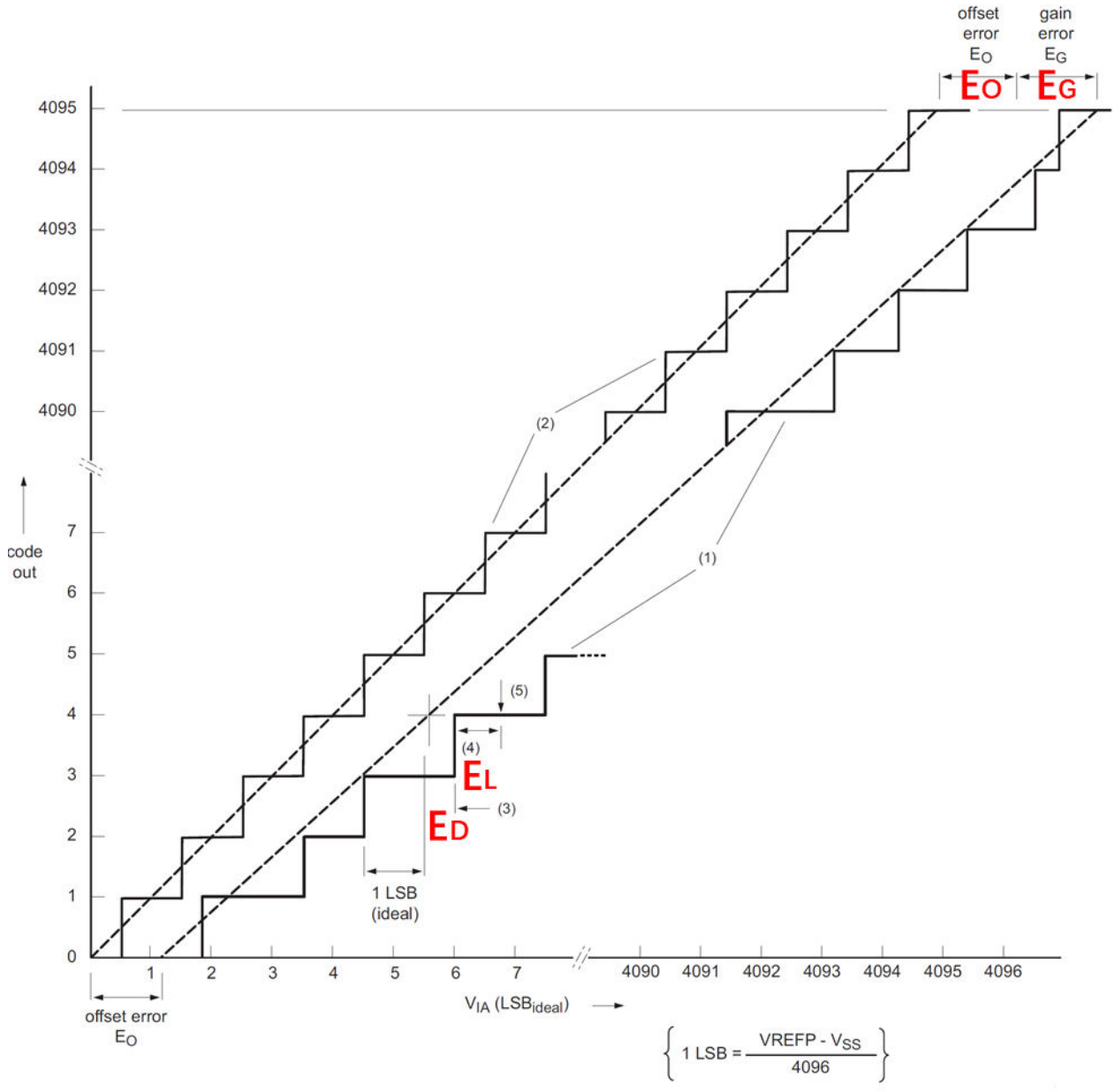
- EL - integral non-linearity. See Figure 1.

  The integral non-linearity (EL) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors.

- ED - differential linearity error. See Figure 1.

  The differential linearity error (ED) is the difference between the actual step width and the ideal step width.

In application design, designer should apply methods to reduce above errors to get the best ADC accuracy.



(1) Example of an actual transfer curve.
(2) The ideal transfer curve.
(3) Differential linearity error (E_D).
(4) Integral non-linearity ($E_{L(adj)}$).
(5) Center of a step of the actual transfer curve.

Figure 1. LPC800 ADC static characteristic parameters

Other factors also will affect ADC accuracy in application, such as:

- Power stability and noise.
- Reference voltage stability.
- Digital and analog part isolation in system.
- ADC input impedance matching with outside circuit impedance.

- PCB layout with EMI and EMC problems.

2 The methods to improve ADC accuracy

2.1 Hardware self-calibration

The A/D converter includes a built-in, hardware self-calibration mode. To achieve the specified ADC accuracy, the A/D converter must be recalibrated, at a minimum, following every chip reset before initiating normal ADC operation. For detailed usage, see LPC800 UM.

2.2 LPC800 ADC design note related with ADC performance

When using LPC800 ADC, for best performance, select VREFP and VREFN at the same voltage levels as VDD and VSS. When selecting VREFP and VREFN different from VDD and VSS, ensure that the voltage midpoint are the same:

(VREFP - VREFN)/2 + VREFN = VDD/2

2.3 Software processing to improve ADC accuracy

2.3.1 Oversampling with averaging to increase ADC accuracy

In the input signal sampling, when a white noise occurs in the input signal, ADC result losses the accuracy. To eliminate this white noise, over-sample the input signals and give an averaging arithmetic processing to the ADC result. This method has efficient help to deal with the white-noise interference.

2.3.2 Mathematical transformation to reduce calculation errors

Use mathematical transformation to reduce errors caused by temperature drift, humidity, environment, and fluctuations in power supply voltage.

In practical applications, some errors may be introduced due to changes in parameters such as ambient temperature and humidity, and the instability of the power supply voltage may also bring certain errors. Of course, you can choose a power module with a better temperature coefficient and higher accuracy to provide a stable voltage. However, due to the high cost of high-precision power modules, the ADC sampling numerical calculation formula is transformed, which can reduce the error caused by voltage fluctuations and improve the sampling accuracy without increasing the system cost.

Method illustration is as below:

Input voltage value can be got from Equation 1.

$$Vadc = \frac{Dadc}{Dref} * Vref$$

Equation 1. Input voltage formula 1

Where:

- V_{adc}: Input voltage value calculated by
- D_{adc}: Digital input voltage value read from ADC
- V_{ref}: Reference voltage
- D_{ref}: Digital reference voltage value read from ADC, this voltage also needed be converted.

Equation 1 can change to Equation 2 and Equation 3:

$$\frac{Vadc}{Vref} - 1 = \frac{Dadc}{Dref} - 1$$

Equation 2. Input voltage change 1

$$\frac{Vadc - Vref}{Vref} = \frac{Dadc - Dref}{Dref}$$

Equation 3. Input voltage change 2

Get Equation 4:

$$Vadc = \frac{Dadc - Dref}{Dref} * Vref + Vref$$

Equation 4. Input voltage formula 4

As shown in Equation 1 and Equation 4, comparing errors for Equation 1 and Equation 4 is same thing as comparing errors for D_{adc} and D_{adc}-D_{ref}. In the fluctuations in power supply voltage or other factors, the error direction is same for D_{adc} and D_{adc} - D_{ref} and the error for D_{adc} - D_{ref} is less than error for D_{adc}.

Now, we can get the result that using this mathematical transformation can reduce errors caused by temperature drift, humidity, environment, and fluctuations in power supply voltage during the analog-to-digital conversion.

2.3.3 Zero voltage pre-sampling to deal with EO

EO is same for each analog-to-digital conversion, so users can do zero voltage pre-sampling to eliminate it.

Before the analog-to-digital conversion, perform a conversion for 0 voltage and keep value in memory. In later conversion, minus each conversion result by the result of 0 voltage in memory, to basically eliminate EO.

2.4 Hardware processing to improve ADC accuracy

To make the ADC achieve the best accuracy, proper design and configurations of the entire system is required. The basic hardware processing is to separate the analog and digital layouts, including isolating the grounds by different PCB planes, avoiding analog/digital tracks crossing each other, using different power supply. In some cases, adding an external RC filter in ADC circuit is also recommended to eliminate the high frequency noise.

The following sections provide some suggestions on PCB layout, system power decoupling, and analog/digital grounding.

2.4.1 ADC pin processing

PCB trace length for ADC pins should be as short as possible. In practical application design, the influence of parasitic parameters on PCB traces for ADC pins should be fully considered.

If some digital signal lines are located between the analog pins, it is recommended avoid them by not selecting these digital pins if possible.

Input filters connected to the ADC will have a significant impact on the noise immunity of the analog parts. The type of the filters to be used depends on the input signal frequency. The location of the filter's capacitors is also very important. It's recommended to place the filter capacitors onto the same (analog) sub ground plane.

2.4.2 Decoupling system power supply

Using electrolytic capacitors near the PCB's power source input, and ceramic capacitors next to the power pins of the microcontroller, usually put a 0.1 µF to filter high frequency noise, and a 100 µF to filter low frequency noise. The capacitors should be as close as possible to the power pins and place the two capacitors between each pair of power pins.

To effectively reduce noise emissions, low the inductive impedance by using the thicker to trace to the microcontroller's power supply. Due to the power line emissions, it is suggested to separate power lines from signal lines to decrease crosstalk.

Figure 2 shows an example for decoupling capacitors placement. C4 is for filtering low-frequent noise, and C5, C6, C7, C8, C9 is for filtering high-frequent noise.

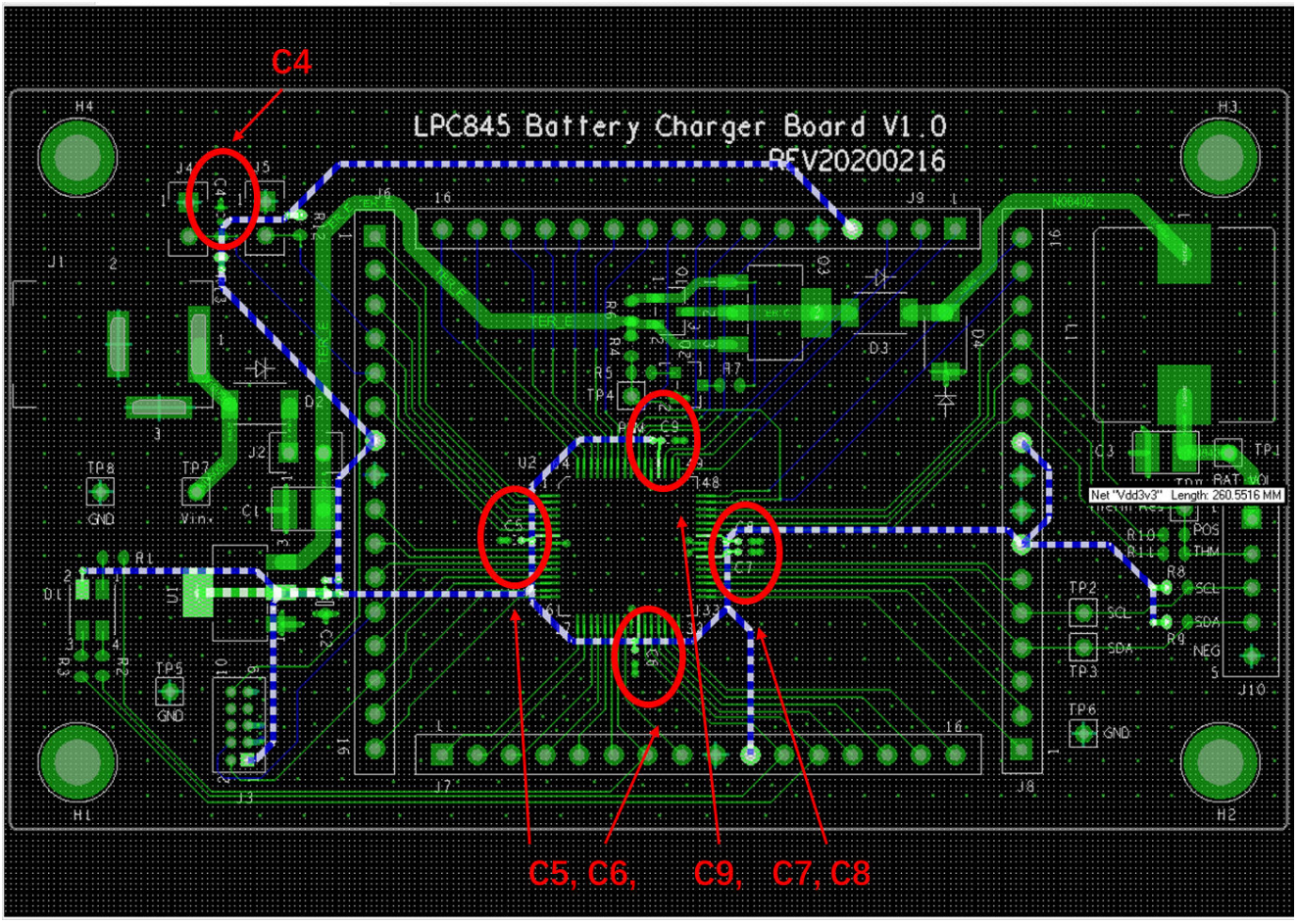


Figure 2. An example for decoupling capacitors placement

2.4.3 Analog/Digital grounding

The noise on the power and ground lines should be reduced as much as possible, A decrease of noise is achieved by segmenting the ground plane into the digital and analog domains. These planes are physically separated by a small gap and connected only at one point that is a few millimeters in size.

Some packages for LPC800, like LPC84x 48/64 LQFP package, the VDDA/VSSA is separated from VDD/VSS, If the digital part and analog part are connected to the same power supply, a small inductor or magnetic bead is used to connect between the digital part and analog part.

Use a ground plane to isolate noisy digital components from analog components and analog ground to surround analog signals when routing.

2.4.4 Analog source impedance match

In some applications, to control the power consumption, the ADC sample circuit which connects to ADC pin uses resisters with value above 100 KΩ. LPC800 has minimum input impedance about 100 KΩ when ADC applies the maximum conversion speed,

1.2 M samples/s for LPC82x/84x and 480 K samples/s for LPC80x. In this case, the ADC pin input impedance must be taken in consideration for input voltage measurement.

Figure 3 shows an example for a typical ADC sampling circuit.

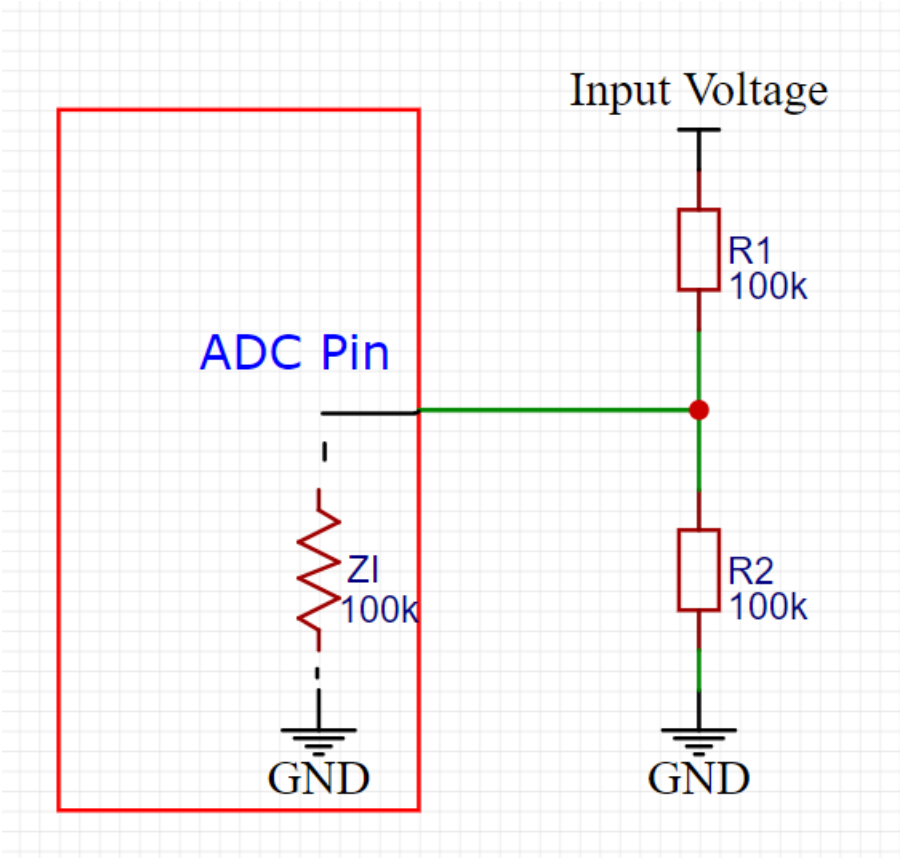


Figure 3. ADC pin analog source impedance match

In this application, when ADC apply maximum convert speed, the voltage in ADC pin will not be half of Input Voltage, should be one third of Input voltage. Designer should take care of this affect in their sample circuit design.

The other characteristic for ADC input impedance is that the input impedance is inversely proportional to convert speed, if user application don’t require high-speed ADC convert, we can slow down the ADC convert speed, e.g. slow 10 times, to get input impedance increase 10 times, this can eliminate the affect caused by ADC pin input impedance mostly. This operation can done by config CLKDIV bits in CTRL register for ADC module.

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