AN13032

MC33771/2 B/C General Purpose Input Output (GPIO)

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Document information

Information	Content
Keywords	MC33771B, MC33772B, MC33771C, MC33772C, BMS, Battery Junction Box, Temperature, high voltage
Abstract	This application note provides guidelines for using the MC33771/2 B/C battery cell controllers for temperature and high voltage sensing.

Revision history

Revision	Date	Description
1	20201218	Initial version

1 Introduction

The NXP Semiconductors battery cell controller components MC33771B, MC33772B, MC33771C and MC33772C feature seven pins (GPIO0..6) that can be used as General Purpose Input/Output (GPIO).

For user flexibility, all GPIOs may be individually configured as digital inputs or output ports, as ratiometric analog inputs for temperature acquisitions, or analog inputs for absolute measurements. Two GPIOs have additional features: GPIO0 as wake-up input, GPIO2 as convert trigger input

The ratiometric mode supports temperature measurement with NTC (Negative Temperature Coefficient) resistances and additional safety features allowing automatic overtemperature / undertemperature detection with programmable temperature thresholds.

Additional features allow short and open load detections.

This application note provides guidelines to connect, use GPIO in analog and ratiometric modes, and provides some considerations on specific use cases.

2 General description

At device initialization (power on reset, hardware reset, software reset) and power-up of the device, the seven GPIOs ports are configured as analog inputs for ratiometric measurements.

Each port can be individually set as digital inputs, analog input, ratiometric measurement and absolute measurement through register GPIO_CFG1, for GPIOx (x = 0 to 6).

The specific features of the GPIO0, GPIO2, GPIO5 and GPIO6 that can be used respectively as wakeup input, Start Of Conversion input (for SPI application) and redundant current sense inputs are not described in this application note. These specific configurations can be done through register GPIO_CGF2. They are fully explained in the data sheet.

2.1 GPIOx pin block diagram

On each GPIO0 to GPIO6 pin, four internal circuit interfaces are connected in parallel to allow the functions listed below. See Figure 1.

- Analog input (absolute or ratiometric)
- Digital input
- Digital output
- Open terminal detection circuit

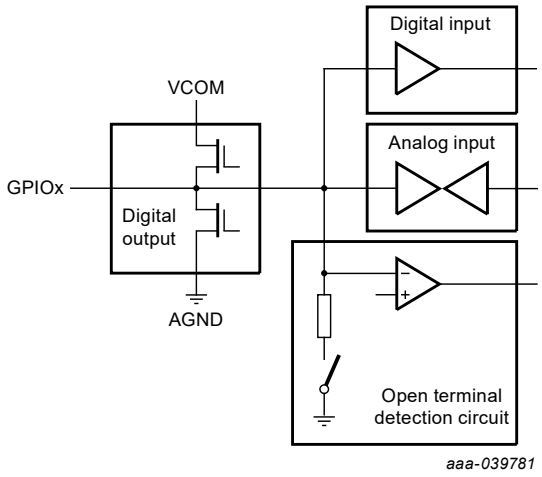

Figure 1. GPIOx pin diagram

All circuit interfaces of these blocks are referenced to VCOM, a 5 V internal regulator, and AGND. VCOM is intended to supply the NTCs in ratiometric mode and other external components (optional EEPROM, etc…), with a maximum current capability (IVCOM) of 5 mA in TPL mode. Up to 10 mA is allowed in SPI mode.

As all the circuit interfaces are in parallel for each GPIO, low impedance path to VCOM in the digital output buffer must be considered, thus giving some electrical limitation even if the GPIO are used as absolute analog inputs.

When the device is in low-power mode (SLEEP or IDLE mode), the VCOM regulator is shut down and voltages applied externally should not exceed maximum values or the device can be damaged. See Section 4.2.1 "ANx min/max voltage ranges".

For GPIO0, an additional wakeup block is connected to the pin. This input is designed to support an external voltage when the device is in SLEEP mode. There is no low impedance path to VCOM.

2.2 GPIO configurations

Two registers are available to the user to configure the GPIO ports. One register is available to read digital configured GPIO port status.

GPIO_CFG1 is used to configure, individually, each GPIO port as ratiometric, analog absolute, input or output port. See Table 1

Table 1. GPIO_CFG1 register

$1D	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write			GPIO6_CFG		GPIO5_CFG		GPIO4_CFG		GPIO3_CFG		GPIO2_CFG		GPIO1_CFG		GPIO0_CFG	
Read	0	0														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_cfg		Description		Register controls the configuration of the GPIO port												
		00		GPIOx configured as analog input for ratiometric measurement												
		01		GPIOx configured as analog input for absolute measurement												
		10		GPIOx configured as digital input												
		11		GPIOx configured as digital output												
		Reset condition		POR												

GPIO_CFG2 is used to configure specific functions for GPIO0 (wakeup) and GPIO2 (SOC) and output level for ports configured as digital output. See Table 2

Table 2. GPIO_CFG2 register

$1E	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write							GPIO2_SOC	GPIO0_WU	GPIO0_FLT_ACT	GPIO6_DR	GPIO5_DR	GPIO4_DR	GPIO3_DR	GPIO2_DR	GPIO1_DR	GPIO0_DR
Read	0	0	0	0	0	0										
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The GPIO_STS register reports the level high or low of the GPIO ports configured as digital inputs. For digital output it also provides a status of the ports, regardless of the digital configuration, which is a feedback of the commanded output. See Table 3.

Table 3. GPIO_STS register

$1F	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]								
Read	GPIO6_H	GPIO6_ST	GPIO5_H	GPIO5_ST	GPIO4_H	GPIO4_ST	GPIO3_H	GPIO3_ST	GPIO2_H	GPIO2_ST	GPIO1_H	GPIO1_ST	GPIO0_H	GPIO0_ST		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_H		Description		The GPIOx_H bits detect and latch the low to high transition occurring on the GPIOx input												
		0		No low to high transition detected												
		1		A low to high transition has been detected												
		Reset condition		POR/clear on write 0												
GPIOx_ST		Description		Realtime GPIOx status												
		0		Report GPIOx at low level												
		1		Report GPIOx at high level												
		Reset condition		POR												

[1] test

3 Digital IO description

3.1 Configurations

Setting the GPIO_CFG1[GPIOx_CFG] bits to 10 or 11 configures the specific port (X=0 to 6) as a digital input or output.

3.2 GPIO configured as digital input

3.2.1 Electrical parameters

Digital input interfaces are compatible with 5 V and 3.3 V logic signals and fulfill the following characteristics:

Table 4. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Input high voltage (3.3 v compatible)	2.0	—	—	V
V_{IL}	Input low voltage (3.3 V compatible)	—	—	1.0	V
V_{HYS}	Input hysteresis	—	100	—	mV
I_{IL}	Input leakage current Pins tristate, v_{in} = v_{com} or AGND	–100	—	100	nA

A deglitch filter is available : 2.5 µs < T_{GPIOX_DIN} < 5.6 µs

3.2.2 Register configurations

The GPIO_STS[GPIOx_ST] bits report the state '0' or '1' of the corresponding GPIOx

Via GPIO_STS[GPIOx_H] bits, low-to-high transition occurring on the GPIOx input can be detected and latched. The bit can be reset by writing 0.

There is no available bits to detect and latch a high-to-low transition.

3.2.3 Maximum voltage rating

Refer to Section 4.2.1 "ANx min/max voltage ranges".

3.3 GPIO configured as digital input

3.3.1 Register configurations

Pins configured as outputs are driven high or low by writing to the GPIO_CFG2[GPIOx_DR] bits.

Status of the ports, regardless of the digital configuration, is provided in the GPIO_STS register. This register is a feedback of the commanded output.

3.3.2 Diagnostics

Ports configured as GPIO outputs are diagnosed by the MC3377x only for short-circuit detection.

An output state GPIO_STS[GPIOx_ST], which is opposite of the commanded state GPIO_CFG2[GPIOx_DR], is considered to be shorted. The corresponding GPIO_SHORT_ANx_OPEN_STS [GPIOx_SH] is set. Each short fault bit GPIOx_SH associated with each GPIOx is OR wired to the FAULT2_STATUS[GPIO_SHORT_FLT] bit.

The GPIOx_SH bit, when unmasked, activates the FAULT pin.

Table 5. GPIOx_SHort_Anx_OPEN_STS register

$21	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Write		w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]	w0c[1]
Read	0	GPIO6_SH	GPIO5_SH	GPIO4_SH	GPIO3_SH	GPIO2_SH	GPIO1_SH	GPIO0_SH	0	AN6_OPEN	AN5_OPEN	AN4_OPEN	AN3_OPEN	AN2_OPEN	AN1_OPEN	AN0_OPEN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GPIOx_H		Description		GPIOx short detection GPIOx_SH ored is provided in FAULT2_STATUS[GPIO_SHORT_FLT]												
		0		No short detected												
		1		Short detected, pad sense is different from pad command												
		Reset condition		POR/clear on write 0												
GPIOx_ST		Description		Analog inputs open load detection. ANx_OPEN ored is provided in FAULT2_STATUS[AN_OPEN_FLT]												
		0		No open load detected												
		1		Open load detected on Anx												
		Reset condition		POR/Clear On Write 0 (ANx_OPEN is set again with open load detect switch closed and open load persists)												

[1] test

3.3.3 Electrical parameters

It is recommended to use an external pull-down resistor to fix the voltage when VCOM is off.

Device current consumption

Configuring GPIOx as digital outputs increases the overall current consumption of the BCC in active mode only.

Up to a 1 mA on Ivpwr at room temperature, if all GPIOx are configured as digital outputs. There is no impact on the low power modes (SLEEP) current consumption

Driver Impedance

In active mode (INIT, NORMAL, DIAG), the output will present a maximum impedance of 1600 Ω.

It is recommended to limit the output current to ±0.5 mA to keep the maximum output voltage range between 0.8 V/ VCOM – 0.8 V.

4 Analog ANx description

Setting the GPIO_CFG1[GPIOx_CFG] bits to 00 or 01 configures the specific port (x=0 to 6) as an analog input for ratiometric measurement or as an analog input for absolute measurement.

GPIOx configured as analog inputs are also named ANx.

4.1 Measurement registers

To perform the voltage measurement, a SOC (Start Of Conversion) request should be triggered. After the cell terminal acquisitions, the seven values AN0 to AN6 are acquired and the 15 bits data are stored in seven 16 bits MEAS_ANx registers, based on the sequence shown in Figure 2.

The resolution of the measurement result in the MEAS_ANx registers does not depend on the selected ADC resolution (13 to 16 bits). The ADC resolution will have an effect on the conversion time (the slowest and the fastest) and on the conversion noise (the lowest and the highest). For absolute mode the resolution is VCT_ANX_RES = 152.58789 µV/LSB. For ratiometric mode the resolution is VANX_RATIO_RES = VCOM * 30.5176 µV/LSB.

The conversion timings and data availability will depend on the ADC resolution. Please refer to the data sheet.

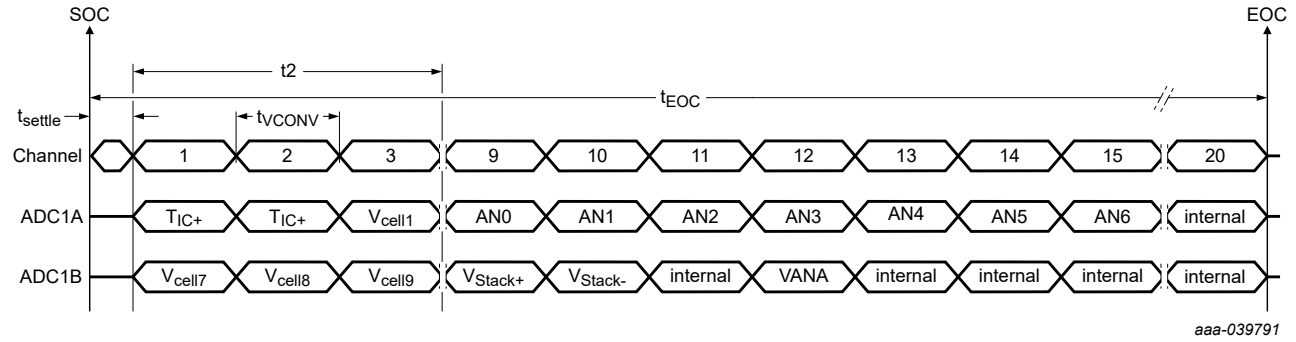

Figure 2. MC33771x ADC conversion sequence in normal mode

For all MEAS_xxxx registers, most significant bits are used to store the data ready status. This bit is cleared into all the user measurement registers when a SOC is initiated. When the following have been acquired, the values are frozen.

- All external voltages (cells, ANx)
- Die temperature for temperature compensation
- Voltage diagnostic references

After the values are frozen

- Gain compensations are applied
- Offsets are measured and cancelled
- Final results are stored into measurement registers

At teoc, depending on the ADC resolution, data ready bits are set in all measurement registers.

4.2 Absolute mode – voltage measurement

Absolute mode is used for voltage measurement, with reference to the ground of the device. Typical application use cases imply battery high-voltage sensing, relay status reporting and isolation monitoring. In high-voltage applications (typically 400 V and above for automotive applications), all these functions are usually integrated in a specific isolated board in addition to the current sensing components, such as the battery junction box and the switch box.

In most of the cases, voltage measurements are designed with low-cost high-ohmic resistor dividers. These dividers deliver a portion of the high voltage to the inputs of the GPIO pins.

Although NXP does not recommend any specific schematic, the latter should fulfill the following rules:

- To guarantee the measurement accuracy and avoid internal ADC clamping, the maximum applicable voltage should not exceed 4.85 V.
- To avoid any accuracy error that can affect all cell terminal and ANx measurement, it is forbidden to have any GPIOx < –0.3 V versus AGND.
- To avoid any damage and uncontrolled behavior, the maximum current that can be injected on any GPIOx is 5 mA.

The errors for the analog measurements are given in the data sheet (VERRx for cell voltage measurements and V_{ANX_ERR} for the GPIOs). These errors already include tolerance for temperature, soldering and aging (5 sigmas).

Depending on the application, residual voltages coming from external sources can be permanently applied on the GPIOx pins. Depending on the mode of the device and therefore on the VCOM state, GPIO[1..6] pins have potentially different weak impedance paths to internal VCOM supply and AGND. See Section 4.

4.2.1 ANx min/max voltage ranges

Device in active mode with VCOM ON (NORMAL, DIAG, INIT modes)

VCOM is a 5 V regulated supply derived from an internal VPRE regulator. VCOM has a high dynamic current capability, above 100 mA, mainly to supply the TPL driver circuit when transmitting messages. In static mode, the current capability is much lower. For instance only 5mA is allocated for external use in TPL mode. This is the static mode that we must consider when external current is injected on GPIOx pin.

To highly simplify the input circuit schematic in static mode, a 40 KΩ equivalent resistance is connected between the VCOM and the GND. Two MOSFETS transistors (output buffer) and two 30 Ω resistances are on the path between VCOM and AGND.

Two cases are discussed below if Vgpio can exceed data sheet limits.

Vgpio > VCOM+0.5 V

The red arrow shows the current path to VCOM if VGPIO> VCOM + 0.5 V. See Figure 3.

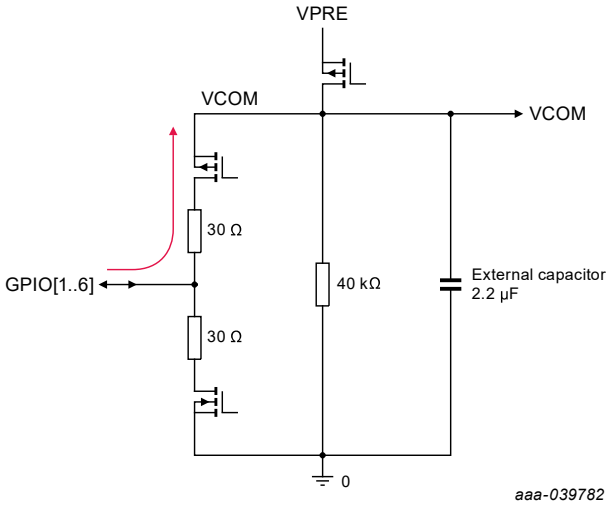

Figure 3. Equivalent diagram when device in active mode

Ideally, for GPIO1 to 6, as mentioned in the data sheet the maximum applied voltage should not exceed (Vgpiox) : VCOM + 0.5 V.

The VCOM internal regulator cannot absorb static DC current, thus injecting less than 140 µA on any GPIOx pin may raise the VCOM up to 5.4 V. This may trigger the VCOM OV detection and associated safety mechanism, such as a retry strategy.

To increase the injection current capability, it can be considered to increase the static DC VCOM current consumption by using external loads connected on the VCOM pin, as NTCs (but might be at high impedance at low temperature), EEPROM, or a simple pull-down resistor. It should be ensured that the VCOM maximum current capability (IVCOM) is not exceeded: 5 mA in TPL mode, 10 mA in SPI mode.

Another solution is to place a 5 V Zener diode on the GPIO pins to protect against overvoltage or to place a 10 kΩ resistor in series to limit the voltage on the GPIO pin. But this would imply possible accuracy degradation due to the GPIO input leakage current (Iil parameter).

Vgpio < AGND

Negative voltage applied on any GPIOx pin, including GPIO0, should not exceed –0.3 V versus the device GND.

Applying below –0.3 V could trigger internal NPN parasitic components. Consequences might included accuracy loss on all GPIOs and also on CT (cell terminal) pins.

Device in Low power modes with VCOM OFF (IDLE and SLEEP modes)

In HV sensing applications or for any voltage monitoring, switches, such as MOSFETs or optomos, should be added to open resistor dividers. In addition, avoid applying any voltage on any GPIO pin when the device is in low power mode.

Vgpio > +0.5 V

For GPIO0, there is no path to VCOM rail, therefore allowing up to 6.5 V on this pin. It does not depend on the configuration of the GPIO0.

When VCOM is OFF, the internal GPIO[1..6] pins are equivalent to the schematic. See Figure 4.

An active circuit switches an $R_{VCOM(SS)}$ VCOM sleep mode pull-down resistor, typ 2 KΩ. It allows a fast discharge of external capacitor (2.2 µF).

To avoid any damage to the device, the maximum input current should not exceed 5 mA per pin.

A voltage above +0.5 V applied on a GPIO pin will bias the internal VCOM rail. Reaching a certain level, this can lead to unexpected and uncontrolled device behavior. For example, the state machine considers the device in SLEEP/IDLE mode but the VCOM is externally biased.

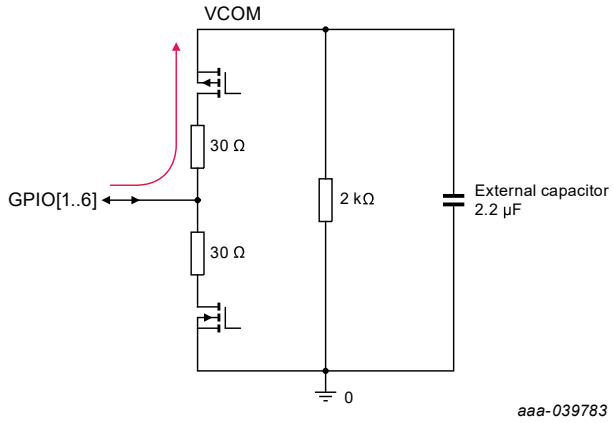

Figure 4. Equivalent diagram when device in low power mode

Vgpio < AGND

To avoid any risk along temperature range and parameter dispersion (resistors) it is safe to limit current to 5 mA per pin.

4.2.2 HV measurements for BJB – accuracy

For accuracy evaluation, two parameters can be considered: maximum input current leakage I_{IL} (±100 nA) and the V_{ANX_ERR}.

The resistor divider should be sized to obtain 4.85 V (Vct_Rng and note) for the maximum measurable battery voltage. This restriction maximizes measurement accuracy and avoids ADC clamping.

A MOSFET switch or an OptoMOS should be used to open the resistor divider when the measurement is not required. This design avoids useless current paths when the device is in low-power mode.

An HV sensing bridge can be simply designed, as shown in Figure 5.

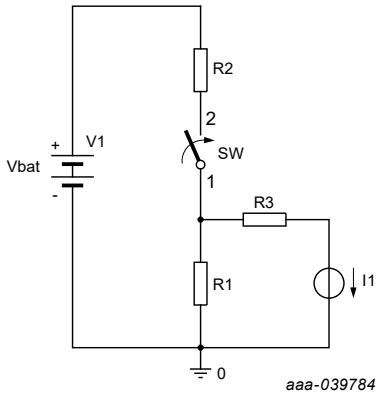

Figure 5. HV sensing bridge circuit

Effect of the ANx leakage current on the accuracy

Maximum leakage current IIL: ±100 nA (after aging, 6 sigmas)

The leakage current will induce a parasitic voltage drop (VERROR) in the resistor divider, following this formula:

$V_{ERROR} = I_{LEAK} * R2//R1 + R3;$

In HV sense application: R2 >> R1

→ The equivalent impedance seen by ANx input is R1+R3.

Example: to sense Vbat = 500 V, one can use R2 = 2 MΩ and R1 = 20 KΩ; R3 = 3.3 KΩ. The maximum error due to the leakage current is around VERROR = 2.3 mV.

Total measurement error: $V_{ERROR} + V_{ANX\_ERR}$

V_{ANX_ERR} : –8 mV/8 mV (In the range [0, 4.85 V], –40 °C < Ta < +105 °C).

Added with V_{ERROR}, and based on the previous example, the total error on measurement is less than 0.5 % in the range 1 to 4.85 V. See Figure 6.

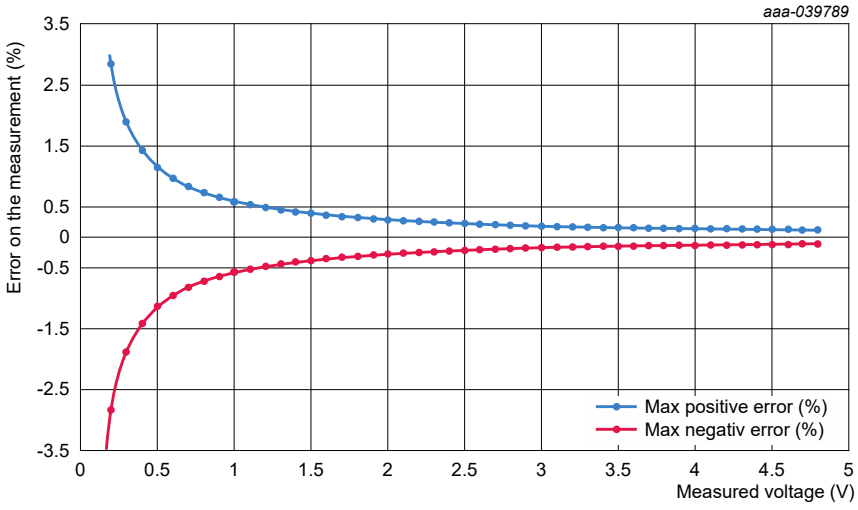

Figure 6. Error on the measurement (%)

4.3 Ratiometric mode – temperature measurement using NTC thermistors

For temperature measurement using NTC thermistors, the ratiometric mode is recommended to get rid of the NTC voltage supply fluctuation. Using a ratiometric measurement mode removes any error that could be coming from a variation of the VCOM voltage, used to supply the NTC thermistors. Thus, better temperature measurement accuracy is achieved.

When the GPIO is configured as analog input for ratiometric measurement, the reference voltage of the ADC (1.25 V) is derived from VCOM.

The VCOM maximum current allowed for external use is IVCOM, typically 5 mA. The VCOM regulator is mainly used to supply the TPL transceiver. If the application is based on SPI communication, then up to 10 mA maximum can be allowed for IVCOM.

If an external power supply is used, there is no other choice but to use absolute measurement and consider the possible variations of its voltage. These variations include temperature, aging, part-to-part variation and supply current. An accurate voltage reference is recommended to get good measurement accuracy.

The typical application schematic is shown in Figure 9.

The content of the ANx measurement register (Code(Hexa) in the formulas below) depends only on the NTC thermistor value (hence its temperature) and not on VCOM voltage value.

$$\mathrm{Code\ (hexa)} = 0\mathrm{x7FFF} * \mathrm{Rntc} / (\mathrm{Rntc} + \mathrm{Rtc}) \tag{1}$$

To calculate the NTC thermistor value, use the following formula :

$$\mathrm{Rntc} = \mathrm{Rtc} / (0\mathrm{x7FFF} / (\mathrm{Code(hexa)} - 1)) \tag{2}$$

To detect overtemperature (OT) and undertemperature (UT), the generated digital value is compared to an individually programmed threshold in the TH_ANx_OT (1.16 V default) and TH_ANx_UT (3.82 V default) registers. ADC1-A results on any temperature measurement input that exceeds the threshold activates the FAULT1_STATUS[AN_OT_FLT,AN_UT_FLT] bit.

NXP does recommend schematics to fulfill best accuracy achievement, automotive EMC/ESD performances, timing constraints for cyclic acquisitions used and safety mechanisms operations.

If other NTCs models are used with specific low-pass filter designs, the following rules should in all case be fulfilled.

- To guarantee the measurement accuracy, the NTCs should be supplied with VCOM.
- VCOM current capability is 5 mA maximum in TPL mode and 10 mA in SPI mode.
- If cyclic acquisition is used in SLEEP mode, the ANx input settling time should be less than 450 µs ≥ Overall LPF filter time constant below 100 µs at overtemperature threshold.
- 100K NTC can be used, but Cntc and Clpft values should not be increased.
- A maximum of 10 nF on Clpft to avoid any damage if SM05 used.

- Resistor values have an impact on safety mechanism SM06.
- SM06 cannot be used with 100K NTCs and proposed schematics.

4.3.1 Cyclic acquisitions - SLEEP mode

When the component is in SLEEP mode (VCOM = 0), cyclic acquisitions can be configured to automatically monitor OT/UT based on NTC measurements. During cyclic acquisitions, cell terminal and ANx registers are not refreshed. Only OT/UT evaluations are executed. In addition, a complete wakeup sequence is started if there is a threshold violation. If not, the device switches back to sleep mode until the next cyclic acquisition sequence. Usually only OT threshold is critical for safety reasons and set between 60 °C and 85 °C.

When the cyclic acquisition starts, VCOM is switched on and the ANx inputs should be stabilized before the ADC acquisition starts; if not, false OT alarms could be triggered.

First and second order filters are recommended in the data sheet to be used with 10 KΩ NTC resistors. Their bandwidths are calculated to match with the required ANx settling times.

In case of usage of high impedance NTCs or high capacitor values leading to low frequency low pass filter bandwidth, OT false alarms due to low VCOM and ANx settling times can be triggered. Some timing considerations should be evaluated to avoid such false alarms.

Acquisition timings

The AN0 is the first analog input (GPIO0 pin) to be sampled in the ADC acquisition sequence after a Start Of Conversion (SOC) is initiated.

After nine cycle times, AN0 measurement starts (valid for both MC33771 and MC33772). See Figure 7, which is from the MC33771B data sheet.

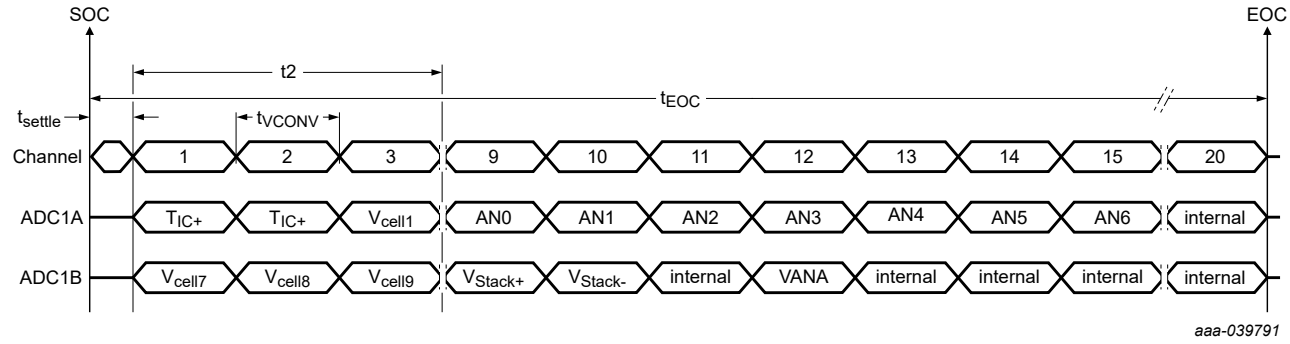

Figure 7. ADC conversion sequence – AN0

At wake up from SLEEP mode, a certain time is required for the VCOM regulator to ramp up and be stabilized before starting any acquisition.

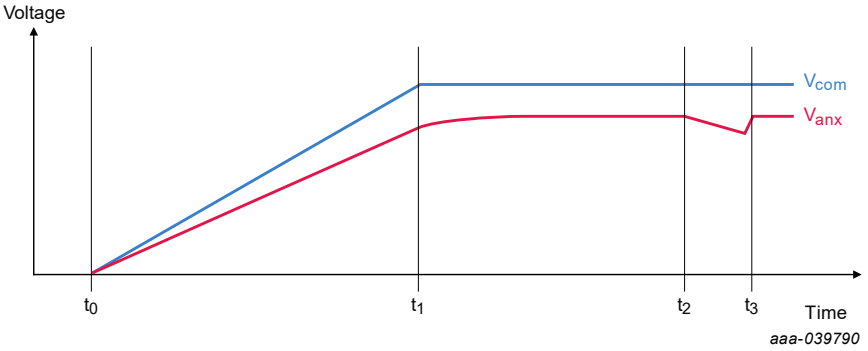

Figure 8. ANx settling time

Vanx must be settled when the measurement appends. The settling time depends on the filter time constant. AN0 is the first acquired analog input:

- t0 = 0 µs: wakeup
- t1 = 240 µs (±5 %): fixed window timing. This is the maximum time allowed for VCOM to ramp up. VCOM monitoring starts after t1: if VCOM_UV is triggered then VCOM is switched OFF.
- t2 = t1 + T_{SETTLE} (12.28 µs) + 8*T_{VCONV} (25.36 µs/16 bits) = 455 µs (±5%): AN0 measurement starts.
- t3 = t2 + T_{VCONV} = 480 µs (±5%): AN0 measurement ends

Total measurement (16 bits) : t1 + T_{SETTLE} + 20* TVCONV = 240 + 12.28 + 20 * 25.36 = 760 µs

- Regardless the low pass filter in front of any ANx pins, the time constant should not exceed 100 µs (455 µs / 5) at overtemperature threshold to avoid any false alarm; fcut = 1.6 Khz min.

NTC filters

Onboard NTC sensors on the same board as the Battery Cell Controller device are considered as local sensors. Because these sensors are local, they are not exposed to ESD events and high EMC disturbances. A first order low-pass filter is recommended to filter ambient noise (Rpft1/Clpft1)

Off-board NTC sensors are fixed in the battery cells. These sensors are connected to the BMS board with cables. They are considered as global sensors and then exposed to ESD events and possible high EMC disturbances. To sustain these constraints and match with our ESD/EMC pass/fail criteria (report to EMC and ESD validation reports), a second order low-pass filter is recommended. These components are shown as optional in Figure 9.

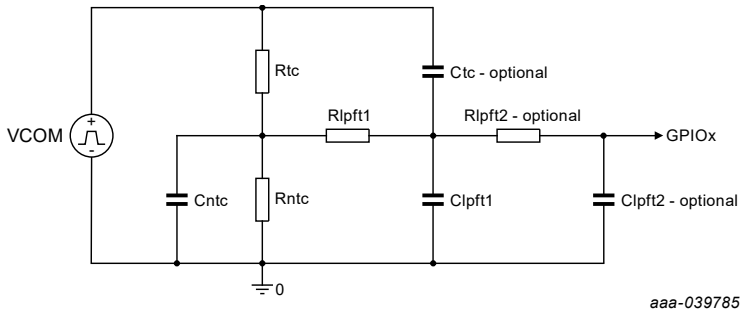

Figure 9. NTC - Low pass filter schematic

Reference	Value
Rtc	6.8 KΩ / 1 %
Rntc	10 KΩ at 25 °C (Murata NCP xxx XV103)
Cntc	1.2nF
Rlpft1	3.3 KΩ
Clpft1	1.2 nF (note 1)
Rlpft2	3.3 KΩ
Clpft2	1.2 nF (note 1)

Note 1: *Clpft1 for onboard NTCs or Clpft2 for offboard NTCs should not exceed 10 nF to avoid damaging the device. See* Section 4.4.1.

For cyclic acquisition constraints (see Acquisition timings), the table below shows some examples of ANx time constants when VCOM is ramping up, with Rntc =10K (Rtc = 6.8K) and Rntc = 100K (Rtc = 100K). This time constant should be less than 100 µs. These values are valid for both onboard and off-board filters.

	NCPxxXV103 10 KΩ at 25 °C		NCP18WF104 100 KΩ at 25 °C	
Temp	**Impedance**	**Fcut**	**impedance**	**Fcut**
25 °C	10K	16 µs	100K	122 µs
60 °C	2.521	7 µs	22.621	46 µs
85 °C	1.097	5.3 µs	9.129	20 µs

With 100 KΩ, UT(undertemperature) below 0 °C cannot be detected during cyclic acquisitions.

For the latter, it is forbidden to increase either Cntc or Clpft values to avoid false OT (overtemperature) alarm at room temperature.

4.3.2 Temperature acquisition accuracy

With the recommended data sheet schematic, the NCPxxxXEV103 10 KΩ NTCs (1%), considering V_{ANX_ERR} = 16 mV maximum along the temperature range, the expected temperature accuracy is shown in Figure 10 (only considering the MC3377xC ANx input pins characteristics, not including the NTC and resistor divider accuracy).

The temperature error is below 2.5 °C along the temperature range –40 °C to +125 °C, and less than 1 °C in the range –20 °C to +85 °C.

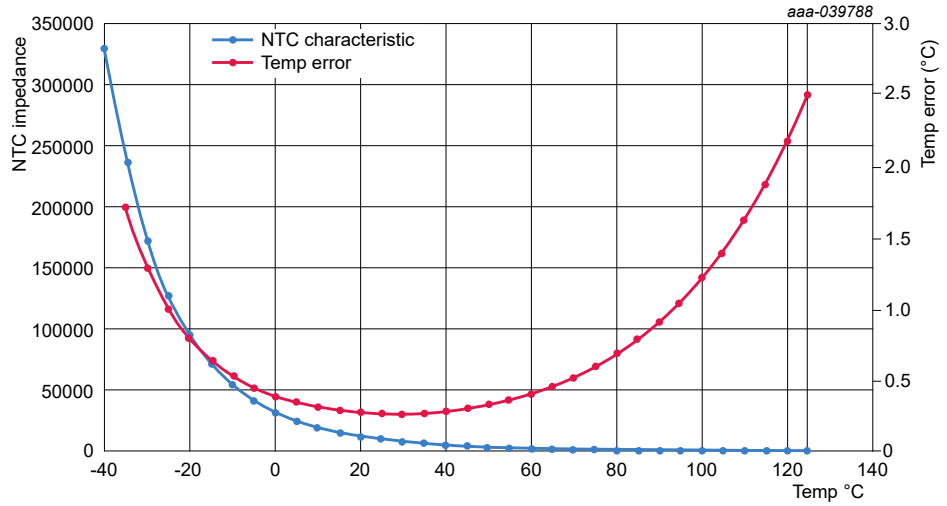

Figure 10. Temperature accuracy

4.4 Safety mechanisms - recommendations

Two safety mechanisms are available for the GPIOx that are configured as analog inputs. Refer to safety manuals for more details and how to execute.

4.4.1 SM05: GPIOx OT/UT functional verification

To functionally verify OT/UT detections, the Anx/GPIOx CMOS output buffers can be individually activated high or low, forcing the Anx voltage to be GND or VCOM. Please refer to safety manuals for complete procedure description.

When the voltage is forced, the Clpft capacitor will be charged from VCOM or discharged to AGND with no current limitation through the internal buffer. To avoid any damage of the internal circuit, the Clpft capacitor should not exceed 10 nF.

4.4.2 SM06: GPIOx Open Terminal (Open Line) Diagnostics

To detect open terminals on a GPIO pin, a weak internal pull-down resistor (Ropenpd min 3.8 KΩ max 6.2 KΩ) is commanded ON during the execution of the safety mechanism.

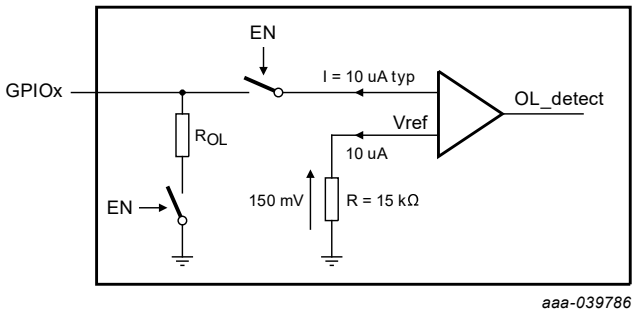

Figure 11. GPIO OL subcircuit

An internal pull-up current of 10 µA typical is generated and bias Ropenpd resistor. An open terminal is detected if the voltage value across Ropenpd is below Vol(th) (0.15 V typ).

With the recommended data sheet schematic, NCPxxxXEV103 10K NTC, and worst case regarding the MC33771/2B/C, the safety mechanism should be executed below 90 °C; Above that temperature, false alarms might be triggered.

This safety mechanism is not intended to detect NTC disconnection, only a GPIO pin disconnection. NTC disconnection is equivalent to an out-of-range low temperature that can be detected using a plausibility check during normal temperature acquisition.

With a 100K NTC thermistor, Rtc has to be calculated to allow executing the safety mechanism in the desired temperature range. For instance, with Rtc = 47 KΩ worst case configuration (Ropenpd = 3800 Ω and Vol(th) = 230 mV), the safety mechanism will work up to 65 °C.

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