QN902X

Hardware Application Note

Rev 1.1 — April 2018 | Application note

Document information

Info	Content
Keywords	Power, Clocks, PCB
Abstract	This document is the application note for hardware design with QN902x.

Revision history

Rev	Date	Description
0.1	20130418	Initial release
0.2	20130522	Add QN9021 reference design;
0.3	20130606	Add QN9020 typical application design schematic
0.4	20130708	Modify the pin name IDC to DCC in figure 9,10,11,12,13
0.5	20130715	Update the RF matching net components value
0.51	20130729	Update the parameter's with crystal Add GPIO description
0.52	20130812	Update load capacitor value of 32.768 kHz crystal
0.6	20130827	Update the Bill Of Material
0.7	20140116	Suggested a 10uF capacitor to connect the pin1 of QN9020
0.8	20140517	Swap the pin XTAL1 and XTAL2 in schematic Update the parameters for crystal's selecting
0.9	20140704	Update the table of GPIO's define
1.0	20150512	Refine some description and migrate to NXP template
1.1	20180423	Added Section 2.4, "Fast boot"

Contents

Date of release: April 2018
Document identifier: AN11814

1. Introduction

The QN902x is an ultra-low power, high-performance, and highly integrated Bluetooth Low Energy (BLE) SoC with few external components.

1.1 Purpose

This document is the application note for a hardware design with QN902x.

2. Hardware design

2.1 Power supply

The QN902x has an integrated a voltage regulator. There are two typical solutions for the QN902x power supply connection.

2.1.1 Using external power supply directly

If using the external power supply directly, all the QN902x power pins should be connected to the external power supply. See the schematics in Fig 10 or Fig 12. The voltage range should be between 2.4 V~3.6 V. For the best performance, the 100-nF decupling capacitors should be on the power supply pins. A 10-µF capacitor should be connected to pin1 of the QN9020 to filter the ripple of the power supply.

2.1.2 Using internal DC-DC converter

Using an internal integrated DC-DC converter helps to further reduce the current consumption. The DC-DC converter generates the required voltage from VCC (pin1 on QN902x) and outputs the voltage at the DCC pin (pin48 in QN9020 or pin32 in QN9021). The DCC pin connects the DC–DC converter circuit to supply the voltage for the three QN9020 power pins (VDD1, VDD2, VDD3). Fig 1 shows the DCC pin (pin48 in QN9020 or pin32 in QN9021) connection in the schematic.

The DCC pin needs a 10-µH inductor and a 15-nH inductor in series and a 1-µF decupling capacitor in parallel. The 15-nH inductor and the 1-µF decupling capacitor filter the noise from the DC-DC converter. All the three components should be placed close to the DCC pin.

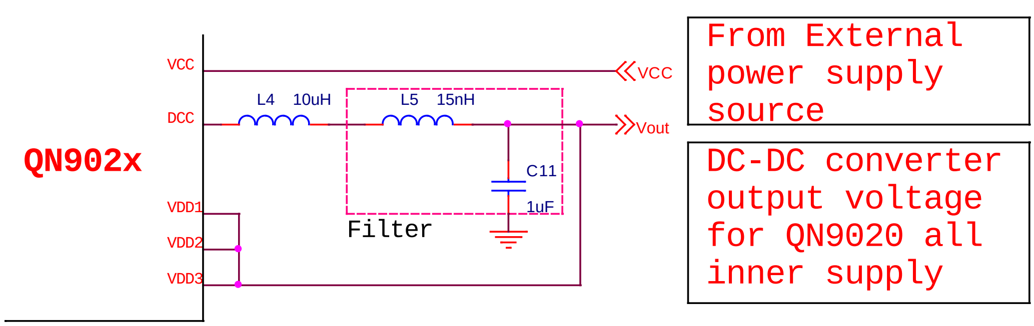

Fig 1. Using internal integrated DC-DC converter reference schematic

2.2 Clocks

Two clocks are required by the QN902x: a 16/32-MHz high-frequency clock and a 32.768-kHz low-frequency clock (RTC).

2.2.1 High-frequency clock

A high-frequency crystal provides the system clock, which accepts a 16/32-MHz external crystal with a ±50 ppm accuracy. Higher accuracy increases the success rate of sending or receiving packets. If possible, use a 20-ppm accuracy crystal. The QN902x has the load capacitances integrated internally. The parameters for crystals' selection are in Table 1.

Table 1. High-frequency crystal selection

Frequency	Accuracy	Load capacitance	Equivalent series Resistance max (Ω)
16/32 MHz	<±50 ppm	8 pF	50

The QN902x also accepts external clock inputs.

- Square clock. For the square wave as the clock input, the voltage range is between 0~VCC.
- Sin wave. For the sin wave as the clock input, the voltage should be higher than 350 mV peak and it should be AC coupled.

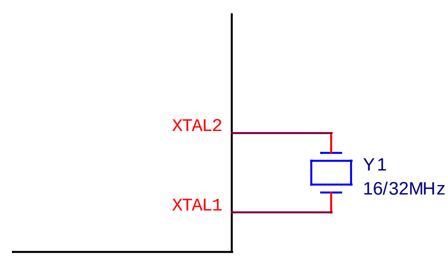

Fig 2. Crystal input interface with no external load capacitance

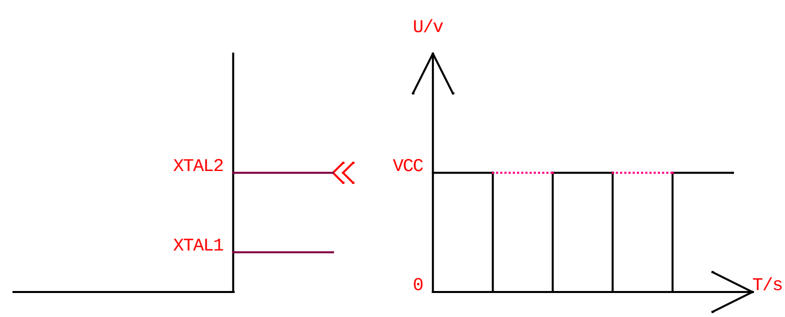

Fig 3. External square wave clock input interface

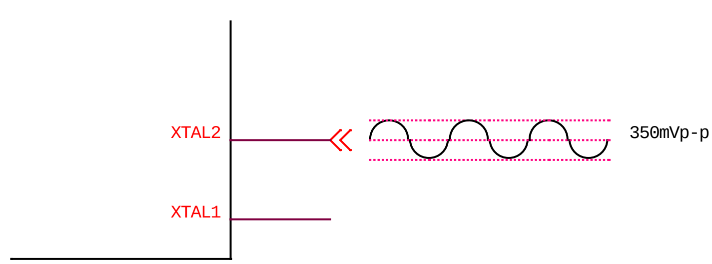

Fig 4. External sin wave clock input interface

2.2.2 Low-frequency clock

- The external 32.768-kHz crystal is used when accurate timing is needed.
- The 32-kHz internal RC oscillator can reduce the cost and power consumption if accurate timing is not a priority.

The parameters for the external 32.768-kHz crystal selection are shown in Table 2. The recommend accuracy is 20 ppm.

Table 2. Low-frequency crystal selection

Frequency	Accuracy
32.768 kHz	<±100 ppm

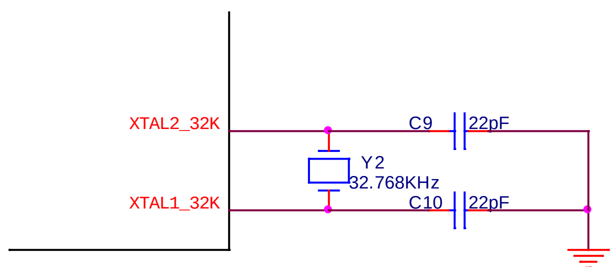

Fig 5. 32.768-kHz crystal circuit

2.3 Reset circuit

The reset pin of the QN902x is RSTN. It is logic low for reset. For normal use, it should be connected to logic high. Connect this pin to the RC reset circuit for the power-on reset. The recommended values for the resistor (Rres) and capacitor (Cres) should be 100 kΩ and 1 μF.

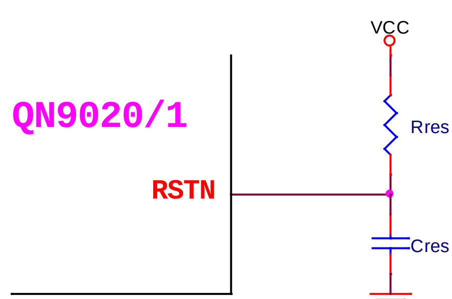

Fig 6. RC reset circuit

2.4 Fast boot

The QN9020 version E has a fast boot function. There is a hardware pin (p2.6) which is used to set the fast boot. When enabled (the pin is pulled up), the QN9020 starts in the fast boot mode without the ISP waiting time.

Note: When the fast boot function is enabled, the ISP waiting process is also ignored. Pull down the pin of P2.6 to perform the ISP operation.

2.5 GPIO's define

Pin_ctrl	0	1	2	3	pin num
[1:0]	GPIO0	UART0_TXD	SPI0_DAT	RSVD	P0_0
[3:2]	GPIO1	RSVD	SPI0_CS0	UART0_CTSn	P0_1
[5:4]	GPIO2	I2C_SDA	SPI0_CLK	UART0_RTSn	P0_2
[7:6]	GPIO3	RSVD	CLKOUT0	TIMER0_eclk	P0_3
[9:8]	GPIO4	RSVD	CLKOUT1	RSVD	P0_4
[11:10]	GPIO5	I2C_SCL	ADC Trig	ACMP1_out	P0_5
[13:12]	SW_DAT	GPIO6	AIN2	ACMP1-	P0_6
[15:14]	SW_CLK	GPIO7	AIN3	ACMP1+	P0_7
[17:16]	GPIO8	SPI1_DIN	UART1_RXD	TIMER2_eclk	P1_0
[19:18]	GPIO9	SPI1_DAT	UART1_TXD	TIMER1_0_out	P1_1
[21:20]	GPIO10	SPI1_CS0	UART1_CTSn	ADC Trig	P1_2
[23:22]	GPIO11	SPI1_CLK	UART1_RTSn	CLKOUT1	P1_3
[25:24]	GPIO12	RSVD	RSVD	TIMER1_3	P1_4
[27:26]	GPIO13	RSVD	PWM1	TIMER1_2	P1_5
[29:28]	GPIO14	SPI0_CS1	PWM0	TIMER0_3	P1_6
[31:30]	GPIO15	UART0_RXD	SPI0_DIN	TIMER0_0	P1_7
[33:32]	GPIO16	SPI1_DIN	UART1_RXD	TIMER3_2	P2_0
[35:34]	GPIO17	SPI1_DAT	UART1_TXD	TIMER3_1	P2_1
[37:36]	GPIO18	SPI1_CLK	UART1_RTSn	TIMER2_3	P2_2
[39:35]	GPIO19	I2C_SDA	ACMP0_out	TIMER3_0	P2_3
[41:40]	GPIO20	I2C_SCL	PWM1	TIMER3_eclk	P2_4
[43:42]	GPIO21	SPI1_CS1	RSVD	TIMER2_2	P2_5
[44:43]	GPIO22	RSVD	PWM1	TIMER2_0	P2_6
[46:45]	GPIO23	ACMP1	PWM0	TIMER1_eclk	P2_7
[48:47]	GPIO24	TIMER2_1	AIN0	ACMP0-	P3_0
[50:49]	GPIO25	TIMER0_2	AIN1	ACMP0+	P3_1
[52:51]	GPIO26	SPI0_DIN	RSVD	ACMP0_out	P3_2
[54:53]	GPIO27	SPI0_DAT	CLKOUT0	RSVD	P3_3
[56:55]	GPIO28	SPI0_CLK	RSVD	RSVD	P3_4
[58:57]	GPIO29	SPI0_CS0	RSVD	TIMER0_0	P3_5
[60:59]	GPIO30	SPI1_CS0	UART1_CTSn	RSVD	P3_6

Most GPIOs have four defined functions and can be multiplexed by the registers' configuration.

Only pins P0_0 to P1_7 can be used as wakeup sources.

Only the pins highlighted in red are shared with the QN9021 QFN5x5 package.

2.6 RF matching circuit

The QN902x radio transceiver requires a matching network to match the 50-Ω impedance. The structure of the matching network is shown in Fig 7 and Fig 8. For all values in the matching network, see the BOM list (Table 3 and Table 4).

The components of the matching circuit should be placed as close to the corresponding pins as possible.

The 50-Ω RF trace between the antennas (or SMA connectors) and the matching circuit should be as short as possible.

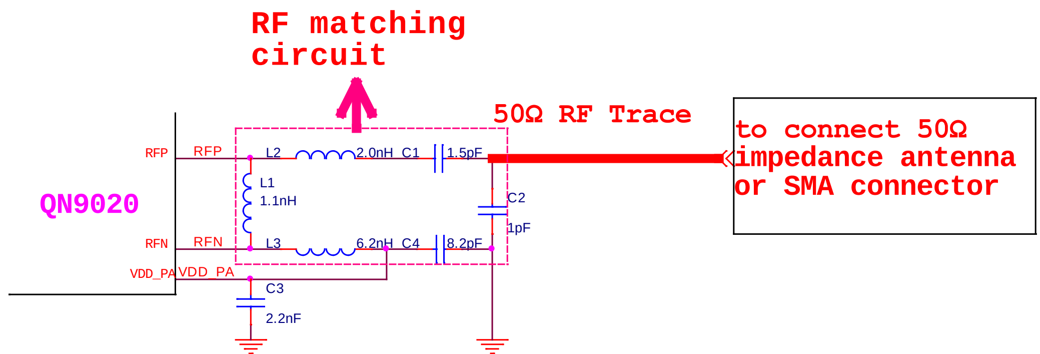

Fig 7. QN9020 RF matching circuit

Table 3. QN9020 RF matching components value

Part name	Part number	Value	Size
Inductor L1	LQP15MN1N1B02	1.1 nH	0402
Inductor L2	LQP15MN2N0B02	2.0 nH	0402
Inductor L3	LQP15MN6N2B02	6.2 nH	0402
Capacitor C1	GRM1555C1H1R5CA01	1.5 pF	0402
Capacitor C2	GRM1555C1H1R0CA01	1.0 pF	0402
Capacitor C4	GRM1555C1H8R2DA01	8.2 pF	0402
Capacitor C3	GRM155R71H222KA01	2.2 nF	0402

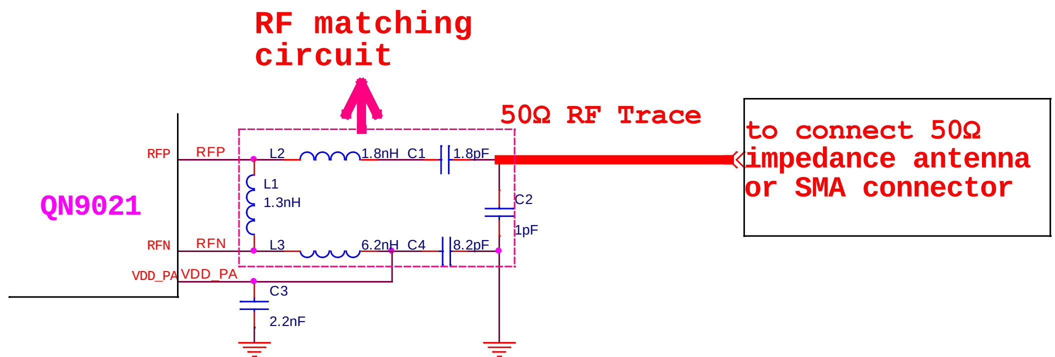

Fig 8. QN9021 RF matching circuit

Table 4. QN9021 RF matching components value

Part name	Part number	Value	Size
Inductor L1	LQP15MN1N3B02	1.3 nH	0402
Inductor L2	LQP15MN1N8B02	1.8 nH	0402
Inductor L3	LQP15MN6N2B02	6.2 nH	0402
Capacitor C1	GRM1555C1H1R8CA01	1.8 pF	0402
Capacitor C2	GRM1555C1H1R0CA01	1.0 pF	0402
Capacitor C4	GRM1555C1H8R2DA01	8.2 pF	0402
Capacitor C3	GRM155R71H222KA01	2.2 nF	0402

2.7 AN Hardware reference design

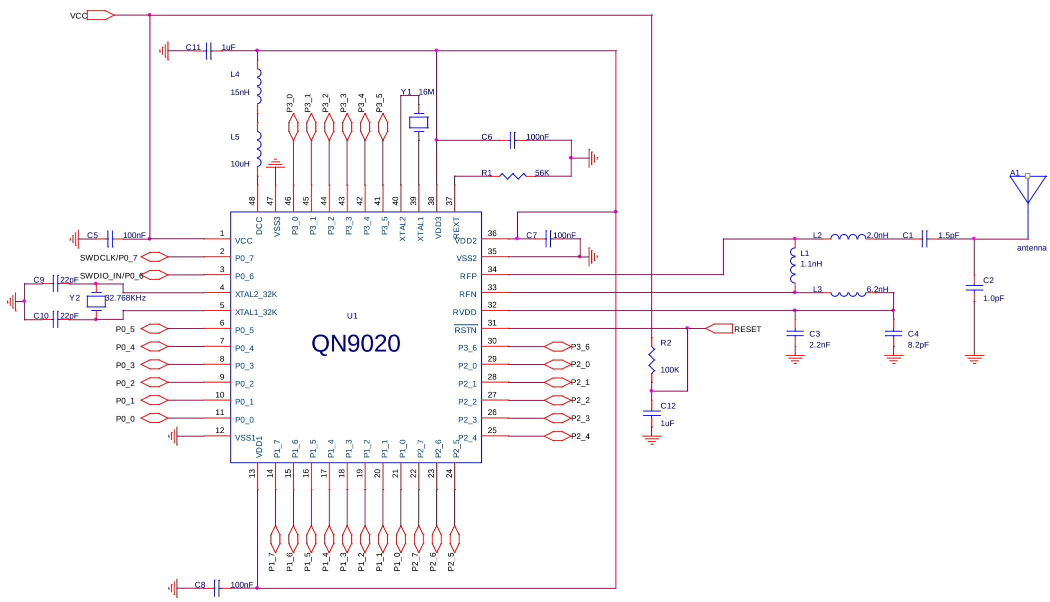

Fig 9. QN9020 with DC-DC converter reference design schematic

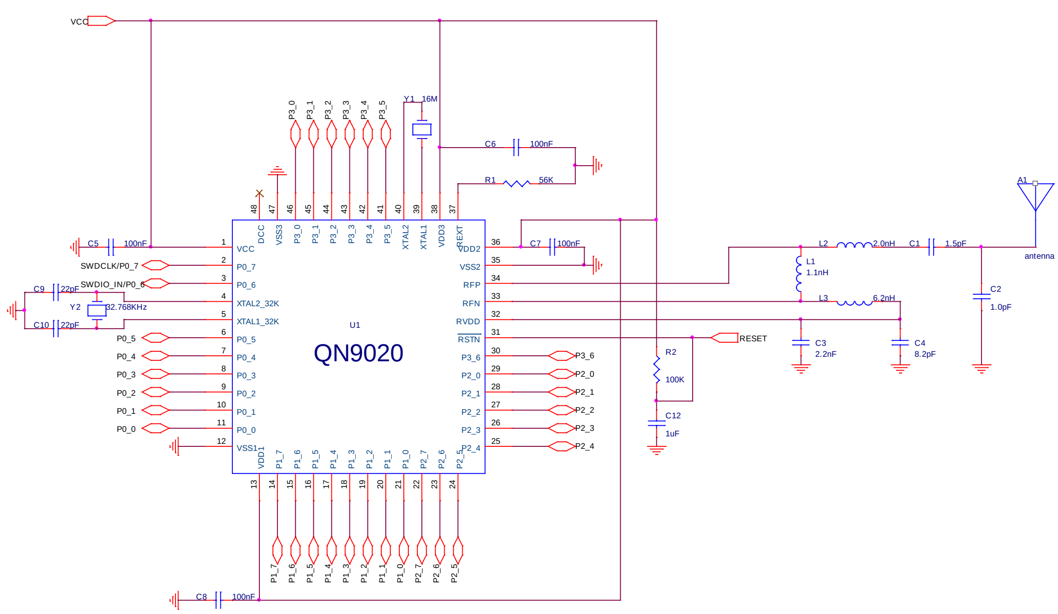

Fig 10. QN9020 without DC-DC converter reference design schematic

All information provided in this document is subject to legal disclaimers.

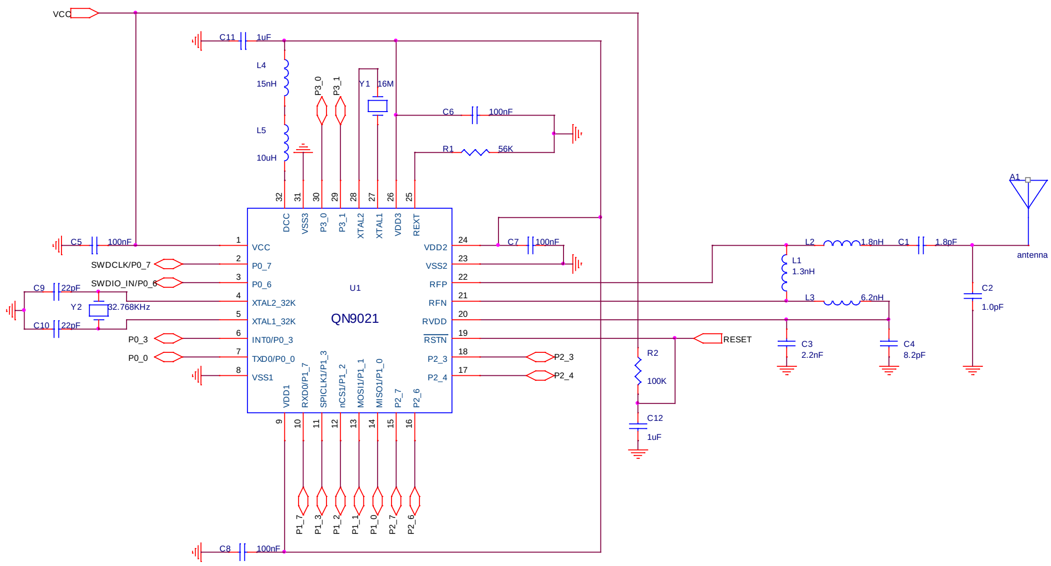

Fig 11. QN9021 with DC-DC converter reference design schematic

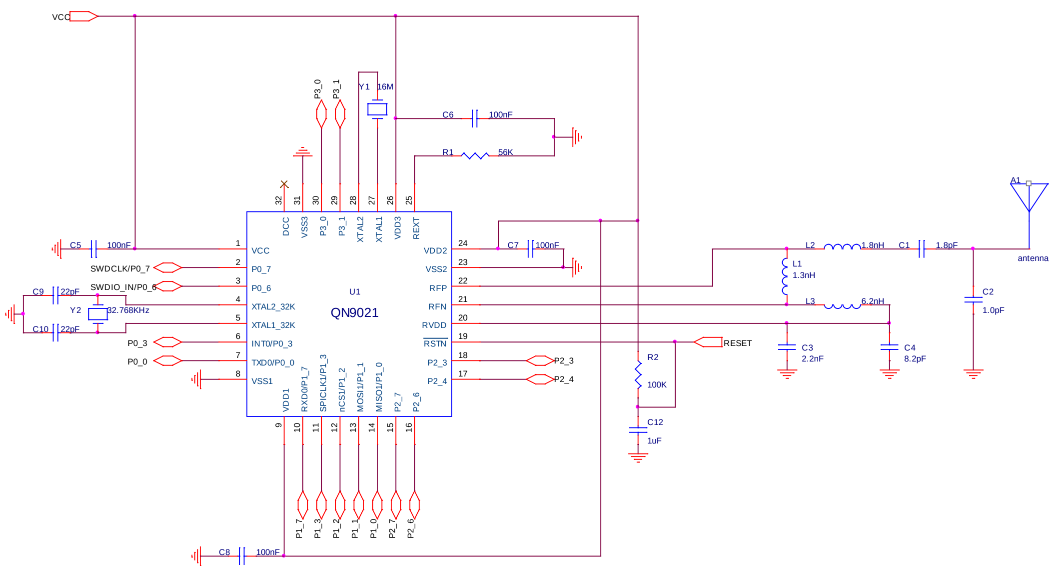

Fig 12. QN9021 without DC-DC converter reference design schematic

2.8 QN9020 typical application design schematic

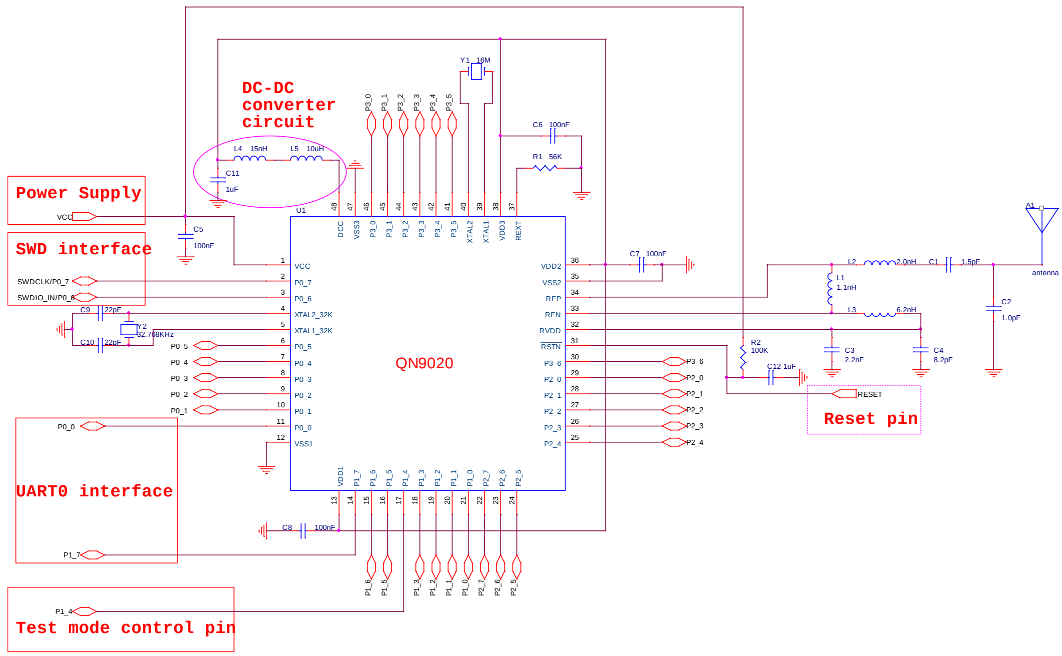

Fig 13. QN9020 typical application design schematic

Note:

- The VCC (pin1) must connect an external power supply.
- The reset pin (pin21) is an input pin used for the QN9020 hardware reset. When it is logical low, it can force the QN9020 to reset.
- When the GPIO P1.4 (pin17) is configured as an input and inputs logical low, it can force the QN9020 to enter the test mode.
- The UART0 or SWD interface, together with the Reset, can be used for the QN9020 to download a program.

Make sure you connect these pins out to interface pads for your production testing and debugging purposes.

2.9 Bill of material

Table 5. Bill of materials for QN9020 with DC-DC converter reference design

QN9020_48 with DC converter reference design BOM					
Item	**Part description**	**Footprint**	**Reference**	**Qty**	**Part no.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11,C12	2	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	—
5	R_SMD,100K, ±5%, 0402	0402	R2	1	—
Inductor					
6	L_SMD,15nH,5%,0402	0402	L4	1	LQG15HN15NJ02
7	L_SMD,10uH,5%,0603	0603	L5	1	LQM18FN100M00D
Oscillator					
8	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
9	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
10	IC, 2.4G SOC, 64KB system memory, QFN48,QN9020	QFN48	U1	1	QN9020
RF circuit					
11	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
12	L_SMD, 2.0nH, ±0.1nH,0402	0402	L2	1	LQP15MN2N0B02
13	L_SMD, 1.1nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N1B02
14	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
15	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
16	C_SMD, 1.5pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R5CA01
17	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
18	Antenna	—	A1	1	—

Table 6. Bill of materials for QN9020 without DC-DC converter reference design

QN9020_48 without DC converter reference design BOM					
Item	**Part description**	**Footprint**	**Reference**	**Qty**	**Part no.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11	1	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	—
5	R_SMD,100K, ±5%, 0402	0402	R2	1	—
Oscillator					
6	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
7	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
8	IC, 2.4G SOC, 64KB system memory, QFN48,QN9020	QFN48	U1	1	QN9020
RF circuit					
9	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
10	L_SMD, 2.0nH, ±0.1nH,0402	0402	L2	1	LQP15MN2N0B02
11	L_SMD, 1.1nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N1B02
12	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
13	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
14	C_SMD, 1.5pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R5CA01
15	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
16	Antenna	—	A1	1	—

Table 7. Bill of materials for QN9021 with DC-DC converter reference design

QN9021_32 with DC converter reference design BOM					
Item	**Part description**	**Footprint**	**Reference**	**Qty**	**Part no.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11,C12	2	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	—
5	R_SMD,100K, ±5%, 0402	0402	R2	1	—
Inductor					
6	L_SMD,15nH,5%,0402	0402	L4	1	LQG15HN15NJ02
7	L_SMD,10uH,5%,0603	0603	L5	1	LQM18FN100M00D
Oscillator					
8	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
9	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
10	IC, 2.4G SOC, 64KB system memory, QFN32,QN9021	QFN32	U1	1	QN9021
RF circuit					
11	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
12	L_SMD, 1.8nH, ±0.1nH,0402	0402	L2	1	LQP15MN1N8B02
13	L_SMD, 1.3nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N3B02
14	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
15	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
16	C_SMD, 1.8pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R8CA01
17	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
18	Antenna	—	A1	1	—

Table 8. Bill of materials for QN9021 without DC-DC converter reference design

QN9021_32 without DC converter reference design BOM					
Item	**Part description**	**Footprint**	**Reference**	**Qty**	**Part no.**
Capacitor					
1	C_SMD, 100nF, X7R, ±10%, 16V, 0402	0402	C5,C6,C7,C8	4	GRM155R71C104KA88
2	C_SMD,1uF, X5R, ±10%, 6.3V, 0402	0402	C11	1	GRM155R60J105KE19
3	C_SMD, 22pF, NP0, 5%, 50V, 0402	0402	C9,C10	2	GRM1555C1H220JA01
Resistor					
4	R_SMD,56K, ±1%, 0402	0402	R1	1	—
5	R_SMD,100K, ±5%, 0402	0402	R2	1	—
Oscillator					
6	Crystal, 16MHz, ±20ppm, 12pF, 2.5x2.0x0.55 mm	SMD_2520	Y1	1	FA-20H
7	Crystal, 32.768K, ±20ppm, 15pF, 2.0x1.2x0.6 mm	SMD_2012	Y2	1	FC-12M
IC					
8	IC, 2.4G SOC, 64KB system memory, QFN32,QN9021	QFN32	U1	1	QN9021
RF circuit					
9	L_SMD, 6.2nH, ±0.1nH,0402	0402	L3	1	LQP15MN6N2B02
10	L_SMD, 1.8nH, ±0.1nH,0402	0402	L2	1	LQP15MN1N8B02
11	L_SMD, 1.3nH, ±0.1nH,0402	0402	L1	1	LQP15MN1N3B02
12	C_SMD, 2.2nF, X7R, ±10%, 50V, 0402	0402	C3	1	GRM155R71H222KA01
13	C_SMD, 8.2pF, COG, ±0.5pF, 50V, 0402	0402	C4	1	GRM1555C1H8R2DA01
14	C_SMD, 1.8pF, COG, ±0.25pF, 50V, 0402	0402	C1	1	GRM1555C1H1R8CA01
15	C_SMD, 1.0pF, COG, ±0.25pF, 50V, 0402	0402	C2	1	GRM1555C1H1R0CA01
Others					
16	Antenna	—	A1	1	—

3. QN902x PCB layout

3.1 PCB stack-up

The recommended PCB stack-up for the QN902x application is shown in Fig 14.

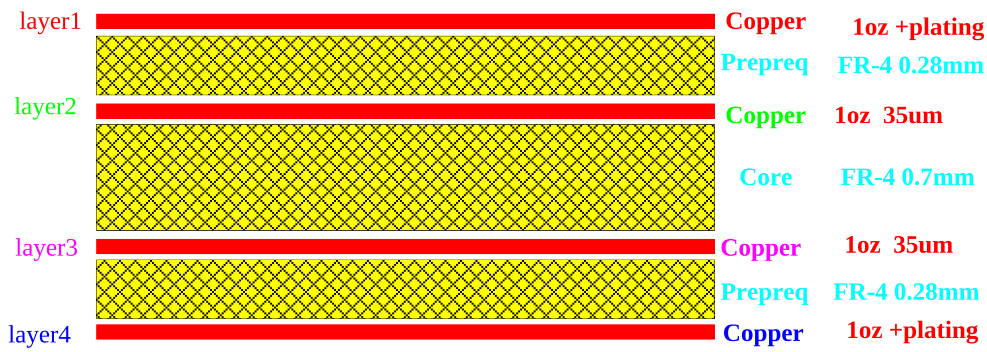

Fig 14. PCB stack-up

The PCB board is 1.5 mm thick and based on a standard flame retardant (FR4) material.

3.2 RF interface

Because the QN902x works at 2.4 GHz, the parasitic parameters from the Printed Circuit Board (PCB) layout affect the RF parameters and it is very sensitive. Pay attention to these details:

- Route the RF traces on the top layer and keep the traces as short as possible (no vias are allowed on the trace).
- The impedance of the RF trace between the matching network and antenna (or the SMA connector) must be 50 Ω. There should be a large, unbroken, and solid ground under this RF trace. There should be a via around the RF trace with high density.
- When the PCB has multiple layers (more than two layers), remove the ground plane on the internal layers under the RF components. Just keep the bottom layer's ground plane for shielding.
- There should be a distance between the components and the ground plane on the top layer.
- No other signal trace is allowed under the RF components and the RF traces.
- The L1 should be placed as close to the QN902x RF port as possible to reduce parasitic capacitance.

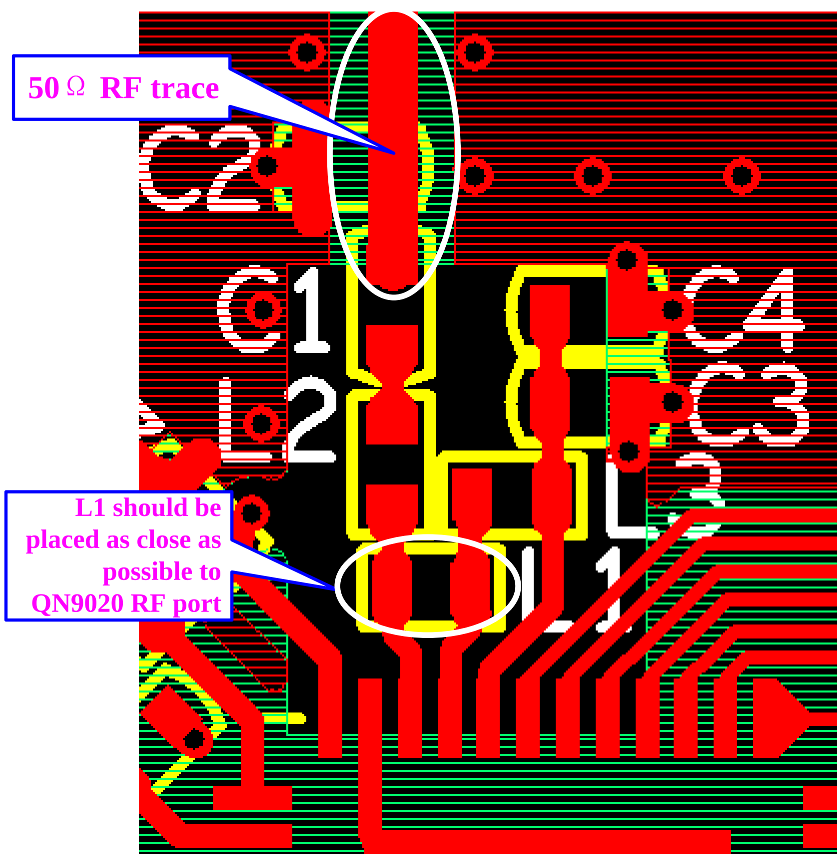

Fig 15. QN902x RF layout

3.3 Clock

If a crystal is used, the parasitic characteristics of the clock trace influence the circuit. Keep the trace as short as possible. Keep the ground plane under the crystal trace to improve the return path. Avoid crossing the crystal trace between the layers.

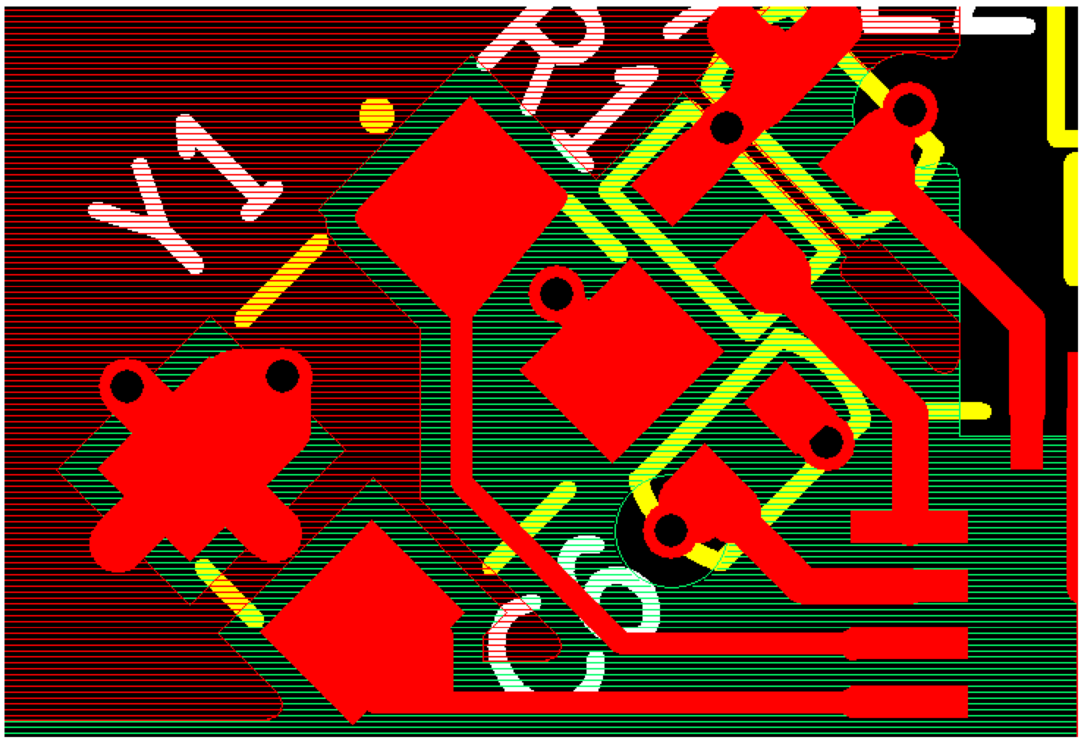

Fig 16. QN902x 16/32M clock layout

3.4 With DC-DC converter

The DC-DC converter generates noise. Place the DC-DC converter components as close to the QN902x device as possible. Make sure that the DC-DC converter output trace is wide enough. The trace must be kept as short as possible. Keep the useful signal trace far from the DC-DC converter routing area.

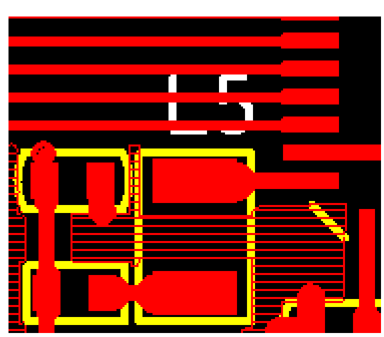

Fig 17. QN902x with DC-DC converter layout

3.5 AN Example of PCB layout

Qn9020 EVB layout

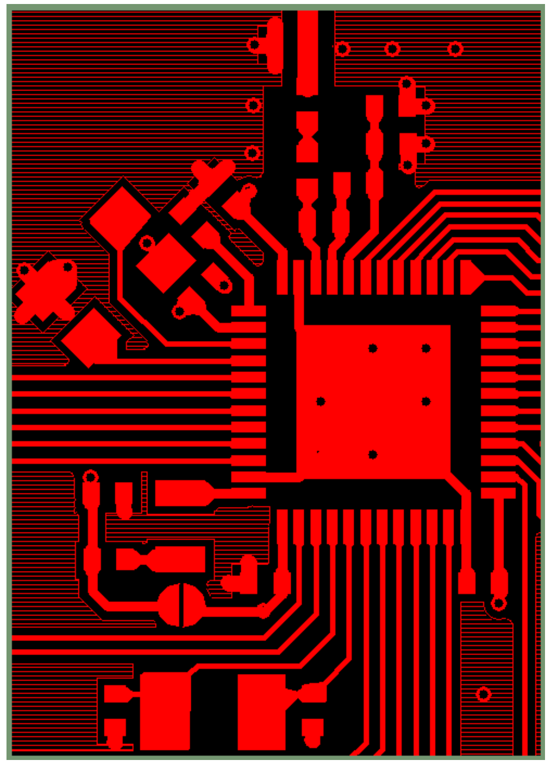

Fig 18. QN902x layer 1

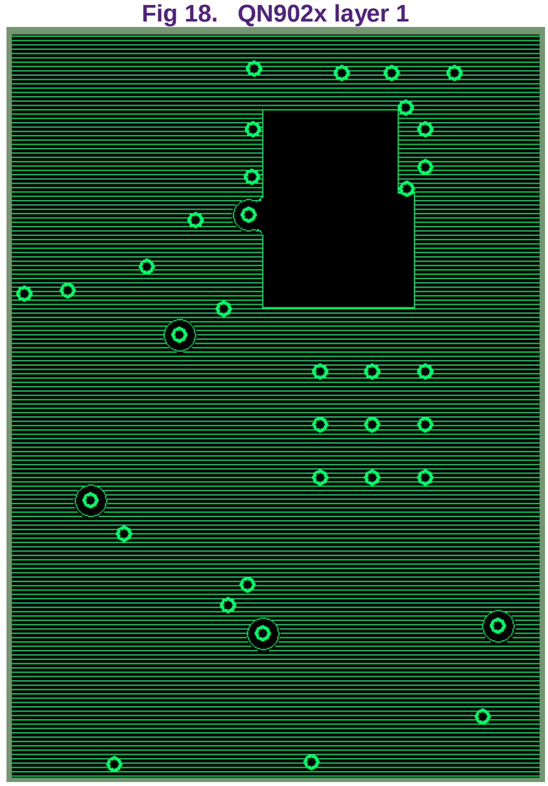

Fig 19. QN902x layer 2

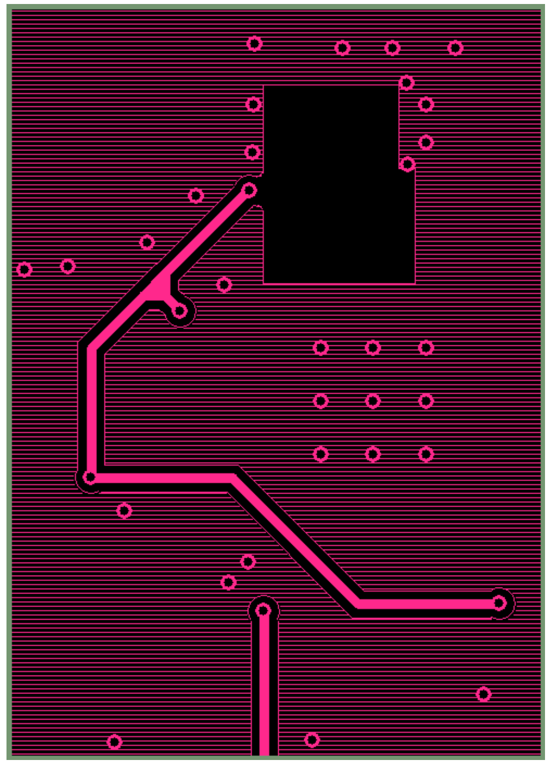

Fig 20. QN902x layer 3

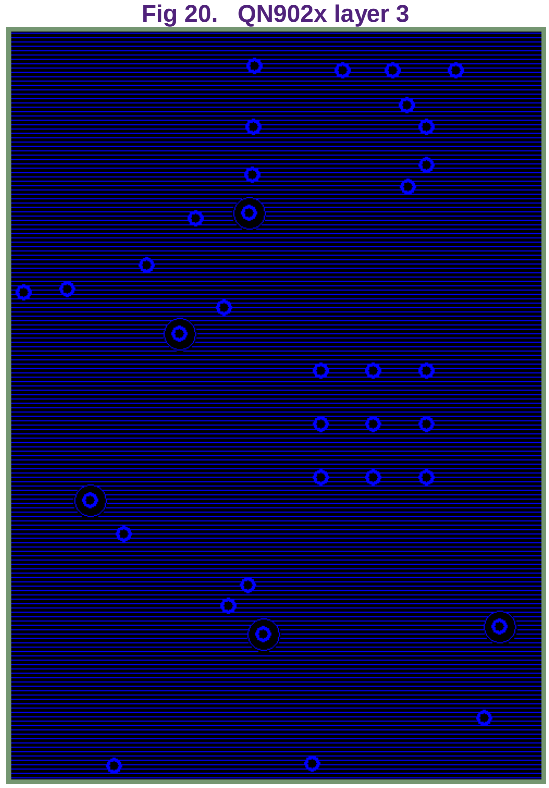

Fig 21. QN902x layer 4

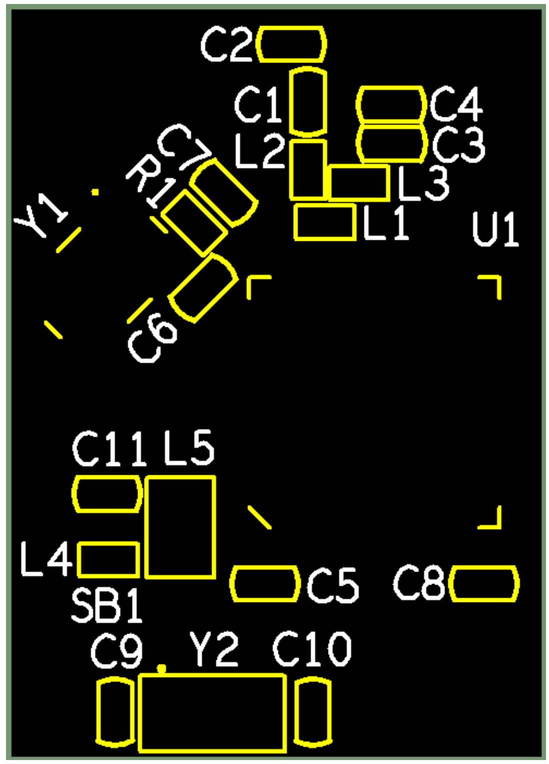

Fig 22. QN902x SILK TO

QN9021 EVB layout

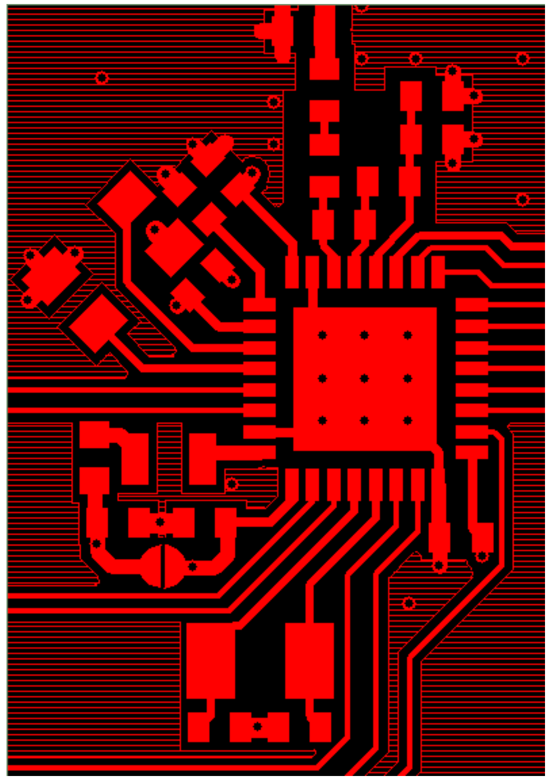

Fig 23. QN9021 layer 1

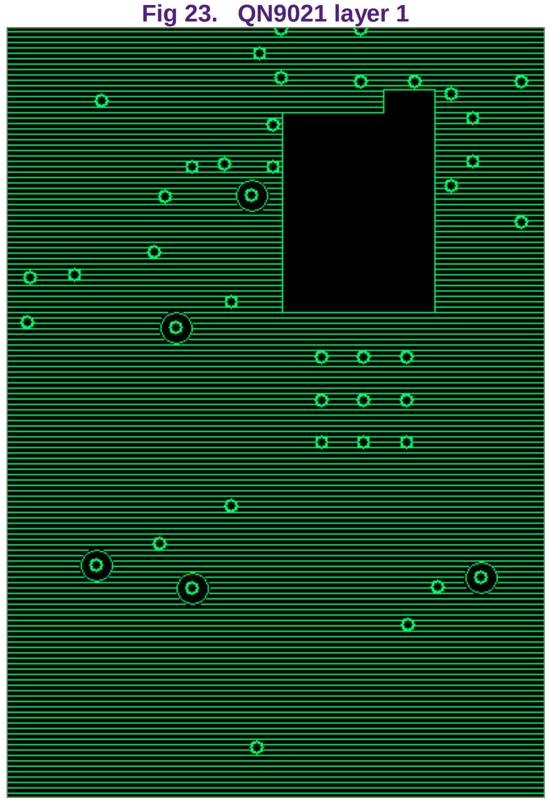

Fig 24. QN9021 layer 2

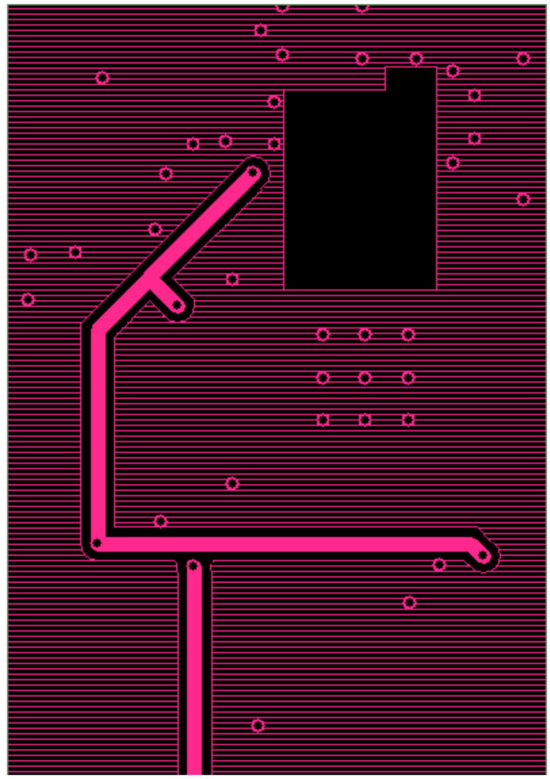

Fig 25. QN9021 layer 3

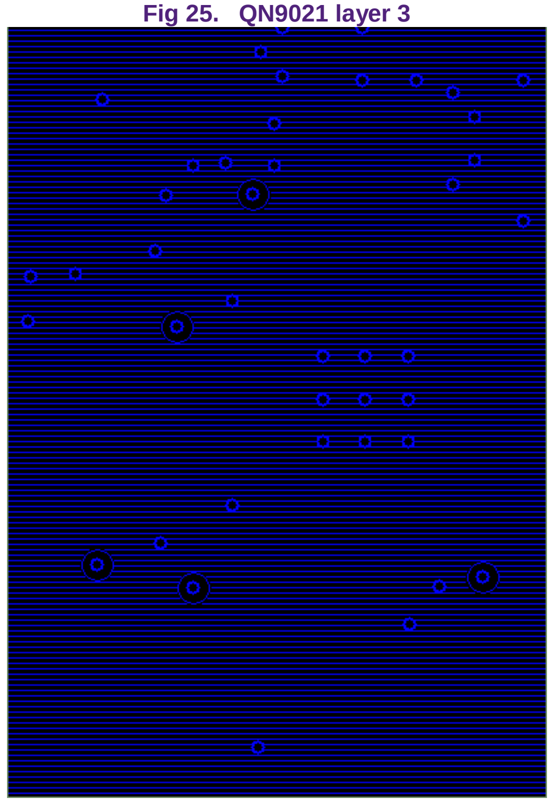

Fig 26. QN9021 layer

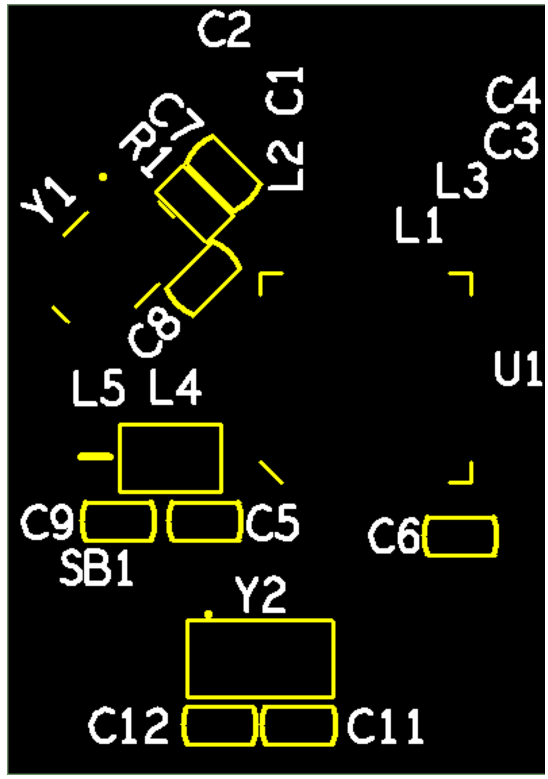

Fig 27. QN9021 SILK TOP

4. Legal information

4.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

4.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

5. List of figures

6. List of tables