

AN11564

PN7120 Antenna Design and Matching Guide

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Application note
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Document information

Info	Content
Keywords	PN7120, NFC, Antenna Design, Antenna matching/tuning
Abstract	<p>This application note is intended to provide some guidelines regarding the way to design an NFC antenna for the PN7120 chip.</p> <p>It also explains how to determine the tuning/matching network to place between this antenna and the PN7120.</p> <p>Standalone antenna performances evaluation and final RF system validation (PN7120 + tuning/matching network + NFC antenna within its final environment) are also covered by this document.</p>



Revision history

Rev	Date	Description
1.1	20160418	<ul style="list-style-type: none">Added description of CLIF_ANA_TX_SHAPE_CONTROL_REG registerSection: 9.3: License statement updated
1.0	20150408	First official release

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1. Introduction

The PN7120 is a highly integrated NFC transceiver IC for contactless communication at 13.56 MHz. This transceiver IC utilizes an outstanding modulation and demodulation concept completely integrated for different kinds of contactless communication methods and protocols at 13.56 MHz.

It can operate both in reader/poller mode and in card/listener mode.

The PN7120 is intended to be connected to an external coil antenna through a specific matching/tuning network.

The purpose of this document is first to provide some guidelines regarding the design of an NFC antenna intended to be connected to the PN7120.

It then depicts a measurement method in order to evaluate the performances of the antenna prior to connecting it to the NXP NFC chip.

The next chapter explains how to determine the tuning/matching network to be placed between a given antenna and the PN7120 (based on the antenna electrical equivalent circuit)

Then, an RF performance validation procedure is proposed.

Finally an example of PN7120 antenna and tuning design is given as reference.

2. Antenna Design

Some of the design rules are very common for NXP NFC designs, i.e. they do neither specifically depend on the used standard (ISO, NFC or EMVCo) nor depend on the NXP Reader IC but rather on physical or technical basics.

2.1 Standard antenna design

The PN7120 can be connected to a standard antenna commonly used on the market today. Those antennas are typically constituted by a spiral loop (*single loop antenna*). The outline dimensions, the number of turns, the copper track thickness, width and spacing define the antenna characteristics.

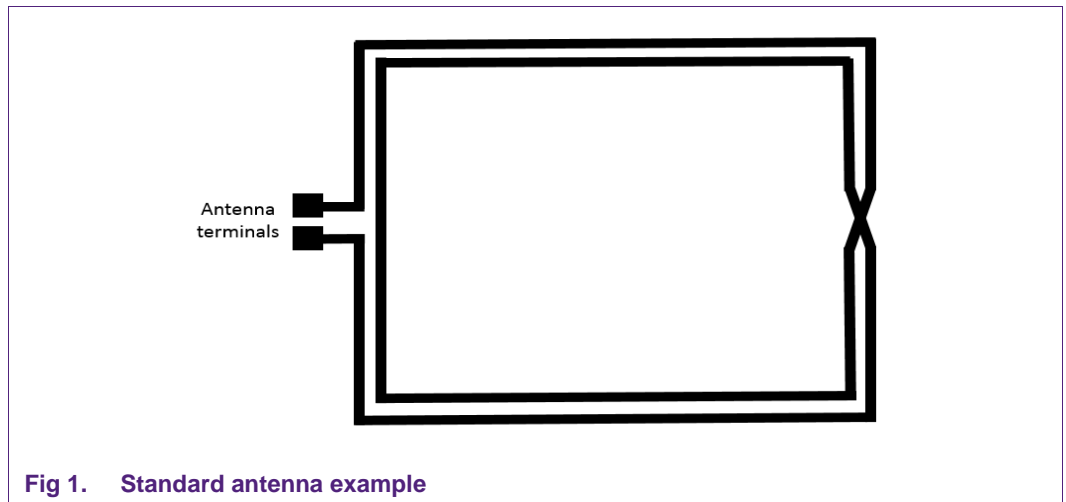


Fig 1. Standard antenna example

2.2 Shielding and environment impact

The PN7120 and the associated NFC antenna are intended to be integrated into an embedded device.

Those devices are composed of metallic parts such as the battery, the PCB, the electronic components and even sometimes the chassis.

If metal is placed close to the NFC antenna the alternating magnetic field generates some eddy currents in the metal. These eddy currents create a magnetic field in opposite direction; it absorbs power, and leads to detuning of the antenna due to a decreased inductance and quality factor. Therefore, it is necessary to shield the antenna with ferrite for proper operation in close metallic environment.

Adding a ferrite sheet allows to shield the antenna against the influence of metal.

The following figures are intended to highlight this phenomenon based on antenna field distribution simulation results. In order to simplify the simulation, the below results are based on a circular antenna with a radius of 7.5 cm with 1 turn and a copper wire of 1mm thickness. The right part shows the field distribution and the left part shows the magnitude of the field strength H over the distance d . The minimal field strength of $H_{MIN} = 1.5$ A/m defined by ISO/IEC 14443 is marked with dotted vertical line.

Fig 2 shows the field distribution in an ideal environment without any metal near the antenna.

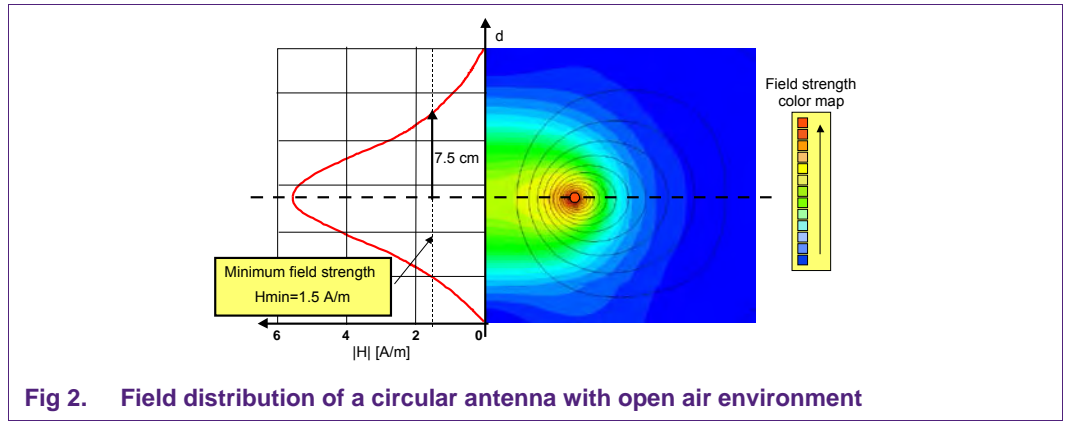


Fig 3 shows the field distribution of the same antenna but with a metal plane near to it. The magnitude of the field strength has significantly decreased compared to the open air case which leads to a decreased operating distance.

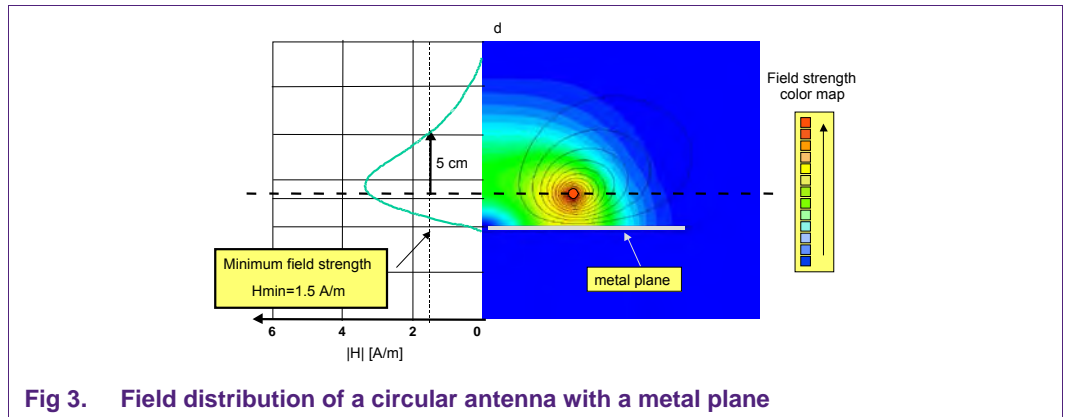
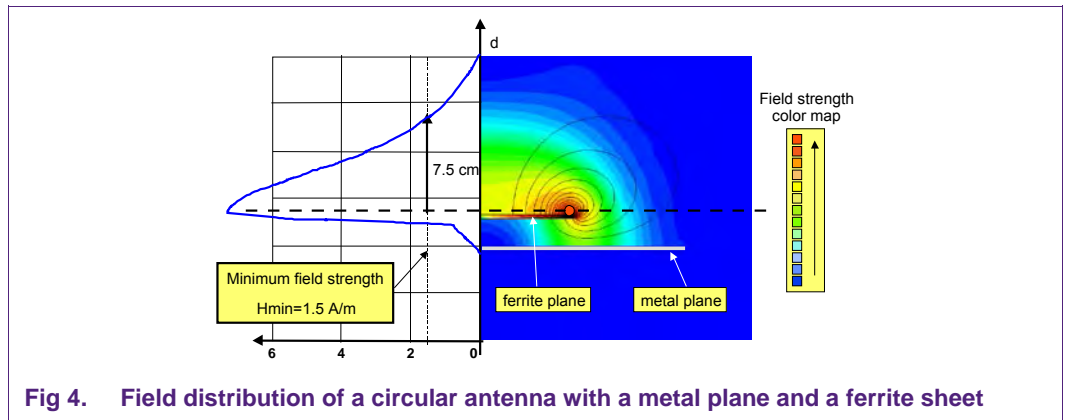


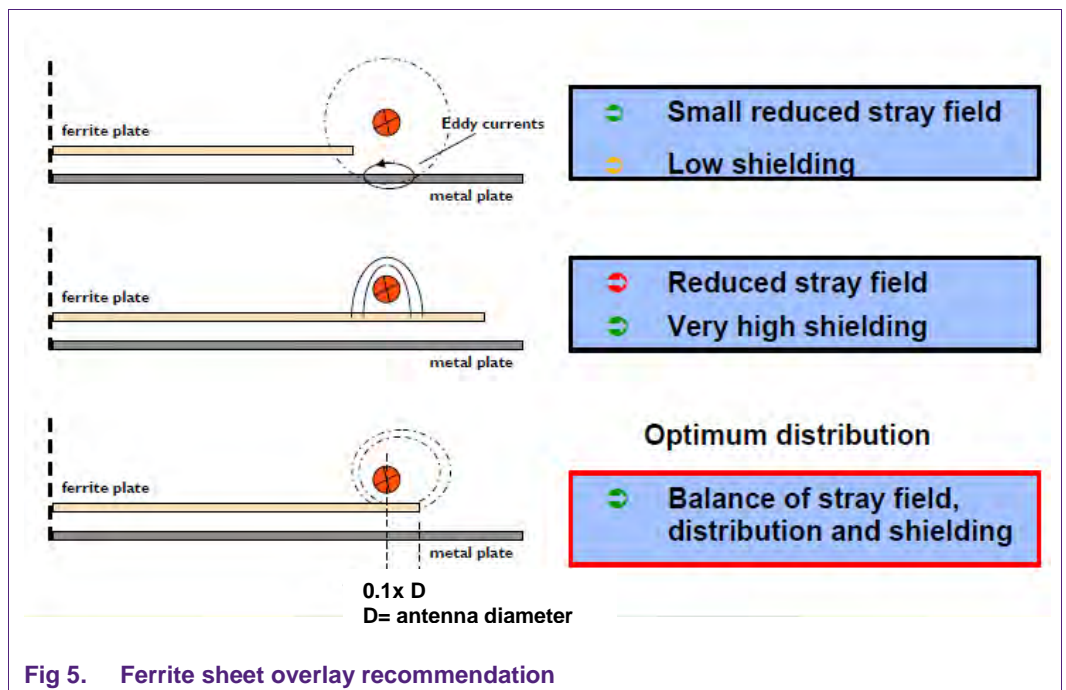
Fig 4 shows the effect of adding a ferrite plane ($\mu_R=40$) between the metal plane and the antenna coil itself. The field distribution is still modified but the operating distance recovers its original open air level.



The simulation shows that the use of a ferrite reduces the generated eddy currents in a metal plane. The ferrite sheet changes the antenna environment characteristics, which results in a fixed detuning of the antenna itself. This shielding will significantly impact the antenna electrical equivalent model so it is key that when doing PN7120 tuning/matching network calculation, the antenna model is measured with the ferrite already in place (when applicable).

2.2.1 Ferrite shielding recommendation

In order to reach a proper shielding, the ferrite sheet must at least fully cover the antenna surface. It is even needed to have an overlay but not too high because otherwise it will tend to reduce the stray field strength. This trade-off is illustrated by the picture below:



The Ferrite quality is also a key parameter which needs to be taken into account to assess the effectiveness of the shielding. A high relative permeability is recommended because it allows achieving a good shielding with a lower thickness. The material has to be specified for a high magnetic permeability in the frequency range that is involved in NFC operation, i.e. 13.56MHz. The relative magnetic permeability of a material is made of two parts: μ' is the real part of relative permeability and μ'' is the imaginary part. μ'' is reflecting the magnetic losses in the material.

Recommended values are:

$$\mu' > 40 \text{ at } 13.56\text{MHz} \text{ and } \mu'' \text{ as low as possible: ratio } \mu''/\mu' < 0.1 \text{ at } 13.56\text{MHz}.$$

Please note that the level of shielding not only depends on the material used but also on the thickness of the ferrite sheet. For a given permeability, the thickest sheet provides the strongest shielding.

3. PN7120 Antenna matching

3.1 Antenna matching circuit

On this chapter we will show the different blocks in order to do the antenna matching. Below diagram depicts typical matching/tuning circuit related to PN7120 design.

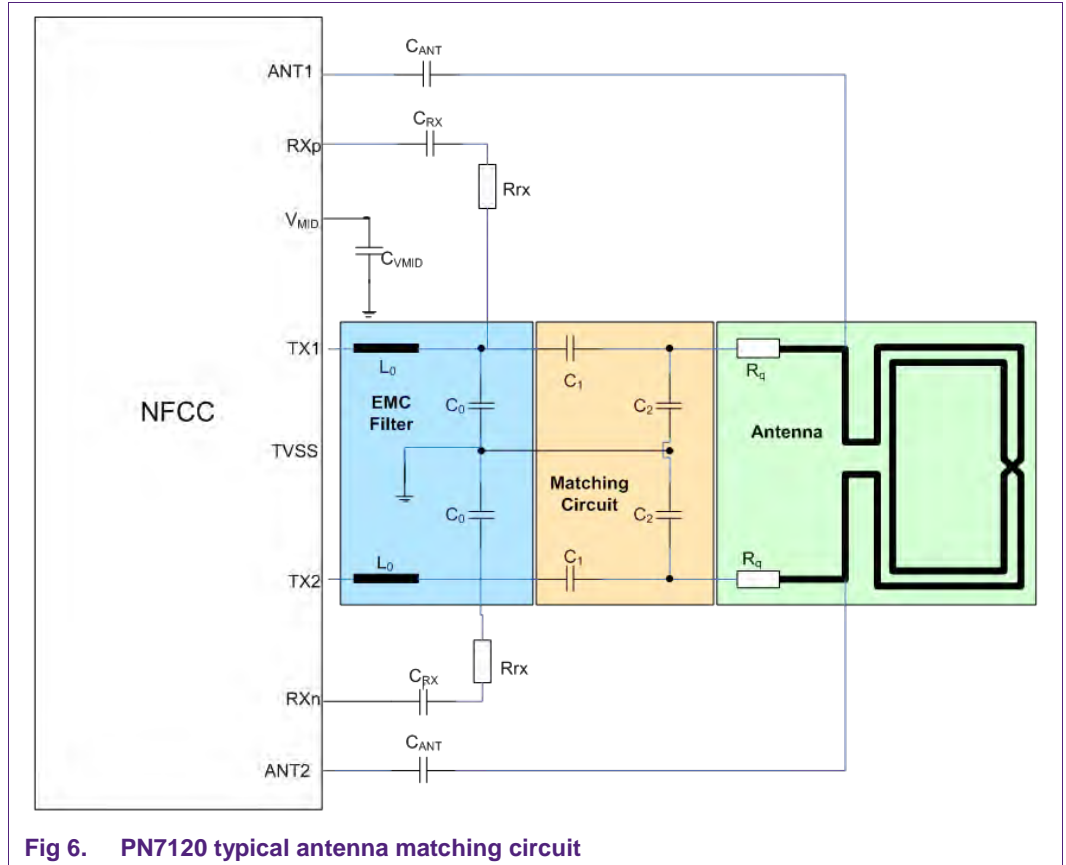


Fig 6. PN7120 typical antenna matching circuit

The process to matching the Antenna to the NFCC is composed of a matching for reader mode and a matching for card mode. The NFCC will select the reader mode matching when it is on reader mode and the card mode matching when the device is on card mode.

The matching procedure can be summarized in 5 steps. :

- 1) Determine antenna coil characteristics
- 2) Determine EMC filter cutoff frequency
- 3) Determine the matching circuit between the antenna and the EMC filter for Reader Mode.
- 4) Adapt the matching for Card Mode.
- 5) Determine the Reception block

3.2 Step 1: Antenna model measurement

Based on the antenna physical characteristics, its electrical equivalent model can be measured and computed.

For this, the antenna has to be connected to an impedance analyzer or a network analyzer to measure the series equivalent components.

Please note that the antenna equivalent circuit must be determined under the final environmental conditions especially when the antenna will be operated in metal environment or when a ferrite sheet shall be used for shielding.

The target of this modeling step is to get the L, R, C equivalent of the antenna.

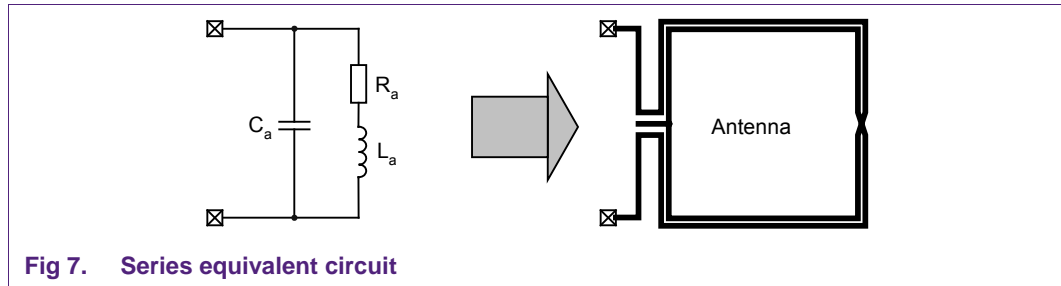


Fig 7. Series equivalent circuit

Recommended values:

$$L_a = 0.3...3\mu H$$

$$C_a = 3...30pF$$

$$R_a = 0.1...2\Omega$$

$$f_{ra} \text{ (self-resonance frequency of the antenna)} = 25\text{MHz or above}$$

The antenna parasitic capacitance C_a should be kept low to achieve a self-resonance frequency > 25 MHz as the relation linking those 2 parameters is:

$$C_a = \frac{1}{(2 \cdot \pi \cdot f_{ra})^2 L_a}$$

In order to get these antenna electrical equivalent parameters, 2 methods are proposed below depending on the available equipment:

3.2.1 Measurement method with impedance analyzer:

Some impedance analyzers like Agilent 4294A or 4395A can determine directly the series or parallel equivalent circuit by measuring the magnitude and the phase of the impedance of the connected antenna.

The antenna has to be at the final mounting position to consider all parasitic effects like metal influence on quality factor, inductance and additional capacitance.

The antenna needs to be connected to the analyzer by using an appropriate test fixture that does not influence any antenna parameters.

The analyzer has to be calibrated (open, short and load compensation at the calibration plane) and the test fixture needs to be compensated (open, short compensation at the connection points) before each measurement.

Settings: $|Z|$, \ominus

Start frequency: 1 MHz

Stop frequency: above self-resonance frequency of the antenna (point where antenna impedance is real: pure resistance)

Advantages:

- Fast and simple method

Disadvantages:

- High-end equipment required
- Low accuracy of the measurement which especially results from the loss resistance for high quality factor coils ($Q > 60$).

3.2.2 Measurement method with any network analyzer

Alternatively, a network analyzer without any equivalent circuit functionality can be used in combination with some calculation to determine the antenna electrical equivalent.

The antenna needs to be connected to the analyzer by using an appropriate test fixture that does not influence the antenna parameters.

The analyzer has to be calibrated (open, short and load compensation at the calibration plane) and the test fixture needs to be compensated (open, short compensation at the connection points) before each measurement.

Settings: S11

Chart: Smith Z

Start frequency: 1 MHz

Stop frequency: above self-resonance frequency of the antenna

4 parameters must be extracted from the above measurement in order to get the serial equivalent circuit of the antenna:

All 4 parameters are due to the geometry of the antenna, R_s is mainly defined by the thickness of the copper wire, R_p is mainly defined by the skin effect and can be changed by thickness and distance between the turns, and L_a of the antenna is a geometrical value.

Basically, increasing the number of turns increases the Q factor but decreases the effective antenna area and reduces its field strength.

R_s Equivalent resistance at $f = 1\text{MHz}$

L_a Equivalent inductance at $f = 1\text{MHz}$

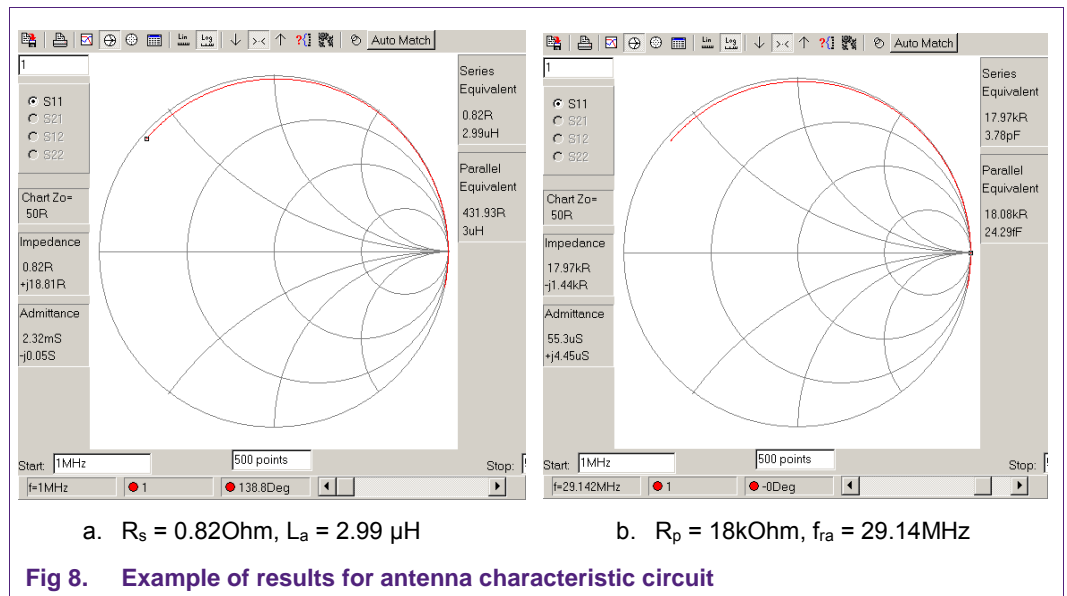
R_p Equivalent resistance at the self-resonance frequency

f_{ra} Self-resonance frequency of the antenna

First the antenna capacitance C_a can be calculated with:

$$C_a = \frac{1}{(2 \cdot \pi \cdot f_{ra})^2 L_a}$$

Fig 8 illustrates the antenna characteristic circuit determination based on the Smith chart:



The series equivalent resistance R_a of the antenna at the operating frequency $f_{op} = 13.56\text{MHz}$ can be calculated out of the characteristic circuit.

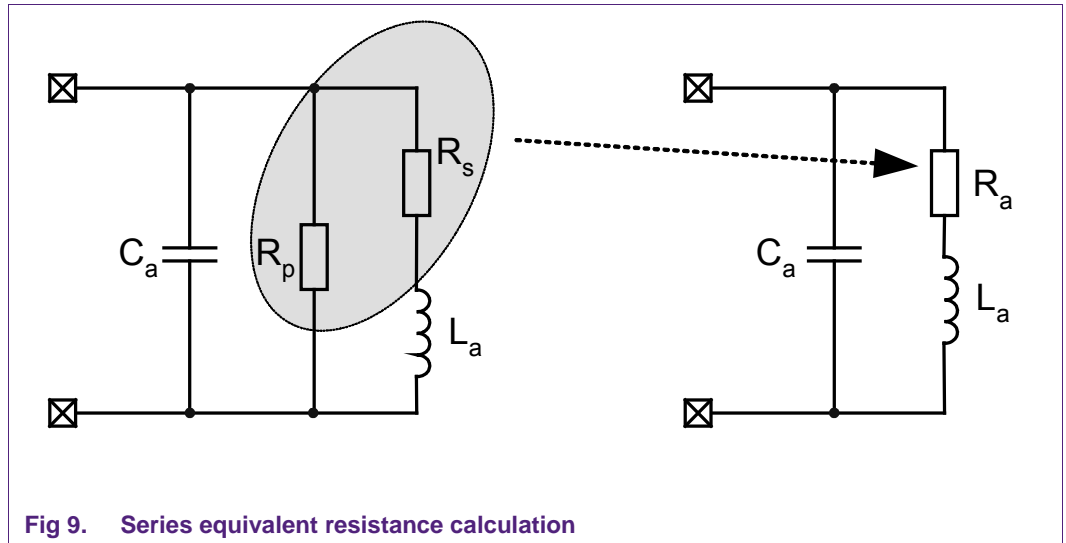


Fig 9. Series equivalent resistance calculation

$$R_p(13.56\text{MHz}) = \frac{R_p(fra)}{\sqrt{\frac{13.56}{fra}}}$$

$$R_a = R_s + \frac{(2 \cdot \pi \cdot f_{op} \cdot L_a)^2}{R_p(13.56\text{MHz})}$$

The parallel resistance $R_p(fra)$ obtained by measurements has to be calculated to the parallel equivalent value at 13.56MHz. This is accomplished in first equation.

R_a in second equation is then calculated by using $R_p(13.56\text{MHz})$.

Please note that this equivalent resistor value is then only valid at 13.56MHz.

3.2.3 Optional Quality factor adjustment

The Q factor of the antenna depends on its inductance value and serie impedance (see equation below). It measures the selectivity of the antenna. If the Q factor is too high the antenna can be too selective which can result in too narrow bandwidth of the resonance and can also impact the shaping of the NFC signal. This is why we recommend the Q factor of the antenna not to exceed 35.

In case the measured antenna quality factor is above this value, R_Q resistors in series can be used to damp it.

The following calculation method can then be used to determine the damping resistor value.

The quality factor of the antenna is calculated with

$$Q_a = \frac{\omega \cdot L_a}{R_a}$$

The value of R_Q needed to reach 35 (resistors in series at each side of the antenna) is calculated by

$$R_Q = 0.5 \cdot \left(\frac{\omega \cdot L_a}{35} - R_a \right)$$

Practical consideration:

In an embedded environment where ferrite shielding is required, a quality factor above 35 is very unlikely. In this case, when Q is lower than 35, damping resistor can be skipped.

A correct range for the Q-factor is 20-35.

3.2.4 Determination of the parallel equivalent circuit:

The parallel equivalent circuit of the **antenna together with the optionally added external damping resistors R_Q** has to be calculated as explained below:

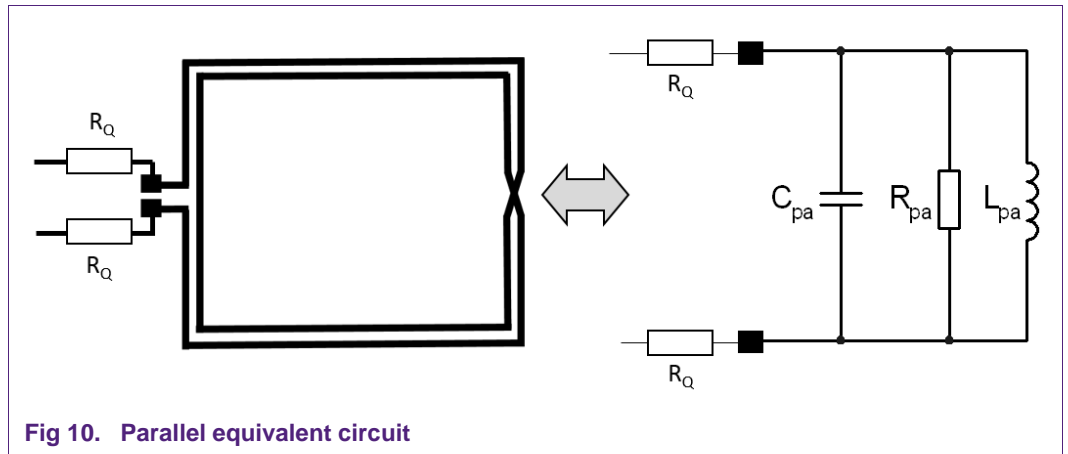


Fig 10. Parallel equivalent circuit

The following formula applies

$$L_{pa} \hat{=} L_a$$

$$C_{pa} \hat{=} C_a$$

$$R_{pa} \hat{=} \frac{(\omega \cdot L_a)^2}{R_a + 2 \cdot R_Q}$$

3.3 Step 2: EMC filter design (L₀ and C₀ definition)

The EMC filter circuit for the PN7120 fulfills two functions: the filtering of the signal and impedance transformation block.

The main properties of the impedance transformation are:

- Decreasing rise time after a modulation phase (poll mode)
- Increasing the receiving bandwidth

L₀ and C₀ value definition:

$$L_0 = 270\text{nH} - 1\mu\text{H}$$

Filter resonance frequency f_{r0} = 15.5MHz ...17MHz, => C₀

$$C_0 = \frac{1}{(2 \cdot \pi \cdot f_{r0})^2 L_0}$$

The EMC filter resonance frequency f_{r0} has to be higher than the upper sideband frequency determined by the highest data rate (848 kHz sub carrier) in the system.

Example:

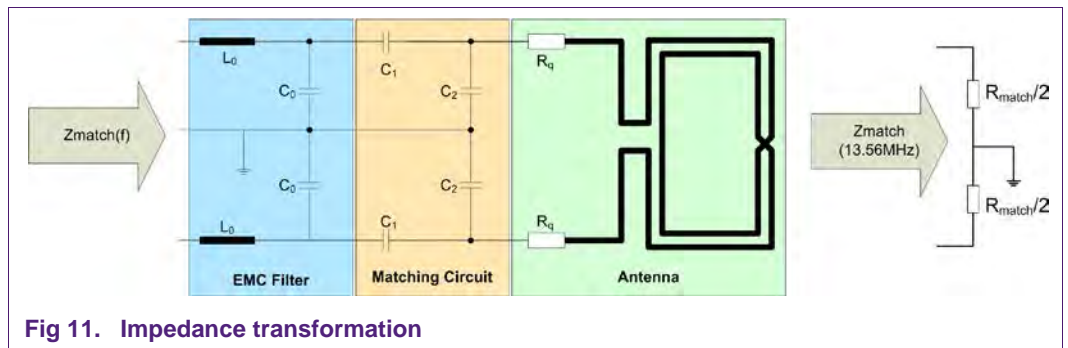
A recommended value of 560nH for L₀ is chosen to calculate the capacitance C₀.

$$L_0 = 560\text{nH}$$

$$f_{r0} = 15.5\text{MHz}$$

$$C_0 = 188.3\text{pF} \rightarrow \text{chosen: } 180\text{pF}$$

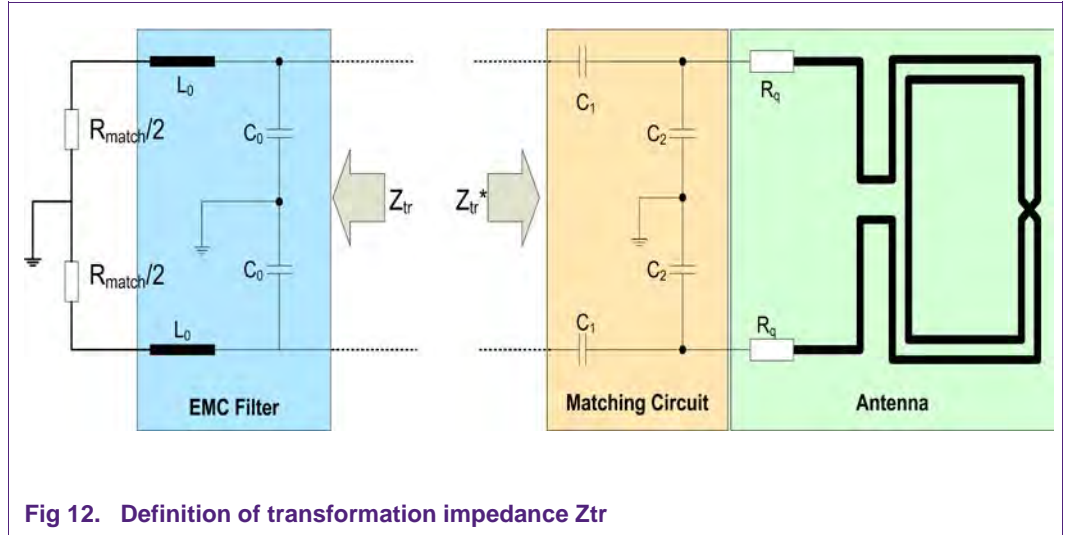
The EMC filter and the matching network must transform the antenna impedance Z_{match}(f) to the required TX matching resistance R_{match} at the operating frequency of f =13.56 MHz.



The measured Z_{match}(f) can be modeled in an equivalent circuit loading each TX pin with R_{match}/2 at 13.56MHz.

By cutting the circuitry after the EMC filter and by using the precondition $R_{match}/2$, the remaining components C_1 and C_2 can be calculated.

Please note that $R_{match}/2$ does not correspond to the driver output impedance



$$Z_{tr} = R_{tr} + jX_{tr}$$

$$Z_{tr}^* = R_{tr} - jX_{tr}$$

$$R_{tr} = \frac{R_{match}}{\left(1 - \omega^2 \cdot L_0 \cdot C_0\right)^2 + \left(\omega \cdot \frac{R_{match}}{2} \cdot C_0\right)^2}$$

$$X_{tr} = 2 \cdot \omega \cdot \frac{L_0 \cdot \left(1 - \omega^2 \cdot L_0 \cdot C_0\right) - \frac{R_{match}^2}{4} \cdot C_0}{\left(1 - \omega^2 \cdot L_0 \cdot C_0\right)^2 + \left(\omega \cdot \frac{R_{match}}{2} \cdot C_0\right)^2}$$

3.4 Step 3: Reader mode matching (C₁ and C₂ definition)

The capacitors C₁ and C₂ are used in combination with the EMC filter to match the antenna to 13.56MHz and at the impedance value R_{match}.

Typical Smith card (S11 measured between TX1/TX2 pins) is shown on Fig 13 (usually called “capacitive matching”).

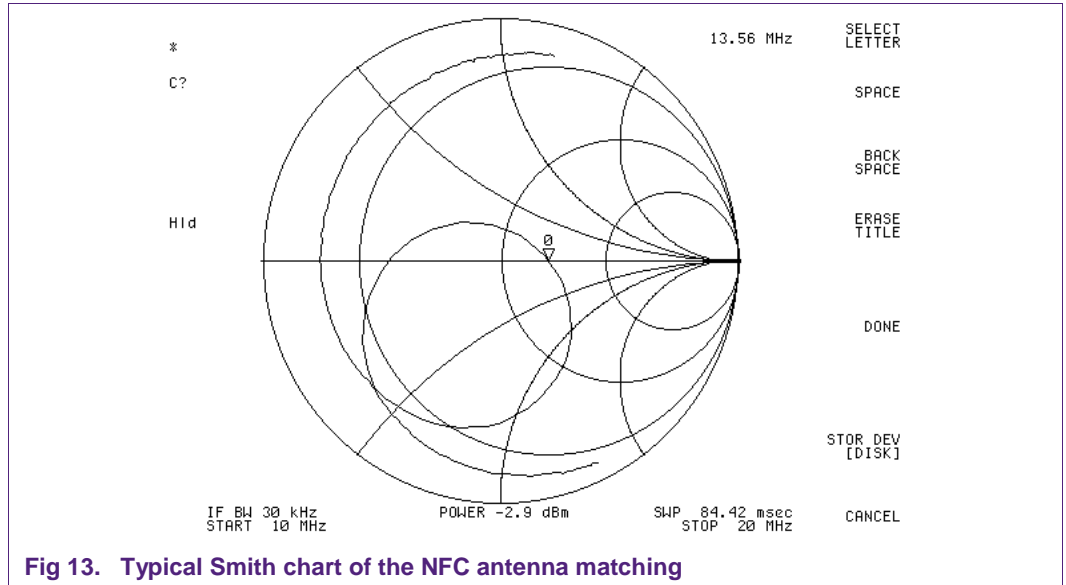


Fig 13. Typical Smith chart of the NFC antenna matching

For the PN7120 the recommendations are given in Table 1.

Table 1. EMC Filter (typical values) and matching impedance target

Component	Value	Remarks
L ₀	560nH	Can be adjusted according to antenna characteristics
C ₀	180pF	Can be adjusted according to antenna characteristics
Z _{match}	70Ω	Impedance target READER mode adjusted with C1 and C2

The reason for the higher cut-off frequency of the EMC filter is a higher stability with close coupling devices in poll mode: less impact of detuning effect on power consumption increase.

The following formulas are then used to calculate the series (C₁) and parallel (C₂) matching capacitances:

$$C_1 \approx \frac{1}{\omega \cdot \left(\sqrt{\frac{R_{tr} \cdot R_{pa}}{4} + \frac{X_{tr}}{2}} \right)}$$

$$C_2 \approx \frac{1}{\omega^2 \cdot \frac{L_{pa}}{2}} - \frac{1}{\omega \cdot \sqrt{\frac{R_{tr} \cdot R_{pa}}{4}}} - 2 \cdot C_{pa}$$

Where L_{pa} , C_{pa} and R_{pa} come from the measured antenna parallel electrical equivalent (see step 1) and R_{tr} and X_{tr} are coming from the EMC filter components value definition (see step 2).

The matching circuit elements C_1 and C_2 must be chosen to get the required match resistance R_{match} (typically 70Ω in READER mode) at 13.56MHz at the PN7120 TX pins.

3.5 Step 4: Card mode tuning (C_2/C_{ANT} ratio definition)

In the PN7120 implementation the TX configurations for the READER mode and for the CARD mode are slightly different. In the previous step the capacitor C_2 was correct set to achieve the 13.56MHz resonance frequency for reader mode, let's call this value $C_{2\text{ reader mode}}$. On Card mode our target is a higher frequency such as 16 MHz resonance frequency. To achieve this value the capacitor $C_{2\text{ card mode}}$ will have a lower value compared to $C_{2\text{ reader mode}}$ from the previous step.

The difference between $C_{2\text{ reader mode}} - C_{2\text{ card mode}} = C_{\text{shift}} = C_{ANT}/2$

But, if we need 2 different values of C_2 to work on reader mode and card mode, which value should we chose? Basically, both! In READER mode C_{ANT} capacitors (see Fig 15) are shorted internally (with a 10Ω resistive switch) while in CARD mode the C_{ANT} are not shorted. The C_{ANT} capacitors when shorted come in parallel to C_2 capacitors and then contribute to the impedance matching in READER mode.

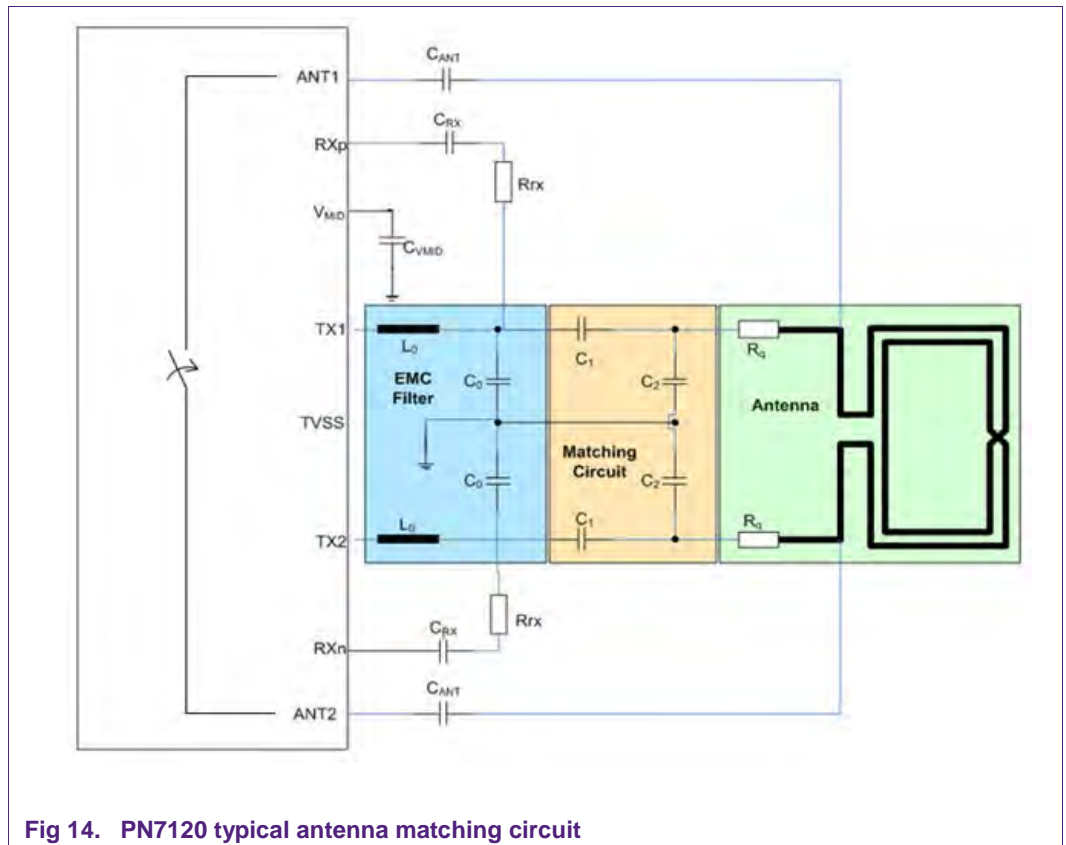


Fig 14. PN7120 typical antenna matching circuit

The way to reach the correct $C_{2\text{ card mode}}$ is given in the next paragraph.

The resonance formula (f_{res} , C_{res} below) are used to calculate the capacitor value to reach the 13.56MHz resonance frequency in Reader mode and the targeted frequency range (16MHz) in CARD mode. The inductance of the antenna has already been measured in step 1.

$$f_{res} = \frac{1}{2 \cdot \pi \sqrt{L \cdot C}} \quad C_{fres} = \frac{1}{(2 \cdot \pi \cdot f_{res})^2 L}$$

Based on this parameter and on the targeted listen mode frequency, the ratio between $C_{2 \text{ reader mode}}$ and C_{ANT} can be defined.

Example:

Let's take an antenna with inductance value $L=3.09\mu H$ and a chosen CARD mode frequency at 16MHz:

$$C_{13.56MHz} = 44.5pF \text{ (reader mode)}$$

$$C_{16MHz} = 32pF \text{ (card mode)}$$

$$C_{13.56MHz} - C_{16MHz} = 12.5pF$$

$$C_{shift} = 12.5pF$$

This means that the total parallel capacitance for the READER mode needs to be 12.5pF higher than in CARD mode.

With this information and with the C_2 ($C_{2 \text{ reader mode}}$) value calculated during step 3, C_2 and C_{ANT} can be calculated.

$$C_{2 \text{ reader mode}} = C_{2 \text{ card mode}} + C_{ANT}$$

$C_{ANT} = 2 \cdot C_{shift}$, because two C_{2ANT} capacitors in series are used in the matching network.

$$C_{shift} = 12.5pF$$

$$C_{ANT} = 25pF \rightarrow 27pF \text{ normalized value}$$

$$C_{2 \text{ card mode}} = C_{2 \text{ reader mode}} - C_{ANT} = 47pF - 27pF = 20pF$$

Once C_2/C_{ANT} split is defined it must be implemented on a real device and some fine tuning must be done with network analyzer.

Based on the value calculated, the matching impedance $Z_{match} = R_{match} + jX_{match}$ must be measured with an impedance or network analyzer. The TX1 and TX2 pins of the PN7120 are the probing points for the network/impedance analyzer to measure Z_{match} .

3.6 Step 5: Rx path tuning (R_{rx} & C_{rx} definition)

Two configurations are possible for the Rx path:

- 1- The first one consists in connecting Rx path on the EMC filter
- 2- The second one consists in connecting Rx path on the antenna.

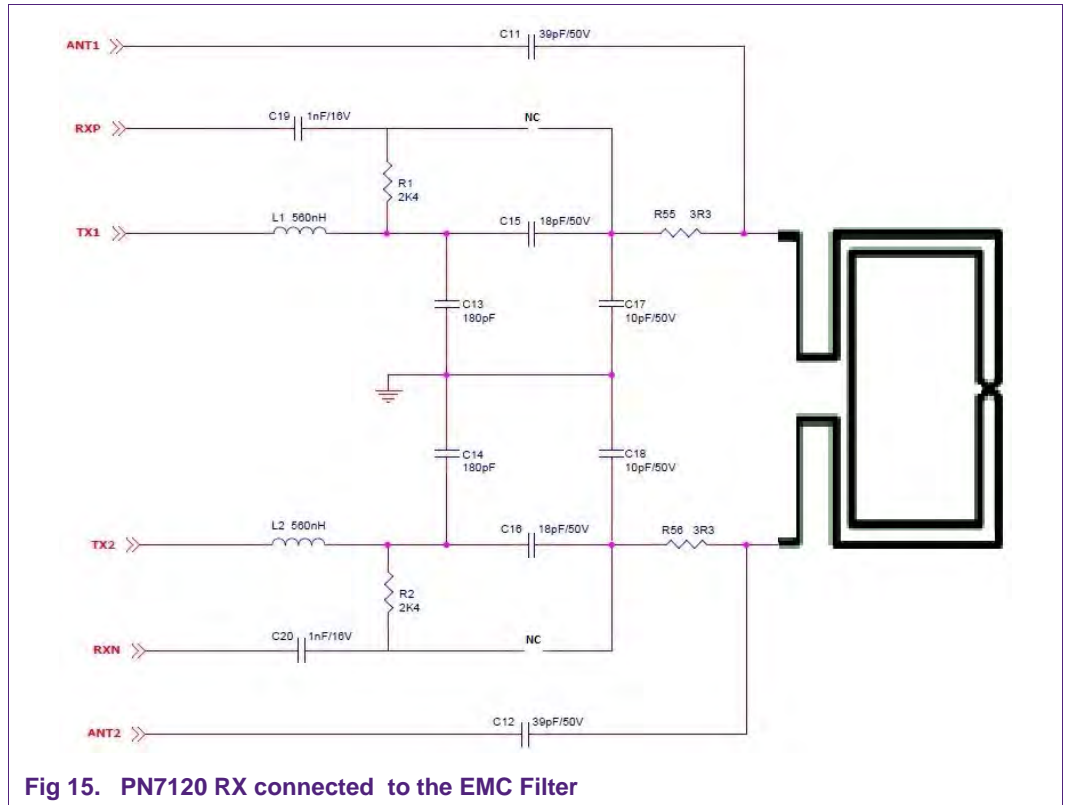


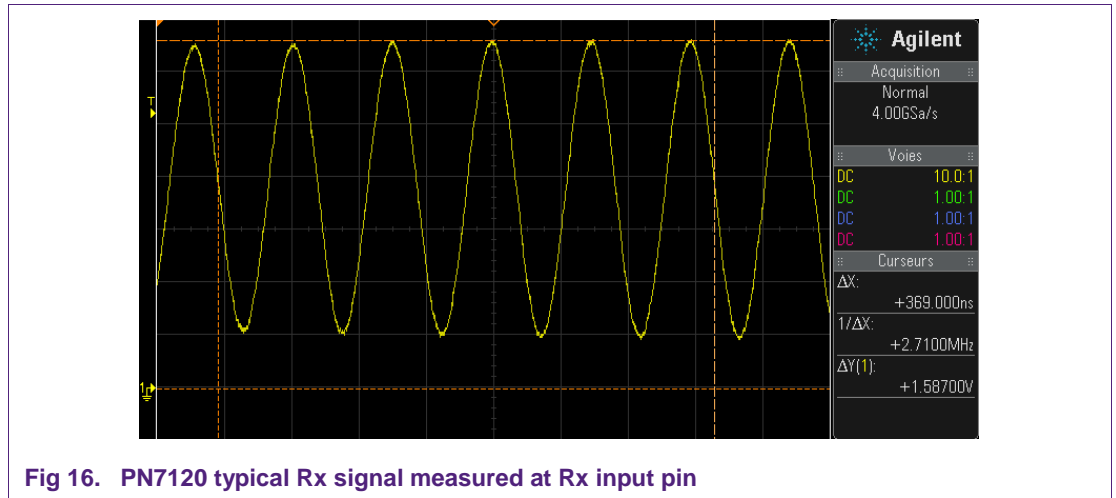
Fig 15. PN7120 RX connected to the EMC Filter

The purpose of the C_{rx} capacitors is to provide an AC coupling of the Rx signal. A value of 1nF can generally be used.

The purpose of the R_{rx} resistor is to provide a voltage drop so that the Rx input is not saturated.

The first step of the Rx path tuning process is to define which Rx path connection is the best. For small antenna or antenna setup in a stringent environment (e.g. metal surrounding, bad isolating ferrite ...) a direct connection to antenna is preferred. For large antenna or optimized setup (e.g. antenna in back cover) the connection can be preferably done on the EMC filter.

Once the RX connection point has been chosen according to the setup, R_{rx} value must be carefully adjusted. The resistor value on the Rx path must be chosen to guarantee that the peak voltage at Rxn and Rxp stays below 1.65Vpk. As illustrated below the 13.56MHz can be observed on top of a DC offset of 900mV.



Note: The peak value depends on the AGC Vref [Bit (1:0)] setting forced by the register CLIF_ANA_AGC_REG. This value was defined to reach the best performances of the Rx sensitivity. Changing the default value is not recommended.

Table 2. CLIF_ANA_AGC_REG and expected maximum Rx voltage

setting	Peak Value
0	1.15Vpk
1	1.45Vpk
2	1.55Vpk
3	1.65Vpk

4. Matching verification

The antenna has first to be matched to the PN7120 as described in the previous chapter §3 PN7120 Antenna matching.

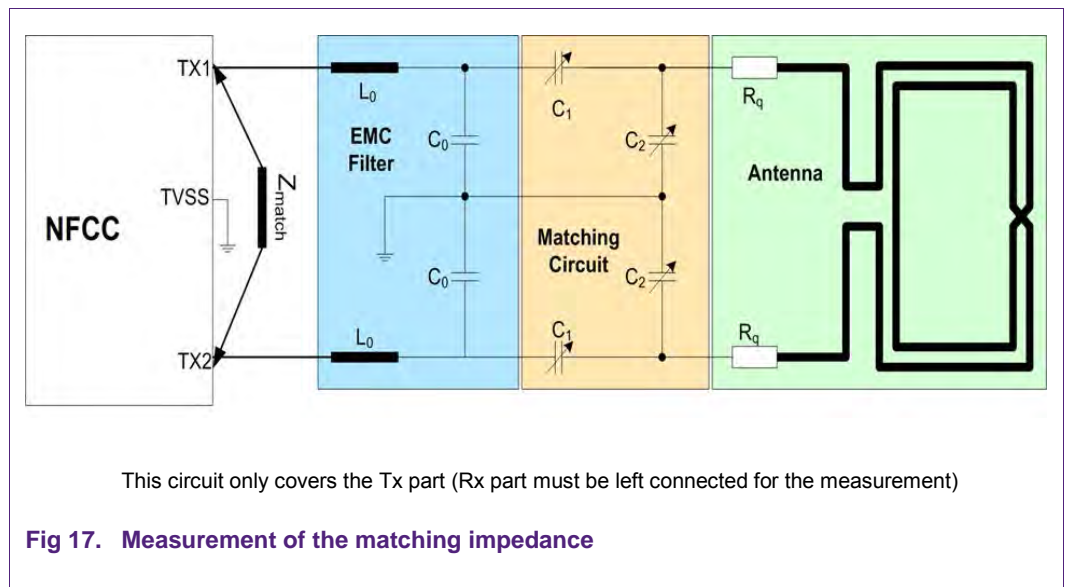
Then the steps described below can be followed to verify the antenna matching.

Due to the fact that the PN7120 IC must NOT be powered ON during this verification, the IC pins are not configured properly. Therefore a 10 ohms resistor must be connected between ANT 1 and ANT2 pin when checking the antenna matching for the READER mode.

4.1 Step 1: verification of the Reader/Poller mode matching.

The load impedance is measured with a network analyzer by contacting a test fixture across the TX1 and TX2 pins of the PN7120.

Both matching and measurement of the NFC antenna have to be performed at the final mounting position to consider all parasitic effects like metal which influences the quality factor, the inductance and parasitic capacitance.



In order to simulate the Reader/Writer behavior of the PN7120, the CANT capacitors need to be shortcut with a 10 Ohm resistor. By shortening both C_{ANT} with a 10Ohm resistance, they came in parallel to C_2 capacitors which causes a frequency down shift.

Connecting a 10 ohms resistor across PN7120 ANT1 and ANT2 pins is mandatory before performing this measurement.

An asymmetric impedance curve shall be seen on the network analyzer:

- Reader/Writer mode → $R_{match} = 70\Omega$ at 13.56MHz

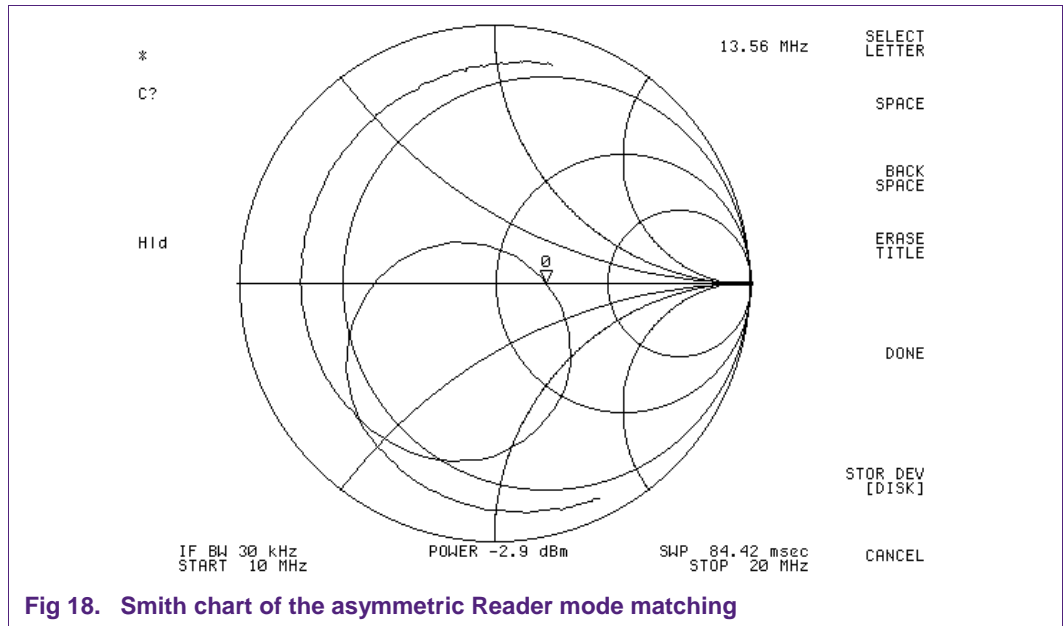


Fig 18. Smith chart of the asymmetric Reader mode matching

If the measurement is not the matching expected by the theoretical matching some adjustments can be necessary.

Practical considerations:
 The value of C1 changes the magnitude of the matching impedance. After changing C1 the imaginary part of Z_{match} must be compensated by adjusting C2 as well.
 C2 changes mainly the imaginary part of Z_{match} .

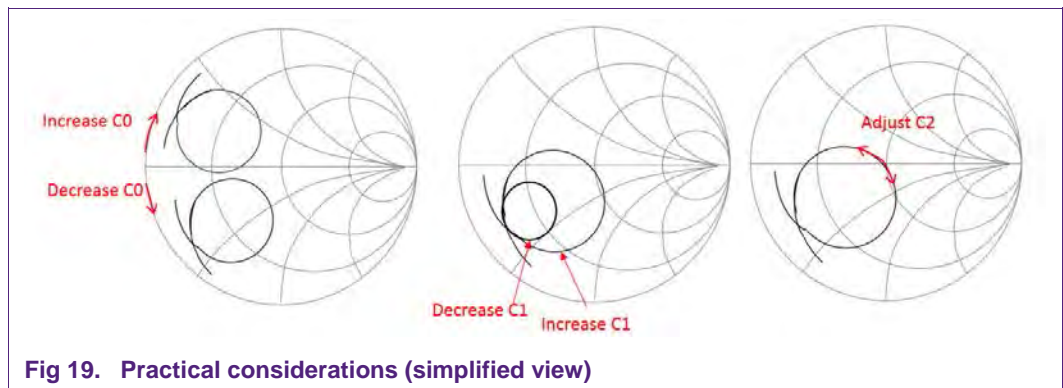


Fig 19. Practical considerations (simplified view)

Remark: Do not forget to remove the 10 ohms resistor after this measurement.

4.2 Step 2: verification of the CARD/listen mode frequency

Similarly to the READER mode verification, measure the load impedance by connecting the probe tips of the network analyzer on the Tx output pins of the IC.

Remark: Do not forget to remove the 10 ohms resistor for this measurement.

The matched frequency should be in the following range:

Card mode frequency → 14.5 – 16 MHz

If it is not, the balance between CANT and C2 capacitors must be fine-tuned as described in the previous paragraphs.

4.3 Components characteristics

Table 3. Components characteristics

Component	Maximum tolerance	Maximum rating
L ₀	5%	100mA at least at 13.56MHz
C ₀	5%	16V at least
C ₁	2%	50V or 25V(*)
C _{2a}	2%	50V or 25V(*)
C _{2b}	2%	50V or 25V(*)
R _q	5%	N/A
R ₁	5%	N/A
C _{RX}	5%	50V or 25V(*)
C _{VMID}	10%	4V at least

(*) the choice of the voltage 50V or 25V is depending on the antenna characteristics and the operating conditions: the voltage at antenna terminals should be measured in the worst case conditions.

5. Performance verification and fine tuning

This section will show you on how to verify the performance of your device after the matching done. This verification gives only an overview of the performance of the system once a register tuning is also request to achieve the optimal performance.

There is two possibilities to check the performance of your antenna. The first method is to compare the interoperability with other devices. For example on card mode you can measure the communication distance with a reader from the market, on reader mode you can check the communication distance with well-known cards.

A second option is to check the performance of your device against a contactless standard. Currently 3 standards are the most common in the contactless world. There is not a rule to know which standard you must follow, but for payments purpose the EMV Co standard will be most commonly used. To check the interoperability with mobiles the NFC Forum can be a good option. For other kinds of applications the “ISO” specification is the most common used.

5.1 Main specifications

5.1.1 ISO/IEC 14443 specifics

The ISO/IEC 14443 (called “ISO” in the following, details see [ISO/IEC14443 \[2\]](#)) specifies the contactless interface as widely being used with contactless smartcards like e.g. MIFARE cards.

The ISO/IEC 14443 defines the communication between a reader (“proximity coupling device” = PCD) and a contactless smartcard (“proximity chip card” = PICC). In four parts it describes the physical characteristics (i.e. the size of the PICC antennas), the analog parameters like e.g. modulation and coding schemes, the card activation sequences (“Anticollision”) and the digital protocol.

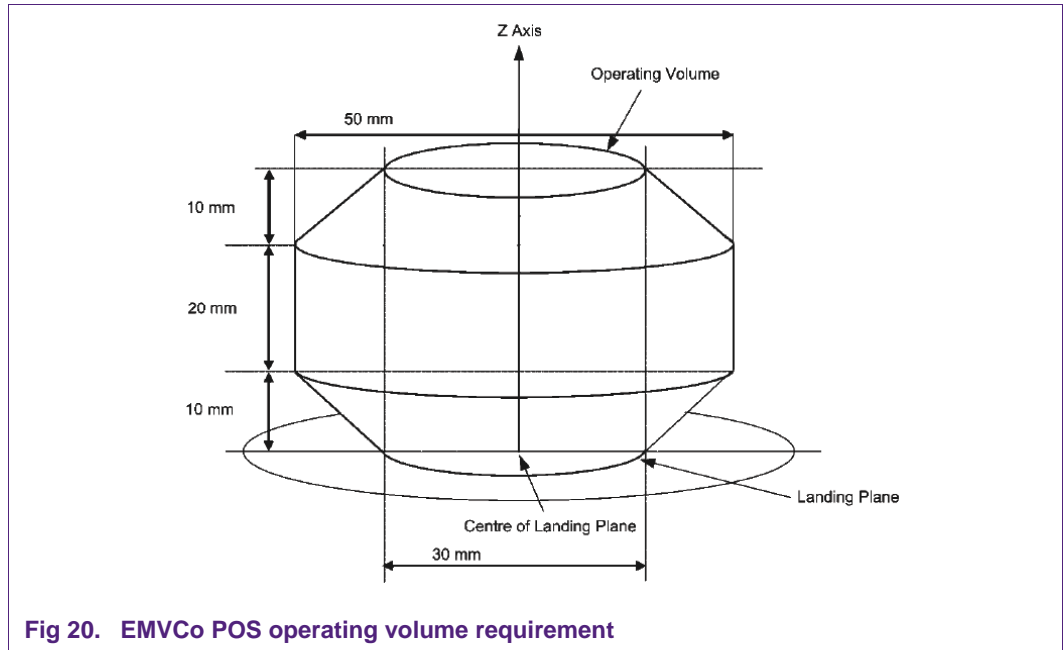
The ISO/IEC 10373-6 [1] describes the test setup and all the related tests for cards and the reader to test the ISO14443 requirements.

This specification covers only Type A and Type B communications.

5.1.2 EMVCo specifics

[EMVCo standard \[3\]](#) it is the most used standard used for contactless payments purpose. It specifies a contactless interface for point of sales (POS) terminals (= PCD) and the corresponding contactless payment cards or mobiles (= PICC). This interface is very similar to the one defined ISO/IEC 14443, but it uses its own set of requirements and specification details. The EMVCo test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6 [1].

One main difference for the tests is the definition of an operating volume, as shown in *Fig 20*.

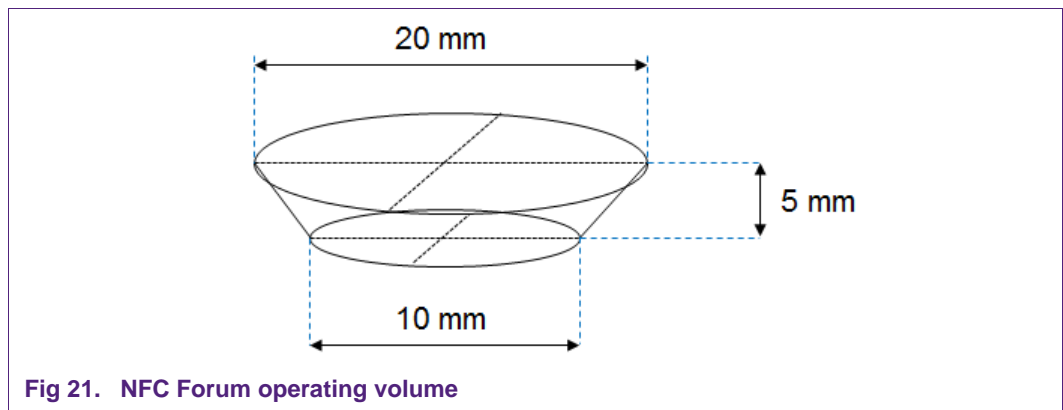


Within this volume the given parameters need to be fulfilled.
This specification covers only Type A and Type B communications.

5.1.3 NFC Forum specifics

The NFC Forum is a standard created to promote the use of NFC technology in consumer electronics, mobile devices, PCs, and more.

The standard NFC Forum device needs to fulfill the reader mode (Poller), and card mode (listener). One of the differences between this standard and the others is the use of 3 different protocols during test, the NFC-A, NFC-B and NFC-F and 6 different antennas for testing (3 for Poller tests and 3 for listener tests). Once again the NFC Forum test equipment and way of testing is quite different from the test specification as defined in ISO/IEC 10373-6 and EMV Co. Additionally the NFC Forum specifies an operating volume as shown in Fig 21.



5.2 Performance check against standards

During this section we will show the basics measurements that can be done to check the performance of your device.

We will show the measurements for reader mode and card mode using an EMV Co test bench. For every measurement we will give you the equivalent measurement on other standards.

5.2.1 Reader Mode measurements

The reader mode measurements will be divided in two parts: The transmission part and the reception part.

For the transmission this part the most relevant tests will be:

1. Field strength measurement
2. Waveform measurement

We will show how to perform this measurements using an EMV Test PICC, "ISO" Reference PICC and the NFC Forum Reference Listeners. These hardware can be bought from one of the accredited laboratories.

For the reception part, some specific test are described on these specifications. However we will not cover these tests on this document. To the test the reception part we will perform some functional tests.

5.2.1.1 Field strength measurement

When the PN7120 is configured in READER mode, the strength of the emitted RF field can be measured by using a Reference PICC that is placed at a short distance from the PN7120 antenna. The reference PICC is calibrated on the relevant test bench: its output voltage corresponds to well-defined field strength.

The output voltage of the Reference PICC can be measured with an oscilloscope or directly measured with a voltmeter if the PN7120 is configured to emit a continuous RF field.

Based on the targeted standard compliance, the Reference PICC to be used can be different.

a. EMVCo example

The *EMVCo standard [3]* for payment applications defines a specific Reference PICC and a large operating volume is required: up to 4cm distance.

This operating volume specified can usually not be met by an embedded equipment application.

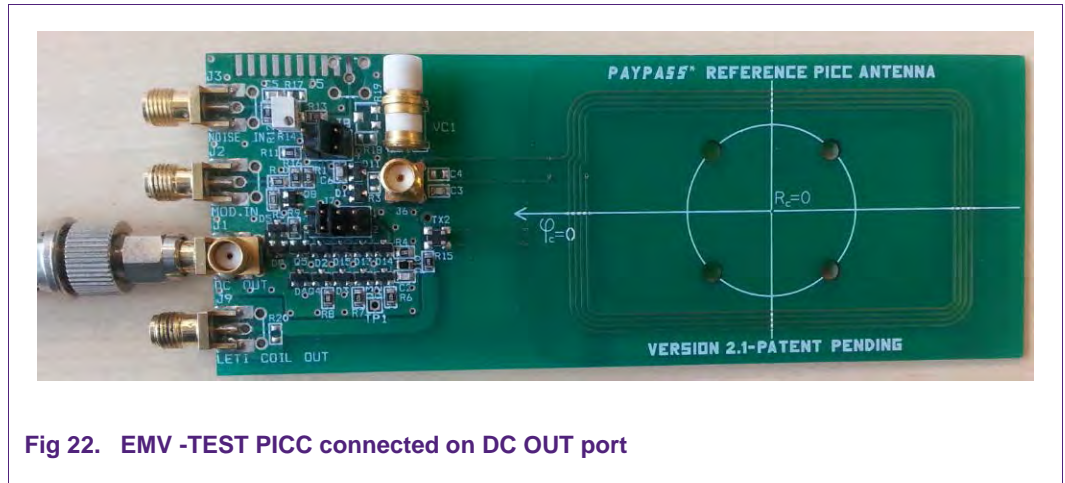


Fig 22. EMV -TEST PICC connected on DC OUT port

Steps:

- 1) Connect the output J1 to an oscilloscope (1Mohms)
- 2) Set the jumper J8 in position 1-4, jumper on the “antenna side”
- 3) Place the EMV - Test PICC in one position of the operating volume
- 4) Set your device to send continuous RF carrier.
- 5) Measure the mean value using an oscilloscope.
- 6) Check the min and max values against EMV Co specification.

b. ISO example

The Reference PICC to be used to check compliance with the [ISO/IEC14443 \[2\]](#) standard is described in the [ISO/IEC10373-6 \[1\]](#) standard.

Here is the specification of the field strength required by the [ISO/IEC14443 \[2\]](#) standard:

- No operating volume (i.e. area providing a field strength greater than 1.5A/m) is required
- a minimum field strength of 1.5A/m must be achieved
- the maximum field strength must not exceed 7,5A/m

This requirement is usually met at short distance (<2cm) in case of an embedded equipment application.

This test was divided in two different tests H max and H min.

For Hmax test:

- 1) Tune the ISO Reference PICC to 19 MHz
- 2) Adjust the R2 load to obtain 3V measured on the connector CON3 when the TEST PCD assembly produce the H max

- 3) Place the ISO Reference PICC in a test position on the device under test
- 4) Set your device to send continuous RF carrier.
- 5) Measure the DC output of the DC output CON3
- 6) The DC voltage at CON3 shall not exceed 3V

For Hmin test:

- 1) Tune the ISO Reference PICC to 13.56 MHz
- 2) Adjust the R2 load to obtain “Vload” (6V for class 1 ref PICC) measured on the connector CON3 when the TEST PCD assembly produce the H min
- 3) Place the ISO Reference PICC in a test position on the device under test
- 4) Set your device to send continuous RF carrier.
- 5) Measure the DC output of the DC output CON3
- 6) The DC voltage at CON3 shall exceed “Vload”

Some ReferencePICCs, which are commercially available (see Fig 23), are pre-calibrated and equipped with several jumper options to address the most relevant tests with a single ReferencePICC.

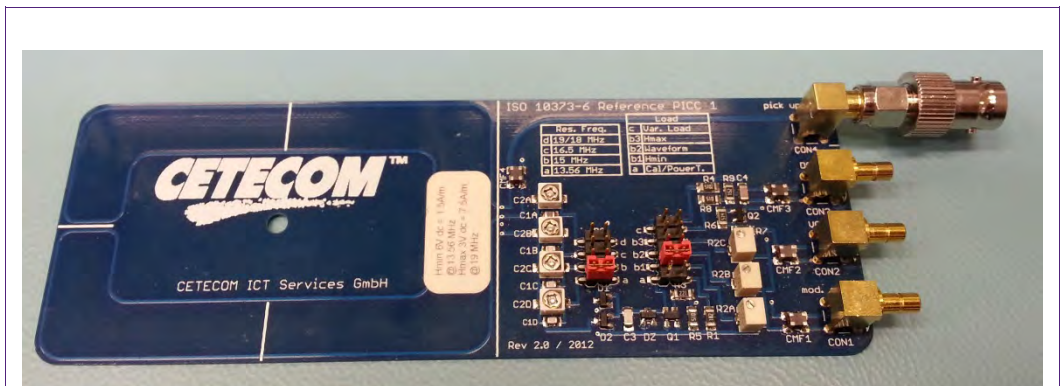


Fig 23. ISO/IEC 10373-6 Reference PICC Class 1

Still for each PICC Class a separated Reference PICC is required.

For example purpose the measurement was show using a Reference PICC Class 1, however PCD must support classes 1, 2, and 3.

The support of the classes 4, 5, and 6 is optional.

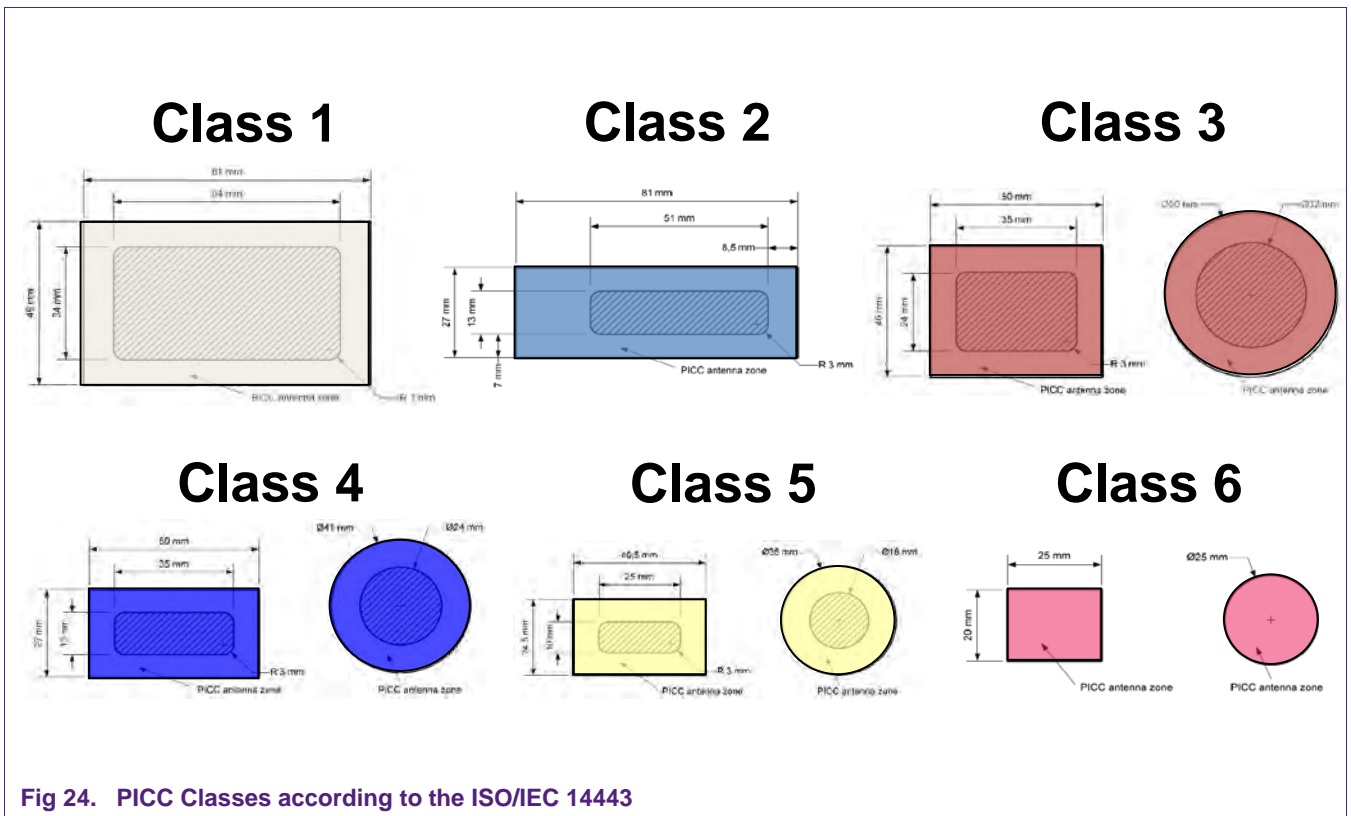


Fig 24. PICC Classes according to the ISO/IEC 14443

c. NFC Forum example

The *NFC Forum standard [4]* defines 3 different Reference PICCs so-called reference listeners: reference Listener 1, reference Listener 3 and reference Listener 6.

The required operating volume is much smaller than EMVCo: the distance is up to 0.5cm only. A test center can be defined for each Listener if the distance between the 3 tests centers can be inside a circle of 20 mm diameter.

The power emission test is divided in two different tests, one for minimum requirements and a second for maximum requirements.

For Minimum Power Emission Measurement:

- 1) Set the load of the reference Listener to 820 ohms
- 2) Place the Reference Listener in a test position on the device under test
- 3) Set your device to send continuous RF carrier.
- 4) Measure the DC output on the connector J1
- 5) Repeat this measurement for all test positions and all reference listeners
- 6) The DC voltage must be inside minimum and maximum limits

For Maximum Power Emission Measurement:

- 1) Set the load of the reference Listener to 82 ohms
- 2) Place the Reference Listener in a test position on the device under test
- 3) Set your device to send continuous RF carrier.
- 4) Measure the DC output on the connector J1
- 5) Repeat this measurement for all test positions and all reference listeners
- 6) The DC voltage must be inside minimum and maximum limits

5.2.1.2 NFC Signal shaping verification

The following verifications provide a quick way to check the shaping of the generated RF signal when the PN7120 is configured in READER mode.

An oscilloscope with a bandwidth of at least 100MHz has to be used to carry out the shaping measurements (see Fig 25).

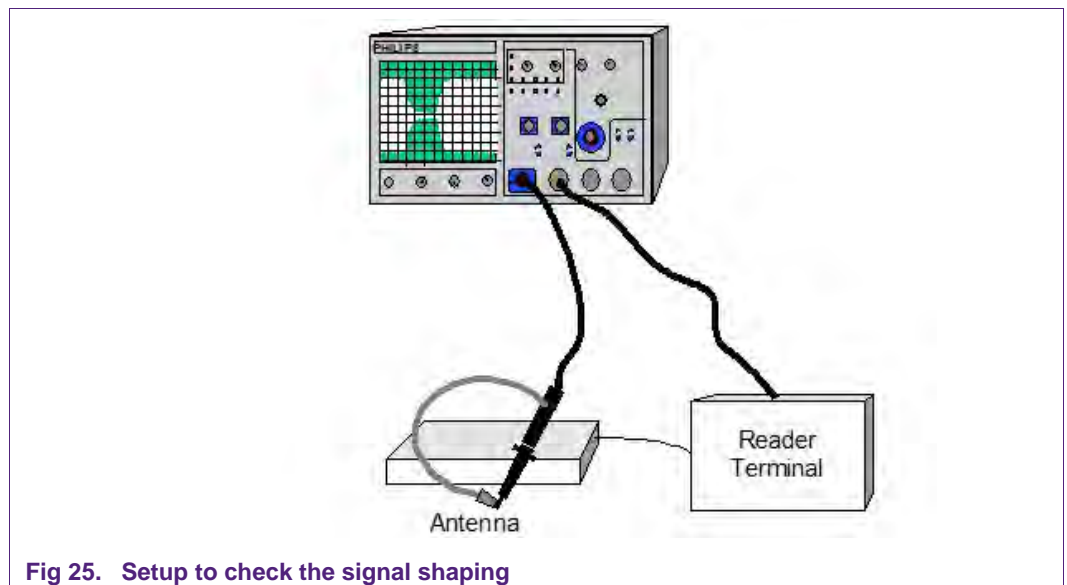


Fig 25. Setup to check the signal shaping

CH1: Use a loop with the ground line shortcut at the probe to enable inductive signal coupling. Hold the probe loop on top of the antenna. When the shaping compliance to a given standard is verified, the corresponding reference PICC must be connected to CH1.

Optional: CH2 used as trigger if possible

The absolute measured voltage in CH1 depends on the coupling (= distance) between the probe loop and the reader antenna.

The influence of the coupling on the shape can be neglected.

Once this quick verification has been done, the proper pick up coil must be used to check the compliancy to the different standards.

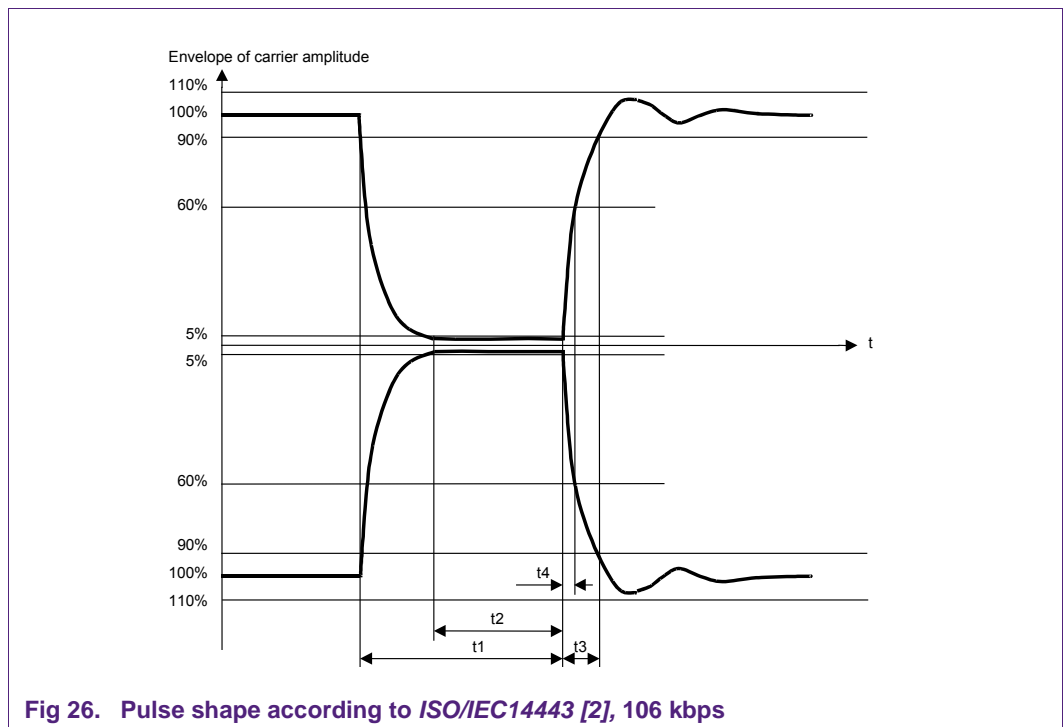
a. Waveform measurement using an “ISO” reference PICC

We will show here how to measure the waveform of your device using an “ISO” reference PICC. This procedure is not the official procedure, once some analysis tools described on this specification will not be used. However this procedure it is a good overview of the waveform measurement defined on “ISO”.

Procedure:

- 1) Tune the ISO Reference PICC to 16.5 MHz
- 2) Place the ISO Reference PICC in a test position on the device under test
- 3) Adjust the R2 load to obtain “Vload” (6V for class 1 ref PICC) measured on the connector CON3
- 4) Set your device to send a Type A or Type B command.
- 5) Using an oscilloscope trigger your acquisition to correct acquire a Type A or Type B pause.
- 6) Using the cursors of the oscilloscope measure the timings described on the figure below
- 7) The Timings measured must be inside minimum and maximum limits

It is recommended to check the pulse shape with the Reference PICC according to the values given in *Fig 26* and *Table 4*.



The times t1-t2 describe the time span, in which the signal falls from 90% down to below 5% of the signal amplitude.

The rising time of the carrier envelope is t_4 . It must be checked that the carrier envelope at the end of the pause reaches 60% of the continuous wave amplitude within $0.4\mu s$.

Table 4. Pulse shapes definition according to ISO/IEC14443[2], 106 kbps

Parameter	Condition	Min	Max
t_1		$28/f_c$	$40.5/f_c$
t_2	$t_1 > 34/f_c$	$7/f_c$	t_1
t_3	$t_1 \leq 34/f_c$	$1.5 \times t_4$	t_1
t_4		0	$6/f_c$

* f_c = carrier frequency

Please note that the standards can evolved. Final value must be directly retrieved from the latest official publication of the corresponding standard.

The type B modulation index m (see Fig 27) has also to be measured; the criteria are given in Table 5.

It must be noted that the PN7120 integrates an automatic adjustment of the modulation index to keep it constant whatever the antenna environment.

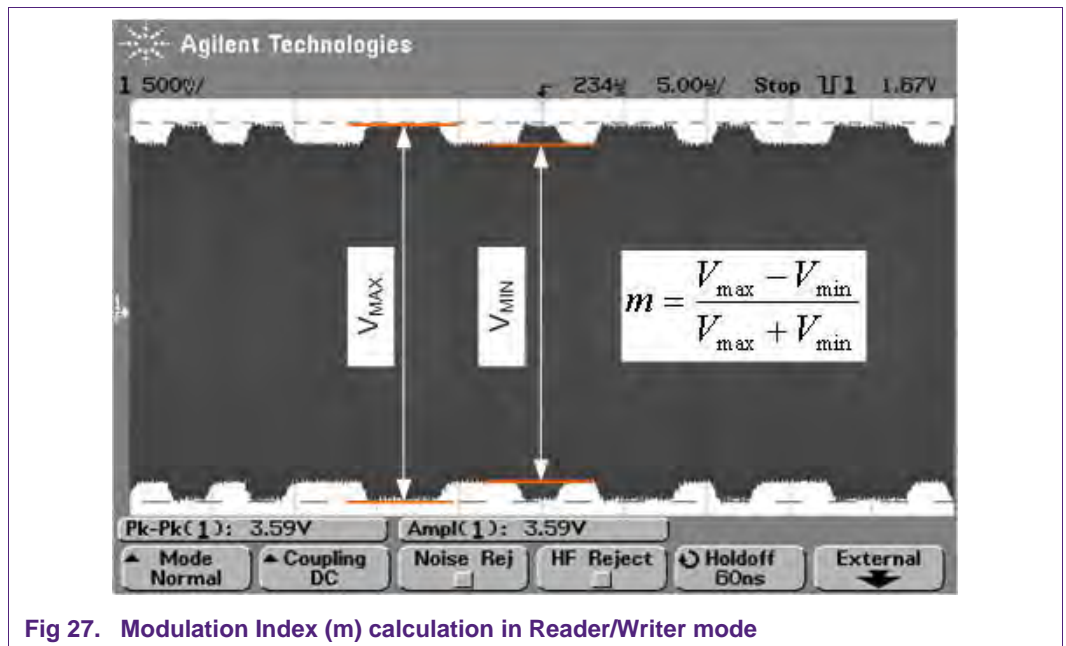


Fig 27. Modulation Index (m) calculation in Reader/Writer mode

Table 5. Type B 106kbps criteria according to ISO/IEC14443

Parameter	Min	Max	Unit
Modulation index	8	14	%
t_f	0	$16/f_c$	
t_r	> 0 and $t_f - 8/f_c$	$< t_f + 8/f_c$ and $16/f_c$	

b. Waveform measurement using an EMV Test PICC

The procedure to check the Waveform on EMV Co specification is very similar to the “ISO”. The procedure below is not exactly the official procedure for the EMV Co testing, but it can give you a good overview of the performance.

- 1) Connect the output J9 to an oscilloscope (50ohms). Additionally EMVCo uses a 20 MHz filter between the oscilloscope and the EMV Test PICC.
- 2) Set the jumper J8 in position 1-2, jumper on the “connector side”.
- 3) Place the EMV - Test PICC in one position of the operating volume (only the center positions will be checked from 0 cm to 4 cm).
- 4) Set your device to send a Type A or Type B command.
- 5) Using an oscilloscope trigger your acquisition to correct acquire a Type A or Type B pause.
- 6) Using the cursors of the oscilloscope measure the timings described in *Fig 27*.
- 7) The Timings measured must be inside minimum and maximum limits

c. Waveform measurement using a NFC Forum reference Listener

The procedure for the NFC Forum is very similar to the two other specifications. However the particularity is the use of different sizes of antennas and loads during the tests. The test procedure should be done using the reference Listener 1, 2 and 3, and the loads 330 ohms and 820 ohms. This procedure is not exactly the official procedure for NFC Forum testing, but it can give you a good overview of the performance.

- 1) Connect the output J4 (sense coil) to an oscilloscope (50ohms).
- 2) Set the jumper for the desired load (330 ohms or 820 ohms)
- 3) Place the reference Listener in one position of the operating volume.
- 4) Set your device to send a NFC A or NFC B or NFC F command.
- 5) Using an oscilloscope trigger your acquisition to correct acquire NFC A or NFC B or NFC F command
- 6) Using the cursors of the oscilloscope measure the timings described in *Fig 27*.
- 7) The Timings measured must be inside minimum and maximum limits

5.2.1.3 Reception check

For simplification purposes we will test the reception of our device on reader mode using some functional checks. Even if the 3 different standards presented until now, have their own tests to check the reception of the reader mode. We suggest to check the reception, checking the communication distance in READER mode with some typical cards:

- MIFARE Ultralight
- MIFARE DESFire
- FeliCa card
- ISO/IEC14443-B card

Additionally using an oscilloscope and a spy coil between the card and the reader it is possible to check if the communication did not occurred because of the reader reception or card reception.

How to check if the problem is from the card or from the reader:

- If you can see the command from the reader but there is no response from the card. This is probably a card reception problem.
- After a response from the card the reader does not send the next expected command. This is probably a reader reception problem.

If you identify one of this situations, the RX path must be measured on the FAIL situation. If the signal is correct, the problem can come from other layers, digital and so on. Additionally you can use a RF spy from a test tool provider, to be able to check this point.

5.2.2 Card mode measurements

The card mode measurements will be divided in two parts: the transmission and the reception part.

For the transmission part, basically we will check load modulation amplitude for the 3 different standards.

On the reception part, we will check the communication distance with some readers.

5.2.2.1 Load modulation amplitude measurement

When the PN7120 is configured in CARD mode, the data are transmitted by modulating the amplitude of the external RF field. This is done simply by changing the load impedance presented to the antenna; it is called load modulation.

An illustration of the signal observed on an EMVCo test bench is shown in Fig 28.

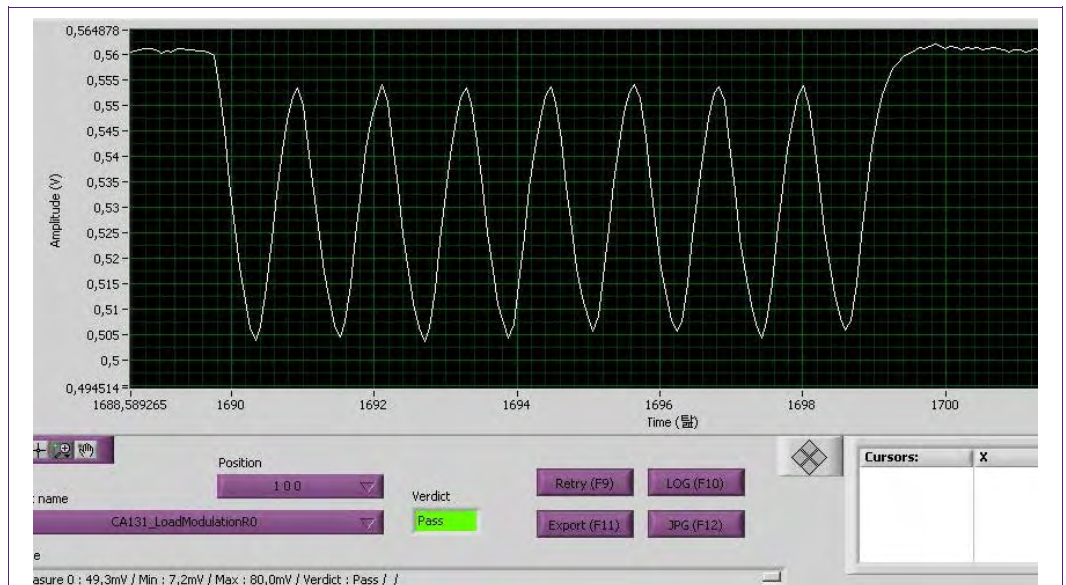


Fig 28. Card Emulation: EMVCo test bench typical measurement

The different standards define the amplitude of the load modulation in listen mode at different distances and positions on the antenna.

The load modulation amplitude or sideband level amplitudes have to be measured by using a specific test bench which is different for each standard (ISO, EMVCo, NFC Forum).

a. How to check the LMA on different test benches using an oscilloscope

If you do not have a certified test bench to test the load modulation, you can use an oscilloscope + the reference antennas for the standard connected to a NFC reader emulator. The procedure will be the following:

- 1) Connect the output of the reference PCD to the oscilloscope.
- 2) Send a request using the requested power level.
- 3) Capture at least 7 cycles of the subcarrier load modulation response
- 4) Using cursors, measure the amplitude peak to peak of the response ("subcarrier")
- 5) The LMA measured must be inside minimum and maximum limits

Table 6. Load modulation HW for LMA test

Parameter	EMV Co	NFC Forum	„ISO“
Antenna	Test PCD	Poller 0,3,6	Test PCD assembly
Output	J2	J2	Bridge*
Input	J1	J1	RF IN

* Bridge corresponds to the output of the load modulation test circuit

5.2.2.2 Reception test

The performance verification of the PN7120 application can be finalized by some functional checks in CARD mode.

We suggest to check the communication distance with some reader, such as:

- Pegoda
- Omnikey 5321
- ACR122

Additionally using an oscilloscope and a spy coil between the card and the reader it is possible to check if the communication did not occurred because of the reader reception or card reception.

How to check if the problem is from the card or the reader:

- If you can see the command from the reader but there is no response from the card. This is probably a card reception problem.
- After a response from the card the reader does not send the next expected command. This is probably a reader reception problem.

If you identify one of this situations, the RX path must be measured on the FAIL situation. If the signal is correct, the problem can come from other layers, digital and so on.

Additionally you can use a RF spy from a test tool provider, to be able to check this point.

5.3 Fine tuning through registers

In addition to the matching methodology, the RF performance can eventually be fine-tuned by the mean of registers which are accessible from the PN7120 host interface.

5.3.1 Register setting command

Please refer to the *PN7120 User Manual* [5] contactless configuration chapter to get more insight on the values and addresses of the registers, especially about the related NCI command TLV structure.

The RF_TRANSITION_CFG parameter which allows to configure the CLIF registers is different from the above structure since there must be transitions to take into account, as soon as a parameter is valid for different modes (e.g. poller mode and listen mode) while its value can be different.

The extension of the TLV structure is given as below:

- The Tag Address is always 0xA0 0D
- The Length can be L=3, 4 or 6
- The Value is actually a secondary data area with a transition ID, the CLIF register offset (equivalent to an address), and the actual value.

Tag (2 Bytes)	Length (1 Byte)	Value (3, 4 or 5 Bytes, depending on the transition ID)		
0xA0 0D	0x03	Transition ID (1 Byte)	CLIF register offset (1 Byte)	1-Byte reg. value
	0x04			2-Byte reg. value
	0x05			4-Byte reg. value

Fig 29. CLIF NCI Structure

Basically, depending on the polling loop events, the transition ID corresponds to a set of transitions applied in the registers.

The transition ID depends on

- IN vs. OUT
 - o In each IN transition a set of CLIF registers is loaded out of the EEPROM
 - o In each OUT transition the settings are reverted
- Initiator vs. Target
- TX vs. RX
- Technology (A, B, F, etc.)
- Baud rate (106kb/s etc.)

A simplified view of the different transition IDs is depicted in Fig 30. It does not include asymmetric data rates for instance.

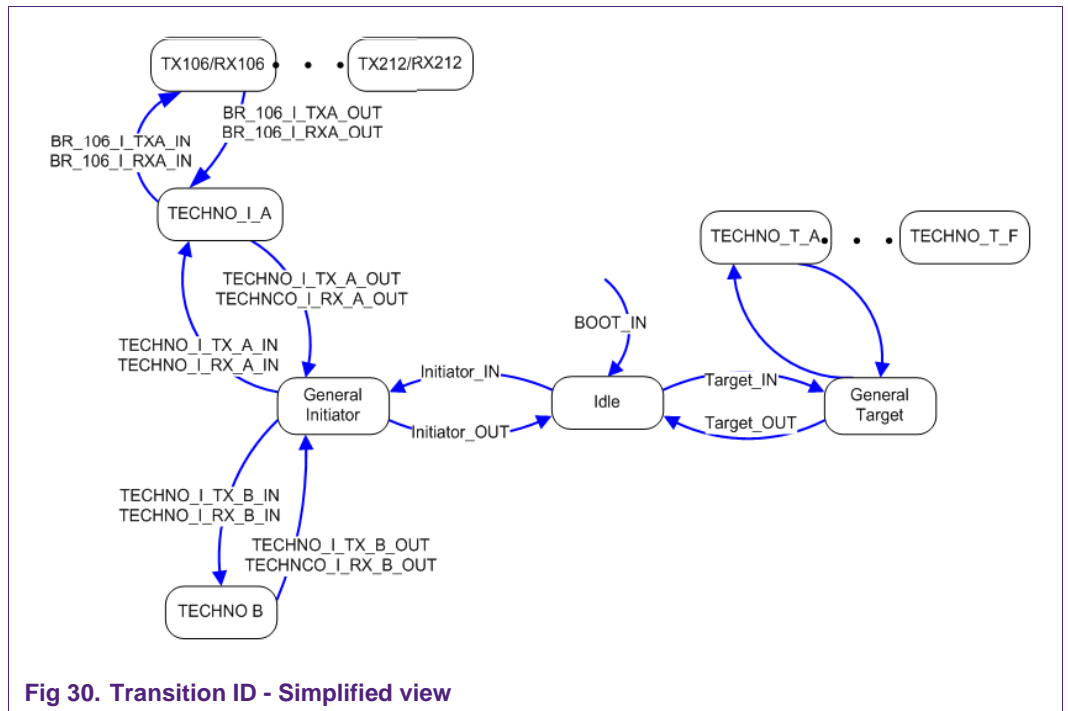


Fig 30. Transition ID - Simplified view

Basically, PN7120 goes to one state or another, but cannot jump to a state where no link is defined, which makes the solution more robust. The transitions are defined as below:

- BOOT
 - o Called at boot time
 - o Basic initialization of CLIF (e.g. SMU_ANA_TX_STANDBY_REG)
- INITIATOR
 - o Called at the beginning of the poller phase

- Initialization common Reader/Initiator mode settings
- TARGET
 - Called when external field is detected and CE/P2P Target is active
 - Initialization of common CE/Target mode settings
- TECHNO_I_RX_X, TECHNO_I_TX_X, TECHNO_T_RX_X, TECHNO_T_TX_X
 - Initialization of common technology dependent settings for transmitter and receiver
- BR_XXX
 - Initialization of bit rate specific settings for transmitter and receiver for all different technologies / modes

The exhaustive list of transitions IDs is given as below.

Table 7. Transition ID values

Transition ID	IN	OUT
RF CLIF BOOT	0	1
RF_CLIF_CFG_IDLE	2	3
RF CLIF CFG INITIATOR	4	5
RF CLIF CFG TARGET	6	7
RF CLIF CFG I PASSIVE	8	9
RF CLIF CFG I ACTIVE	A	B
RF CLIF CFG T PASSIVE	C	D
RF CLIF CFG T PREACTIVE	E	F
RF_CLIF_CFG_T_ACTIVE	10	11
RF CLIF CFG TECHNO I TXA	12	13
RF CLIF CFG TECHNO I RXA P	14	15
RF CLIF CFG TECHNO I TXB	16	17
RF CLIF CFG TECHNO I RXB	18	19
RF CLIF CFG TECHNO I TXF	1A	1B
RF CLIF CFG TECHNO I RXF P	1C	1D
RF_CLIF_CFG_TECHNO_I_RXF_A	1E	1F
RF CLIF CFG TECHNO I TX15693	20	21
RF CLIF CFG TECHNO I RX15693	22	23
RF CLIF CFG TECHNO T TXA P	24	25
RF CLIF CFG TECHNO T RXA	26	27
RF CLIF CFG TECHNO T TXB	28	29
RF CLIF CFG TECHNO T RXB	2A	2B
RF_CLIF_CFG_TECHNO_T_TXF_P	2C	2D
RF CLIF CFG TECHNO T TXF A	2E	2F

Transition ID	IN	OUT
RF CLIF CFG TECHNO T RXF	30	31
RF_CLIF_CFG_BR_106_I_TXA	32	33
RF CLIF CFG BR 106 I RXA P	34	35
RF CLIF CFG BR 106 I RXA A	36	37
RF CLIF CFG BR 212 I TXA	38	39
RF CLIF CFG BR 212 I RXA	3A	3B
RF_CLIF_CFG_BR_424_I_TXA	3C	3D
RF CLIF CFG BR 424 I RXA	3E	3F
RF CLIF CFG BR 848 I TXA	40	41
RF CLIF CFG BR 848 I RXA	42	43
RF CLIF CFG BR 106 I TXB	44	45
RF CLIF CFG BR 106 I RXB	46	47
RF CLIF CFG BR 212 I TXB	48	49
RF CLIF CFG BR 212 I RXB	4A	4B
RF CLIF CFG BR 424 I TXB	4C	4D
RF CLIF CFG BR 424 I RXB	4E	4F
RF_CLIF_CFG_BR_848_I_TXB	50	51
RF CLIF CFG BR 848 I RXB	52	53
RF CLIF CFG BR 212 I TXF	54	55
RF CLIF CFG BR 212 I RXF P	56	57
RF CLIF CFG BR 212 I RXF A	58	59
RF CLIF CFG BR 424 I TXF	5A	5B
RF CLIF CFG BR 424 I RXF P	5C	5D
RF CLIF CFG BR 424 I RXF A	5E	5F
RF CLIF CFG BR 26 I TX	60	61
RF CLIF CFG BR 26 I RX	62	63
RF CLIF CFG BR 53 I TX	64	65
RF CLIF CFG BR 53 I RX	66	67
RF CLIF CFG BR 106 T TXA P	68	69
RF CLIF CFG BR 106 T TXA A	6A	6B
RF_CLIF_CFG_BR_106_T_RXA	6C	6D
RF CLIF CFG BR 212 T TXA	6E	6F
RF CLIF CFG BR 212 T RXA	70	71
RF CLIF CFG BR 424 T TXA	72	73
RF CLIF CFG BR 424 T RXA	74	75
RF CLIF CFG BR 848 T TXA	76	77

Transition ID	IN	OUT
RF CLIF CFG BR 848 T RXA	78	79
RF_CLIF_CFG_BR_106_T_TXB	7A	7B
RF CLIF CFG BR 106 T RXB	7C	7D
RF CLIF CFG BR 212 T TXB	7E	7F
RF CLIF CFG BR 212 T RXB	80	81
RF CLIF CFG BR 424 T TXB	82	83
RF_CLIF_CFG_BR_424_T_RXB	84	85
RF CLIF CFG BR 848 T TXB	86	87
RF CLIF CFG BR 848 T RXB	88	89
RF CLIF CFG BR 212 T TXF P	8A	8B
RF CLIF CFG BR 212 T TXF A	8C	8D
RF CLIF CFG BR 212 T RXF	8E	8F
RF CLIF CFG BR 424 T TXF P	90	91
RF CLIF CFG BR 424 T TXF A	92	93
RF CLIF CFG BR 424 T RXF	94	95
RF CLIF GTM A	96	97
RF_CLIF_GTM_B	98	99
RF CLIF GTM FELICA	9A	9B
RF CLIF CMA	9C	9D

The registers can be one to 4 Bytes long. As an example, Fig 31 shows the CLIF_ANA_TX_AMPLITUDE_REG register in transition TARGET_IN to 0xF3F30000.

Note that the byte order for the register value is defined as Little Endian, meaning LSByte written first (LSB to MSB).

The order of the different bytes is given as follows (32 bits):

[7:4] [3:0] [15:12] [11:8] [23:20] [19:16] [31:28] [27:26]

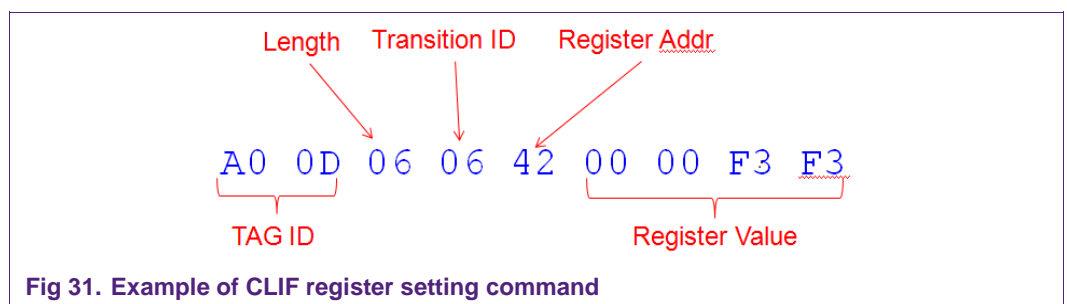


Fig 31. Example of CLIF register setting command

5.3.2 Configuring load modulation in CARD mode

In CARD mode, load modulation is performed by switching the ANT1/ANT2 pins between high impedance to low impedance, which switches the CANT capacitors in parallel to the antenna ON and OFF.

5.3.2.1 CLIF_ANA_TX_AMPLITUDE_REG

It is also possible to have an extra load switch between TX1 & TX2 in addition to CANT capacitors, which increases the LMA effect further.

This is based on the *CLIF_ANA_TX_AMPLITUDE_REG* register using *TX_GSN_CW_CM* and *TX_GSN_MOD_CM* parameters.

Register name	Transition ID	Register Address	Default Value
CLIF_ANA_TX_AMPLITUDE_REG	0x06	0x42	0xFFF10000
CLIF_ANA_TX_AMPLITUDE_REG	0x9A	0x42	0xF1F10001

Fig 32. Fine tuning of CLIF_ANA_TX_AMPLITUDE_REG register in CARD mode

This tuning must ensure a correct operation and interoperability between PCD and PICC products.

Performance for high distance communication (Low field strength) must be checked against readers like Pegoda and payment readers.

In addition to the readers, the following test benches shall be used to get the best performance:

- 1- EMVCo test bench to define minimum functionality for PICC and PCD usage vs. RF powering, frames, timings, Type A, Type B commands.
- 2- ISO test bench to verify the operation of a PICC vs. ISO/IEC 14443-2, and ensures independency vs. coupling effect.

This chapter covers the EMVCo test bench methodology. Please refer to *Book D – EMVco [3]* chapter 3.4 and 4, to get more insight on Load Modulation definition, mechanism and timing constraints.

Register definition

Bits [27:24] & [19.16] adjust the N-MOS transistor conductance value applied during non-modulated phases (CW- Continuous Wave) and modulated phase (MOD- Modulation phase) respectively (see *Fig 33*).

[0001] means minimum conductance (maximum impedance), and vice versa.

Note that [0000] shall not be used.

Based on these adjustments, the load modulation shape can be improved to comply with the targeted standards, including interoperability.

CLIF_ANA_TX_AMPLITUDE_REG			
Bit	Name	Value 0xFFFF10000	Description
[31:28]	TX_GSN_CW_RM	1111	gsn setting @ continuous wave in poll mode
[27:24]	TX_GSN_CW_CM	1111	gsn setting @ continuous wave in listen mode
[23:20]	TX_GSN_MOD_RM	1111	gsn setting @ modulation in poll mode
[19:16]	TX_GSN_MOD_CM	0001	gsn setting @ modulation in listen mode
[15:14]	RFU	00	
[13:12]	TX_CW_AMPLITUDE_RM	00	Set amplitude of unmodulated carrier @ poll mode
[11:10]	RFU	00	
[9:8]	RFU	00	
[7:3]	TX_RESIDUAL_CARRIER	00000	Set amplitude of unmodulated carrier
[2]	TX_CW_TO_MAX_RM	0	TX HI output is the maximum voltage obtainable from charge pump
[1]	RFU	0	
[0]	TX_PD	0	Charge pumps clamped to tvdd

Fig 33. CLIF_ANA_TX_AMPLITUDE_REG register definition in listen mode

Register setting procedure

- a) Adjusting CW GSN to get optimal field strength from the reader (best sensitivity on RX)

Parameter

- 1- CLIF_ANA_TX_AMPLITUDE_REG [19:16]= [6] (e.g. of fix value)
- 2- CLIF_ANA_TX_AMPLITUDE_REG [27:24]= From 1 to F

Measurement

- 1- Run EMVCo CA121 @ 4cm (or 5cm if no proven results)
- 2- Read distance on Pegoda

Target

- 1- Select the range of CW for which CA121 passes (OK)
- 2- Get the best CW value which provides the highest distance

- b) Adjusting MOD GSN to get optimal Pegoda distance (optimal LMA on TX)

Parameter

- 1- CLIF_ANA_TX_AMPLITUDE_REG [27:24]= [best value from previous test]
- 2- CLIF_ANA_TX_AMPLITUDE_REG [19:16]= Adjust to 1, 3, 9, F

Measurement

- 1- Read distance on Pegoda
- 3- Perform EMVCo test CA131 @ 2 (LMA) and get value.

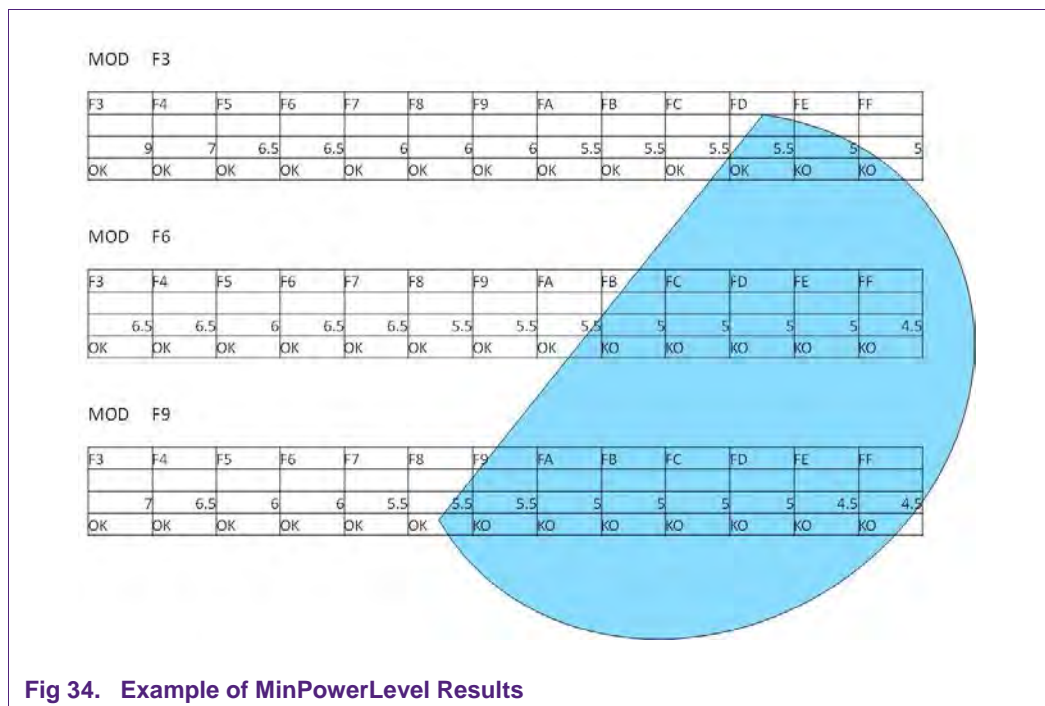
Target

- 1- Get MOD for highest distance, and confirm
- 2- Confirm LMA passes for selected MOD value and with 3cm and 4cm.

Measurement examples

The graphs below show a selection of measurements regarding distance, MinPowerLevel and LMA. The best [CW, MOD] can be selected accordingly:

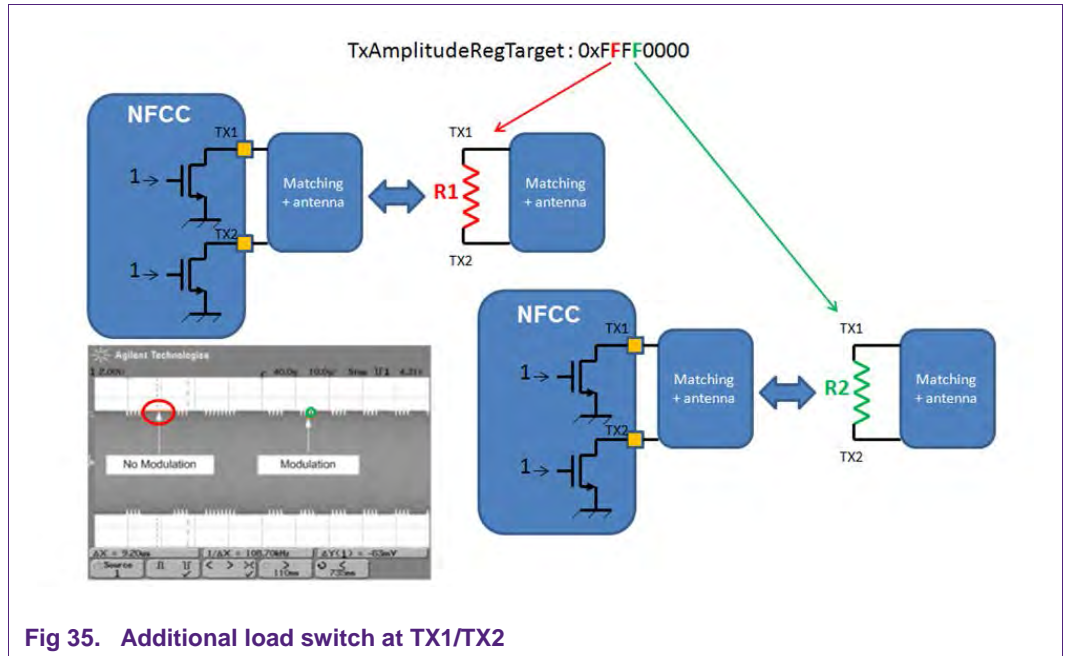
[CW, MOD] = (1,6), but a range within (1,6)(1,6) can be considered in case of interoperability issues.



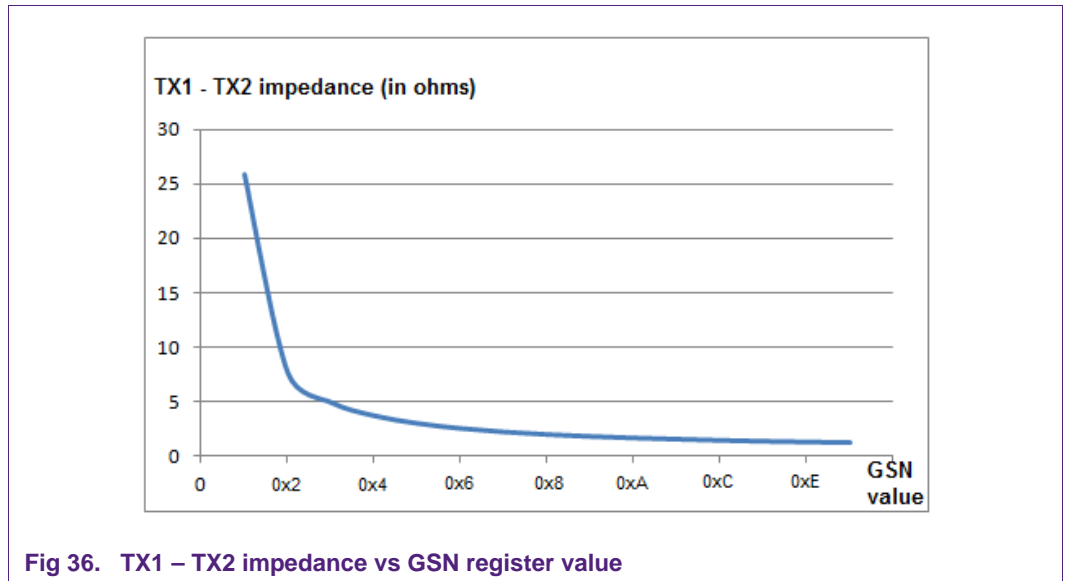
Schematics principle

Typical TX impedance versus GSN register value is depicted on **Error! Reference source not found.**

When TX_GSN_MOD_CM is different from TX_GSN_CW_CM a load switch between TX1 & TX2 is applied on top of the C2b capacitor switch.



Typical impedance on TX1 or TX2 for a given GSN value is shown on the curve below:



Transition to update

The update of the CLIF_ANA_TX_AMPLITUDE_REG must be done for 2 different transitions:

- Transition 0x06 for type A and B
- Transition 0x9A for type F

5.3.3 Configuring pulse shape in poll mode

a. Type A definition

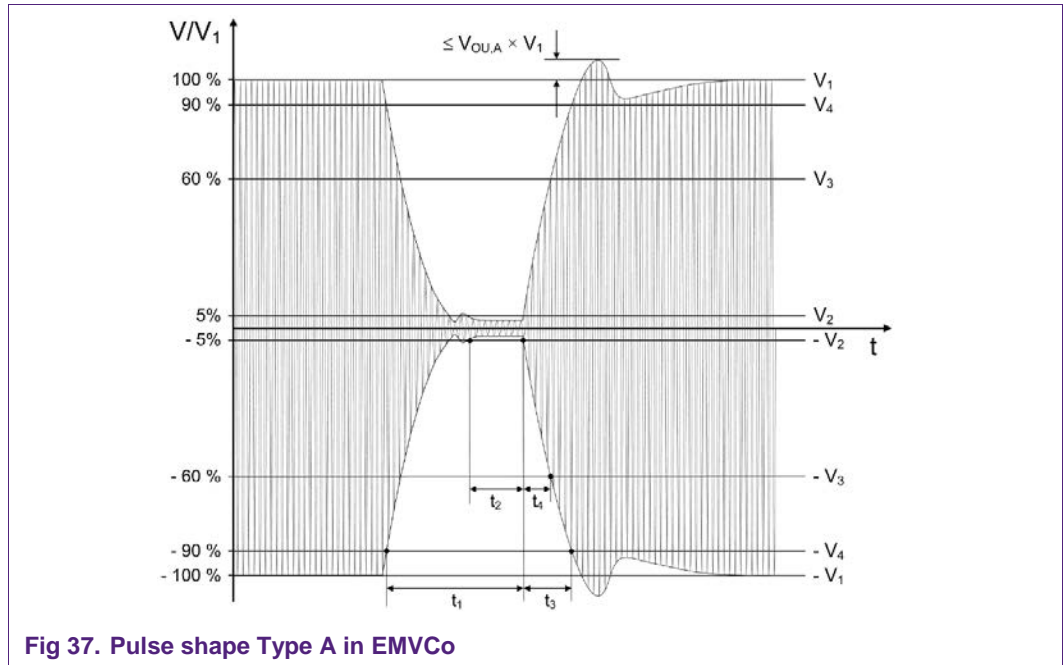


Fig 37. Pulse shape Type A in EMVCo

The time t1-t2 describes the time span in which the signal falls from 90% down below 5% of the signal amplitude. The most critical time concerning rising carrier envelope is t4. It must be checked that the carrier envelope at the end of the pause reaches 60% of the continuous wave amplitude within 0.4µs.

Ringing following the falling edge shall remain below $V_{ou,A} \times V_1$.

Overshoots immediately following the rising edge shall remain within $(1 \pm V_{ou,A}) \times V_1$.

Please refer to Book D – EMVCo [3] to get t1, t2, t3, t4 and $V_{ou,A}$ values.

b. Type B definition

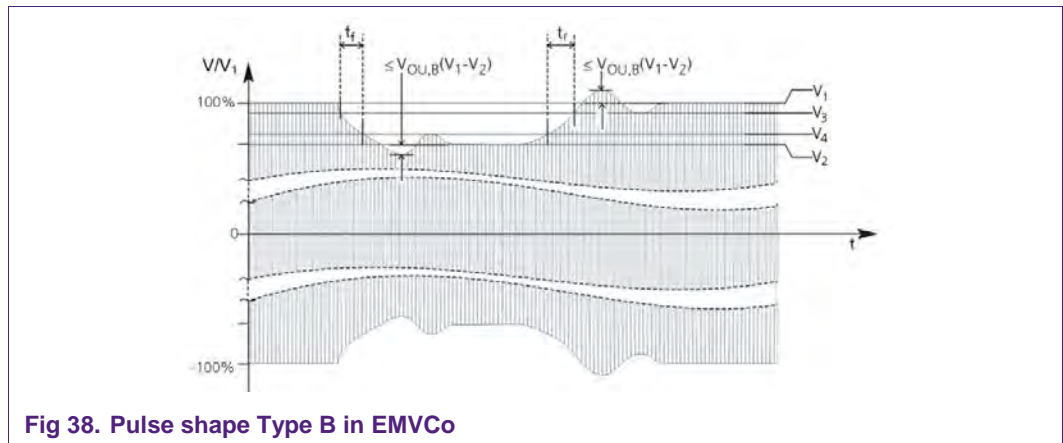


Fig 38. Pulse shape Type B in EMVCo

V1 is the initial value measured immediately before any modulation is applied by the reader.

V2 is the lower value.

The modulation index (mi), V3 and V4 are defined as follows:

$$mi = (V1-V2)/(V1+V2)$$

$$V3 = V1 - 0.1*(V1-V2)$$

$$V4 = V2 + 0.1*(V1-V2)$$

Please refer to *Book D – EMVCo [3]* to get the values of modi, tf, tr and Vou,B.

The following register can be fine-tuned to improve the shaping of the pulse in Type A and Modulation index in Type B.

5.3.3.1 CLIF_ANA_TX_AMPLITUDE_REG

CLIF_ANA_TX_AMPLITUDE_REG with the transition ID #44 is the register to configure.

Register name	Transition ID	Register Address	Default Value
CLIF_ANA_TX_AMPLITUDE_REG	0x44	0x42	0xFFFF1090

Fig 39. Fine tuning of CLIF_ANA_TX_AMPLITUDE_REG register

Register definition

Bits [31:28] & [23:20] adjust the N-MOS transistor conductance value applied during non-modulated phases (CW- Continuous Wave) and modulated phase (MOD- Modulation phase) respectively.

- [31:28]: It is recommended to keep it at its maximum value (F), to get maximum envelop of the carrier amplitude of type B modulation
- [23:20]: It plays on the modulation index in Type B.

Bits [13:12] & [7:3] adjust the load modulation amplitude by choosing the amplitude of the output signal generated at PN7120 TX pin.

- [13:12] plays on modulation index Type B by degrading CW amplitude. When set to '3', type A amplitude appears larger than Type B
- [7:3] plays on the modulation index Type B. The higher the value, the higher the modulation index

Bit [2]: It is recommended to fix this value to '0' which improves the modulation index Type B.

CLIF_ANA_TX_AMPLITUDE_REG			
Bit	Name	Value 0xFFFF1090	Description
[31:28]	TX_GSN_CW_RM	1111	gsn setting @ continuous wave in poll mode
[27:24]	TX_GSN_CW_CM	1111	gsn setting @ continuous wave in listen mode
[23:20]	TX_GSN_MOD_RM	1111	gsn setting @ modulation in poll mode
[19:16]	TX_GSN_MOD_CM	0001	gsn setting @ modulation in listen mode
[15:14]	RFU	00	
[13:12]	TX_CW_AMPLITUDE_RM	00	Set amplitude of unmodulated carrier @ poll mode
[11:10]	RFU	00	
[9:8]	RFU	00	
[7:3]	TX_RESIDUAL_CARRIER	00000	Set amplitude of unmodulated carrier
[2]	TX_CW_TO_MAX_RM	0	TX HI output is the maximum voltage obtainable from charge pump
[1]	RFU	0	
[0]	TX_PD	0	Charge pumps clamped to tvdd

Fig 40. CLIF_ANA_TX_AMPLITUDE_REG register definition in poll mode

Register setting procedure

a) Adjusting TX_RESIDUAL_CARRIER

Parameter

- 1- Start with CLIF_ANA_TX_AMPLITUDE_REG [7:0]= [90] (default value)
- 2- CLIF_ANA_TX_AMPLITUDE_REG [7:0] = A0 then B0, C0, C8 to increase index
- 3- CLIF_ANA_TX_AMPLITUDE_REG [7:0] = 80 then 70, 60 to decrease index

Measurement

- 1- Utilize a PICC card and an oscilloscope to observe the LMA and modulation index Type B @ 0cm, then 1cm. Both must meet the standard

Target

- 1- Select CLIF_ANA_TX_AMPLITUDE_REG [7:0] for which modulation index is OK

If TX_RESIDUAL_CARRIER adjustment is not enough, try TX_CW_AMPLITUDE_RM tuning.

b) Adjusting TX_CW_AMPLITUDE_RM

Parameter

- 1- Select the best CLIF_ANA_TX_AMPLITUDE_REG [7:3] value
- 2- CLIF_ANA_TX_AMPLITUDE_REG [13:12] = 0, 1, 2 or 3

Measurement

- 1- Utilize a PICC card and an oscilloscope to observe the LMA @ 0cm, then 1cm

Target

- 1- Select CLIF_ANA_TX_AMPLITUDE_REG [13:12] for which modulation index OK

If TX_CW_AMPLITUDE_RM adjustment is not enough, try TX_GSN_CW_RM & TX_GSN_MOD_RM tuning.

c) Adjusting TX_GSN_CW_RM & TX_GSN_MOD_RM

Parameter

- 1- Keep CLIF_ANA_TX_AMPLITUDE_REG [31:28] = F
- 2- CLIF_ANA_TX_AMPLITUDE_REG [23:20] = 5

Measurement

- 1- Utilize a PICC card and an oscilloscope to observe the LMA @ 0cm, then 1cm

Target

- 1- Select CLIF_ANA_TX_AMPLITUDE_REG [23:20] for which modulation index OK

5.3.4 Optimizing Rx path in poll mode

5.3.4.1 CLIF_ANA_RX_REG

CLIF_ANA_RX_REG can be fine-tuned to improve the analog down-sampling and baseband amplification of the card response before it is processed by the digital block.

Register name	Transition ID	Register Address	Default Value
CLIF_ANA_RX_REG	0x22	0x44	0x00020029
CLIF_ANA_RX_REG	0x34	0x44	0x00020021
CLIF_ANA_RX_REG	0x35	0x44	0x00020021
CLIF_ANA_RX_REG	0x46	0x44	0x00020021
CLIF_ANA_RX_REG	0x4A	0x44	0x00020021
CLIF_ANA_RX_REG	0x4E	0x44	0x00020021
CLIF_ANA_RX_REG	0x52	0x44	0x00020021
CLIF_ANA_RX_REG	0x5C	0x44	0x00020021
CLIF_ANA_RX_REG	0x56	0x44	0x00020021

Fig 41. Fine tuning of CLIF_ANA_RX_REG register

Register definition

Bits [3:2] set the lower corner frequency of the BBA internal band-pass filter to reduce analog demodulation interferences.

Care:

- If the corner frequency is set too close or above the actual baseband signal frequency, the signal strength of the « useful » signal is dampened, leading to a loss of reading range, but at the same time it can also stabilize the reader performance
- => Tradeoff might be necessary.
- Furthermore the RX_HPCF parameter influences the BBA amplification level (gain). The higher the HPCF, the lower the gain (1-2dB / per setting).
- For a reliable setting of the HPCF the observation of the frequency spectrum of the BBA input should be available for the given design
- => Since not available, each setting has to be evaluated by functional testing

Value range:

- For 106kbps baseband signals: 0b00 ... 0b10
- For 212kbps baseband signals: 0b00 ... 0b11
- For 424kbps baseband signals: 0b00 ... 0b11
- For 848kbps baseband signals: 0b00 ... 0b11

Bits [1:0] set the amplification level of the **BaseBandAmplifier**

Care:

- The gain must be set in combination with the HPCF parameter taking into account the optimization of the disturbances in the down-mixed RX signal.

Value range:

- High performance & sensitivity for max. reading range: 0b10 ... 0b11
 - o Strongly depends on the SNR in the system
- Typical: 0x01 ... 0x10
- High robustness & stability but low reading range : 0x00

CLIF_ANA_RX_REG			
Bit	Name	Value 0x00020021	Description
[31:4]	RFU	x	
[3:2]	RX_HPCF	00	Lower Corner Frequency: 00->45kHz, 01->85kHz, 10->150kHz, 11->250kHz
[1:0]	RX_GAIN	01	Gain Adjustment BBA: 00->33dB, 01->40dB, 10->50dB, 11->57dB

Fig 42. CLIF_ANA_RX_REG register definition

Register setting procedureParameter

- 1- CLIF_ANA_RX_REG [3:2]= from 00 to 11
- 2- CLIF_ANA_RX_REG [1:0]= from 00 to 11

Measurement

- 1- Use DESFire EV1, MIFARE UL, TOPAZ and measure distance

Target

- 1- Select settings for which distance is improved

Remark: For each communication type and baud rate, you must choose the right transition. In *Table 8* you will find the transition which corresponds to each tag type.

Table 8. CLIF_ANA_RX_REG transitions

	Baud rate	Transition ID
Type A	106	34
	212	
	424	35
	848	
Type B	106	46
	212	4A
	424	4E
	848	52
Type F	212	56
	424	5C
Type ISO15693	-	22

5.3.4.2 CLIF_SIGPRO_RM_CONFIG1_REG

CLIF_SIGPRO_RM_CONFIG1_REG can be used to tune the digital signal processing regarding the bit and subcarrier detection for the down-sampled and amplified listen mode response.

Register name	Transition ID	Register Address	Default Value
CLIF_SIGPRO_RM_CONFIG1_REG	0x22	0x2D	0x000C4450
CLIF_SIGPRO_RM_CONFIG1_REG	0x34	0x2D	0x000C50DC
CLIF_SIGPRO_RM_CONFIG1_REG	0x3A	0x2D	0x001F5715
CLIF_SIGPRO_RM_CONFIG1_REG	0x3E	0x2D	0x001F5715
CLIF_SIGPRO_RM_CONFIG1_REG	0x42	0x2D	0x000F33DD
CLIF_SIGPRO_RM_CONFIG1_REG	0x46	0x2D	0x000C4805
CLIF_SIGPRO_RM_CONFIG1_REG	0x4A	0x2D	0x000C4805
CLIF_SIGPRO_RM_CONFIG1_REG	0x4E	0x2D	0x000C4805
CLIF_SIGPRO_RM_CONFIG1_REG	0x52	0x2D	0x000C4805
CLIF_SIGPRO_RM_CONFIG1_REG	0x56	0x2D	0x000CCC05
CLIF_SIGPRO_RM_CONFIG1_REG	0x5C	0x2D	0x000CCC05

Fig 43. Fine tuning of CLIF_SIGPRO_RM_CONFIG1_REG register

Register definition

Bits [15:12] define the threshold for the bit and subcarrier detection based on the amplitude of the correlated I & Q channel signal. It is used for all listen mode response types.

Bits [11:8] define the threshold for the phase shift detection based on the amplitude of the correlated I & Q channel. It is used for Type B (all baud rates) and Type A higher baud rates in addition to the Min_Level

For Min_Level and Min_Level_P:

- High value: receiver will be less sensitive but more robust against noise
- Low value: receiver will become sensitive to small card response but also to noise in the system
- Strong dependency on ANA_RX_REG

Care:

- Direct result of a register change is visible after a functional with Target activated
- Since the amplitude of the correlated I&Q channels is evaluated, the whole receiver path configuration has a major impact on the final register value (from the RXN/ RXP-pins to the BBA output)

Value range:

- High performance & sensitivity for max. reading range: 0x2 ... 0x5
- Typical: 0x5 ... 0x9
- High robustness & stability but low reading range : 0x9 ... 0xF

Bits [6:5] define the required signal strength/threshold of an incorrect modulation for Type A-106kbps meaning the second half bit is also modulated. If the correlated I/Q signal for the un-modulated half bit is above this threshold a collision is detected.

Care:

- The higher the coil level the more robust the system will be but at the same time also less sensitive if it comes to detection of two cards

Value range:

- Typical : 0b00 ...0b01

CLIF_SIGPRO_RM_CONFIG1_REG			
Bit	Name	Value 0x000390A3	Description
[31:16]	RFU	x	
[15:12]	MIN_LEVEL	0101	Define the min level of the reception
[11:8]	MIN_LEVEL_P	0000	Define the min level for the phase shift detector unit
[7]	RFU	x	
[6:5]	COIL_LEVEL	10	Defines how strong a signal must be to be interpreted as a collision for Manchester subcarrier communication types. 00* > 12;5%; 01 > 25%; 10 > 50%; 11 No Collision
[4:0]	RFU	x	

Fig 44. CLIF_SIGPRO_RM_CONFIG1_REG register definition

Register setting procedure

Parameter

- 1- CLIF_SIGPRO_RM_CONFIG1_REG [15:12]= from 00 to 11
- 2- CLIF_SIGPRO_RM_CONFIG1_REG [11:8] = from 00 to 11

Measurement

- 1- Use DESFire EV1, MIFARE UL, TOPAZ and measure distance (see annex 1)

Target

- 1- Select settings for which distance is improved

Remark: For each communication type and baud rate, you must choose the right transition. In *Table 9* you will find the transition which corresponds to each tag type.

Table 9. CLIF_SIGPRO_RM_CONFIG1_REG transitions

	Baud rate	Transition ID
Type A	106	34
	212	3A
	424	3E
	848	42
Type B	106	46
	212	4A
	424	4E
	848	52
Type F	212	56
	424	5C
Type ISO15693	-	22

5.3.5 Configuring FDT

5.3.5.1 CLIF_TRANSCEIVE_CONTROL_REG

CLIF_TRANSCEIVE_CONTROL_REG can be adjusted to meet FDT requirement.

Register name	Transition ID	Register Address	Default Value
CLIF_TRANSCEIVE_CONTROL_REG	0x06	0x03	0x7000
CLIF_TRANSCEIVE_CONTROL_REG	0x32	0x03	0x3D40

Fig 45. Fine tuning of CLIF_TRANSCEIVE_CONTROL_REG

Register definition

CLIF_TRANSCEIVE_CONTROL_REG			
Bit	Name	Value 0x7000	Description
[15:8]	TX_BITPHASE	1110000	Defines the number of 13.56MHz cycles used for adjustment of tx_wait to meet the FDT.
7	RFU	0	
6	TX_MILLER_SYNC_ENABLE	0	1' => Guard time is synchronized to miller envelope for transmission. Used for AGC.
5	TX_SKIP_SEND_ENABLE	0	1' => No transmission is started after tx_wait is expired and START_SEND was set. Note: The bit is cleared by HW when the WaitReceive state is .
4	TX_PICC2_TIMESLOT_ENABLE	0	1' => Two PICC responses are transmitted in different timeslots. Note: Only valid when command Transceive is active
3	TX_FRAMESTEP_ENABLE	0	1' => At every start of transmission, each byte of data is sent in a separate frame. SOF and EOF is appended to the data byte according to the framing settings. After one byte is transmitted, the TxEncoder waits for a new start trigger to continue with the next byte
2	RX_MULTIPLE_ENABLE	0	1' => The receiver is re-activated after the end of a reception. A statusbyte is written to the RAM containing all relevant status information of the frame.
1	MILLER_SYNC_ENABLE	0	1' => Miller pulse synchronisation is enabled. Note: TX_BITPHASE is used to adjust the prescaler of the guard timer. Note: This bit is set by HW when TypeA protocol is detected in automatic mode detection.
0	INITIATOR	0	1' => The CLIF is configured for initiator mode. Depending on this setting the behavior of the transceive command is different

Fig 46. CLIF_TRANSCEIVE_CONTROL_REG register definition

5.3.6 Configuring TX control

5.3.6.1 CLIF_TX_OVERSHOOT_CONTROL_REG

CLIF_TX_OVERSHOOT_CONTROL_REG can be adjusted to protect transmission against overshoot.

Register name	Transition ID	Register Address	Default Value
CLIF_TX_OVERSHOOT_CONTROL_REG	0x06	0x15	0x00

Fig 47. Fine tuning of CLIF_TX_OVERSHOOT_CONTROL_REG

Register definition

CLIF_TX_OVERSHOOT_CONTROL_REG			
Bit	Name	Value 0x00	Description
[7:5]	RFU	0	
[4:1]	TX_OVERSHOOT_PATTERN_LEN	0000	Defines length of the overshoot prevention pattern (value +1). The pattern is applied starting from the MSB of the defined pattern, all other bits are ignored.
0	TX_OVERSHOOT_PROT_ENABLE	0	If set to 1, the overshoot protection is enabled.

Fig 48. CLIF_TX_OVERSHOOT_CONTROL_REG register definition

5.3.6.2 CLIF_TX_UNDERSHOOT_CONTROL_REG

CLIF_TX_UNDERSHOOT_CONTROL_REG can be adjusted to protect transmission against undershoot.

Register name	Transition ID	Register Address	Default Value
CLIF_TX_UNDERSHOOT_CONTROL_REG	0x06	0x16	0x00

Fig 49. Fine tuning of CLIF_TX_UNDERSHOOT_CONTROL_REG

Register definition

CLIF_TX_UNDERSHOOT_CONTROL_REG			
Bit	Name	Value 0x00	Description
[7:5]	RFU	0	
[4:1]	TX_UNDERSHOOT_PATTERN_LEN	0000	Defines length of the undershoot prevention pattern (value +1). The pattern is applied starting from the MSB of the defined pattern, all other bits are ignored.
0	TX_UNDERSHOOT_PROT_ENABLE	0	If set to 1, the undershoot protection is enabled.

Fig 50. CLIF_TX_UNDERSHOOT_CONTROL_REG register definition

5.3.6.3 CLIF_ANA_TX_SHAPE_CONTROL_REG

CLIF_ANA_TX_SHAPE_CONTROL_REG can be used to shape the TX transmission signal in type A, by adjusting its rising/falling edge.

Register name	Transition ID	Register Address	Default Value
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x20	0x4A	0x00000000
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x32	0x4A	0x1B010753
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x38	0x4A	0x1B010756
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x3C	0x4A	0x1B010756
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x40	0x4A	0x00000715
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x44	0x4A	0x07010743
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x48	0x4A	0x07010743
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x4C	0x4A	0x07010743
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x50	0x4A	0x07010732
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x54	0x4A	0x07010743
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x5A	0x4A	0x07010763
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x6A	0x4A	0x1B010753
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x8C	0x4A	0x07010743
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x92	0x4A	0x07010763

Fig 51. Fine tuning of CLIF_ANA_TX_SHAPE_CONTROL_REG

Register definition

CLIF_ANA_TX_SHAPE_CONTROL_REG			
Bit	Name	Value	Description
		0x1B010753	
[31:29]	RFU	0	
[28:24]	TX_RESIDUAL_CARRIER_OV_PREV	1101	Defines the value for the residual carrier for the period the overshoot prevention pattern is active
[23:17]	RFU	0	
16	TX_SET_SINGLE_CP_MODE	1	Enables single charge-pump mode; Allows RC-shaping of modulation waveform
[15:12]	RFU	0	
[11:8]	TX_SET_SLEW_SHUNTREG	0111	Set slew rate for shunt regulator
[7:4]	TX_SET_TAU_MOD_FALLING	0101	Transmitter TAU setting for falling edge of modulation shape. In AnalogControl module the output signal is switched with the tx_envelope. Only valid is TX_SET_SINGLE_CP_MODE is set
[3:0]	TX_SET_TAU_MOD_RISING	0011	Transmitter TAU setting for rising edge of modulation shape. In AnalogControl module the output signal is switched with the tx_envelope. Only valid is TX_SET_SINGLE_CP_MODE is set

Fig 52. Fig 37.CLIF_ANA_TX_SHAPE_CONTROL_REG register definition

Register setting procedure

Parameter

- 1- CLIF_ANA_TX_SHAPE_CONTROL_REG [3:0]= from 0 to F (tr, rising edge)
- 2- CLIF_ANA_TX_SHAPE_CONTROL_REG [7:4]= from 0 to F (tf, falling edge)
- 3- CLIF_ANA_TX_SHAPE_CONTROL_REG [16] must be set to 1

Measurement

- 1- Use oscilloscope and zoom as depicted in the picture below

Target

- 1- Select settings for which the timing meets the spec
- 2- 0 value means faster rising and falling edges (potential overshoot, undershoot issue)
- 3- F value means smoother rising and falling edges

6. Reference design

The PN7120 have been widely tested and validated with below described single loop antenna.

6.1.1 Antenna reference

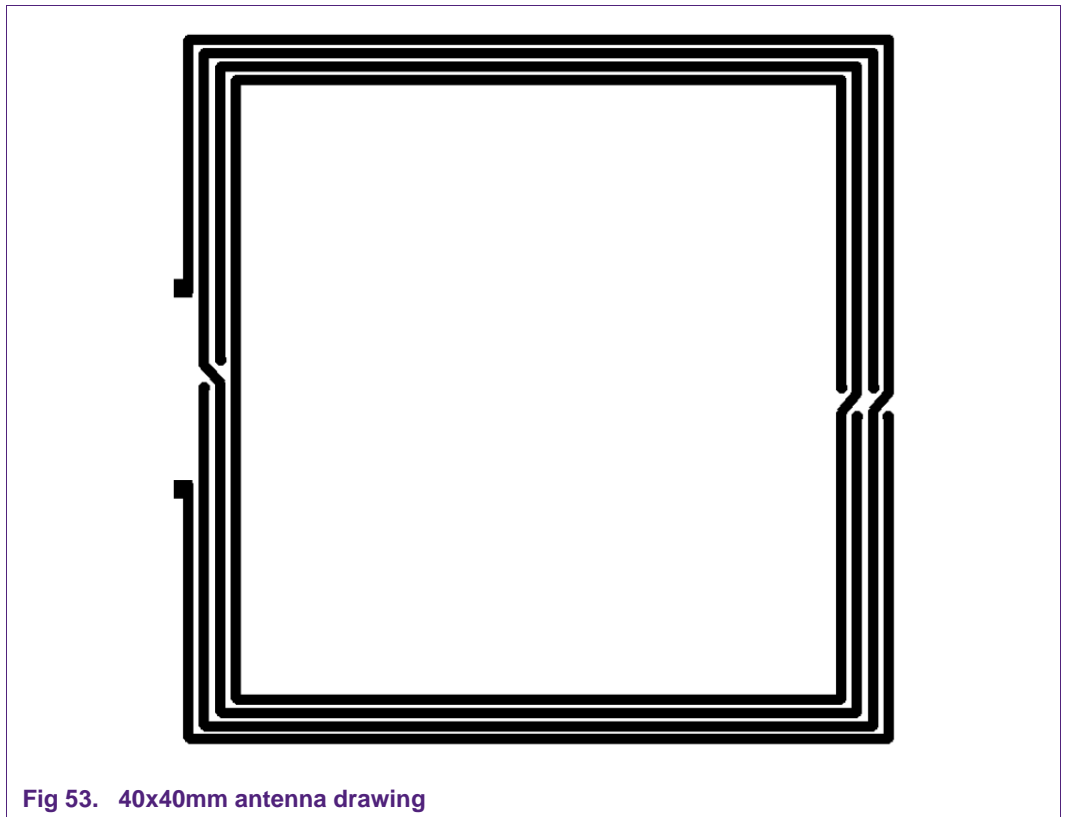


Fig 53. 40x40mm antenna drawing

Table 10. 40x40mm Antenna outlines

Physical outlines of the antenna board are shown here

Description	Value	Unit
size	40 x40	mm
# turns	4	
Copper width	0.4	mm
Spacing	0.3	mm
Copper height	35	µm

This antenna is tested in open air environment (no ferrite or metal sheet below).

The expected antenna performances are given in *Table 11*:

Table 11. 40x40mm Antenna expected performances

Tested Item	Expected performances
Detection distance with a MIFARE Ultralight ID1 PICC (antenna center aligned)	3,5 cm
NFC Forum reader compliance	Full compliance expected for PN7120
Sideband amplitude measured on an ISO10373-6 assembly PCD bench	Full compliance from 1.5A/m to 7.5A/m
Load modulation amplitude measured on an EMVCo 2.2 bench	Full compliance up to 4cm in the whole EMVCo operating volume
Detection distance with a Pegoda reader v1 (antenna center aligned)	7,5 cm

6.1.2 Recommended characteristics

In case you want to design your own single loop antenna for the PN7120, it is recommended to respect the below described characteristics:

Table 12. Recommended standard coil antenna physical characteristics

Description	Min	Max
Size	500 mm ²	5000 mm ²
# turns	2	8
Copper width	0.2mm	2mm
Spacing	0.2mm	2mm
Copper thickness	20µm	

7. References

- [1] ISO/IEC10373-6 standard – Identification cards – Test methods – Part 6: Proximity cards – 2011 release
- [2] ISO/IEC14443-2 standard – Identification cards - Contactless integrated circuit(s) cards – Proximity cards – 2010 release
- [3] Book D- EMV Contactless Communication Protocol Specification- Version 2.5 February 2013
- [4] NFC Forum – NFC Analog Specification - 2012 release
- [5] UM10819 - PN7120 User Manual

8. Abbreviations

Abbr.	Meaning
A/m	Amper per meter (magnetic field strength measurement unit)
AGC	Automated Gain Control
AN	Application Note
CH1 / CH2	Channel 1 / Channel 2
EMC	ElectroMagnetic Compatibility
Hmin / Hmax	Minimal and Maximum magnetic field strength
H-field	Magnetic field
IC	Integrated Circuit
ISO/IEC	International Standard Organization / International Electrotechnical Community
mA	milli Ampere
MHz	Mega Hertz
NFC	Near Field Communication
NFC	NFC Controller (i.e. PN7120)
PC	Personal Computer
PCB	Printed Circuit Board
PCD	Proximity Coupling Device (Contactless reader)
PICC	Proximity Integrated Circuit Card (Contactless card)
Q / Q-factor	Quality Factor
RF	Radiofrequency
TBD	To Be Defined
V	Voltage
Vpp	Peak to peak voltage

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10. List of figures

Fig 1.	Standard antenna example	4	Fig 32.	Fine tuning of CLIF_ANA_TX_AMPLITUDE_REG register in CARD mode	40
Fig 2.	Field distribution of a circular antenna with open air environment	5	Fig 33.	CLIF_ANA_TX_AMPLITUDE_REG register definition in listen mode	41
Fig 3.	Field distribution of a circular antenna with a metal plane	5	Fig 34.	Example of MinPowerLevel Results	42
Fig 4.	Field distribution of a circular antenna with a metal plane and a ferrite sheet	5	Fig 35.	Additional load switch at TX1/TX2	43
Fig 5.	Ferrite sheet overlay recommendation	6	Fig 36.	TX1 – TX2 impedance vs GSN register value	43
Fig 6.	PN7120 typical antenna matching circuit	7	Fig 37.	Pulse shape Type A in EMVCo	44
Fig 7.	Series equivalent circuit	8	Fig 38.	Pulse shape Type B in EMVCo	44
Fig 8.	Example of results for antenna characteristic circuit	10	Fig 39.	Fine tuning of CLIF_ANA_TX_AMPLITUDE_REG register	45
Fig 9.	Series equivalent resistance calculation	11	Fig 40.	CLIF_ANA_TX_AMPLITUDE_REG register definition in poll mode	46
Fig 10.	Parallel equivalent circuit	12	Fig 41.	Fine tuning of CLIF_ANA_RX_REG register	47
Fig 11.	Impedance transformation	13	Fig 42.	CLIF_ANA_RX_REG register definition	48
Fig 12.	Definition of transformation impedance Z_{tr}	14	Fig 43.	Fine tuning of CLIF_SIGPRO_RM_CONFIG1_REG register	50
Fig 13.	Typical Smith chart of the NFC antenna matching	15	Fig 44.	CLIF_SIGPRO_RM_CONFIG1_REG register definition	51
Fig 14.	PN7120 typical antenna matching circuit	16	Fig 45.	Fine tuning of CLIF_TRANSCEIVE_CONTROL_REG	52
Fig 15.	PN7120 RX connected to the EMC Filter	18	Fig 46.	CLIF_TRANSCEIVE_CONTROL_REG register definition	53
Fig 16.	PN7120 typical Rx signal measured at Rx input pin	19	Fig 47.	Fine tuning of CLIF_TX_OVERSHOOT_CONTROL_REG	53
Fig 17.	Measurement of the matching impedance	20	Fig 48.	CLIF_TX_OVERSHOOT_CONTROL_REG register definition	54
Fig 18.	Smith chart of the asymmetric Reader mode matching	21	Fig 49.	Fine tuning of CLIF_TX_UNDERSHOOT_CONTROL_REG	54
Fig 19.	Practical considerations (simplified view)	21	Fig 50.	CLIF_TX_UNDERSHOOT_CONTROL_REG register definition	54
Fig 20.	EMVCo POS operating volume requirement	24	Fig 51.	Fine tuning of CLIF_ANA_TX_SHAPE_CONTROL_REG	55
Fig 21.	NFC Forum operating volume	24	Fig 52.	Fig 37. CLIF_ANA_TX_SHAPE_CONTROL_REG register definition	55
Fig 22.	EMV -TEST PICC connected on DC OUT port	26	Fig 53.	40x40mm antenna drawing	57
Fig 23.	ISO/IEC 10373-6 Reference PICC Class 1	27			
Fig 24.	PICC Classes according to the ISO/IEC 14443	28			
Fig 25.	Setup to check the signal shaping	29			
Fig 26.	Pulse shape according to <i>ISO/IEC14443 [2]</i> , 106 kbps	30			
Fig 27.	Modulation Index (m) calculation in Reader/Writer mode	31			
Fig 28.	Card Emulation: EMVCo test bench typical measurement	33			
Fig 29.	CLIF NCI Structure	35			
Fig 30.	Transition ID - Simplified view	36			
Fig 31.	Example of CLIF register setting command	39			

11. List of tables

Table 1.	EMC Filter (typical values) and matching impedance target	15
Table 2.	CLIF_ANA_AGC_REG and expected maximum Rx voltage	19
Table 3.	Components characteristics.....	22
Table 4.	Pulse shapes definition according to <i>ISO/IEC14443[2]</i> , 106 kbps	31
Table 5.	Type B 106kbps criteria according to <i>ISO/IEC14443</i>	31
Table 6.	Load modulation HW for LMA test	34
Table 7.	Transition ID values	37
Table 8.	CLIF_ANA_RX_REG transitions.....	49
Table 9.	CLIF_SIGPRO_RM_CONFIG1_REG transitions.....	52
Table 10.	40x40mm Antenna outlines.....	57
Table 11.	40x40mm Antenna expected performances....	58
Table 12.	Recommended standard coil antenna physical characteristics	58

12. Contents

1.	Introduction	3	5.2.1.3	Reception check.....	32
2.	Antenna Design	4	5.2.2	Card mode measurements.....	33
2.1	Standard antenna design	4	5.2.2.1	Load modulation amplitude measurement.....	33
2.2	Shielding and environment impact	4	5.2.2.2	Reception test	34
2.2.1	Ferrite shielding recommendation	6	5.3	Fine tuning through registers.....	35
3.	PN7120 Antenna matching	7	5.3.1	Register setting command.....	35
3.1	Antenna matching circuit.....	7	5.3.2	Configuring load modulation in CARD mode....	40
3.2	Step 1: Antenna model measurement.....	8	5.3.2.1	CLIF_ANA_TX_AMPLITUDE_REG	40
3.2.1	Measurement method with impedance analyzer.....	9	5.3.3	Configuring pulse shape in poll mode	44
3.2.2	Measurement method with any network analyzer	9	5.3.3.1	CLIF_ANA_TX_AMPLITUDE_REG	45
3.2.3	Optional Quality factor adjustment	11	5.3.4	Optimizing Rx path in poll mode.....	47
3.2.4	Determination of the parallel equivalent circuit:	12	5.3.4.1	CLIF_ANA_RX_REG	47
3.3	Step 2: EMC filter design (L_0 and C_0 definition)	13	5.3.4.2	CLIF_SIGPRO_RM_CONFIG1_REG	50
3.4	Step 3: Reader mode matching (C_1 and C_2 definition).....	15	5.3.5	Configuring FDT	52
3.5	Step 4: Card mode tuning (C_2/C_{ANT} ratio definition).....	16	5.3.5.1	CLIF_TRANSCEIVE_CONTROL_REG.....	52
3.6	Step 5: Rx path tuning (R_{TX} & C_{RX} definition).....	18	5.3.6	Configuring TX control.....	53
4.	Matching verification	20	5.3.6.1	CLIF_TX_OVERSHOOT_CONTROL_REG	53
4.1	Step 1: verification of the Reader/Reader mode matching.....	20	5.3.6.2	CLIF_TX_UNDERSHOOT_CONTROL_REG	54
4.2	Step 2: verification of the CARD/listen mode frequency	22	5.3.6.3	CLIF_ANA_TX_SHAPE_CONTROL_REG	55
4.3	Components characteristics	22	6.	Reference design	57
5.	Performance verification and fine tuning	23	6.1.1	Antenna reference.....	57
5.1	Main specifications	23	6.1.2	Recommended characteristics	58
5.1.1	ISO/IEC 14443 specifics	23	7.	References	58
5.1.2	EMVCo specifics	23	8.	Abbreviations	59
5.1.3	NFC Forum specifics.....	24	9.	Legal information	60
5.2	Performance check against standards	25	9.1	Definitions.....	60
5.2.1	Reader Mode measurements.....	25	9.2	Disclaimers.....	60
5.2.1.1	Field strength measurement.....	25	9.3	Licenses	60
5.2.1.2	NFC Signal shaping verification	29	9.4	Trademarks	60
			10.	List of figures	61
			11.	List of tables	62
			12.	Contents	63

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