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TEA1892 GreenChip synchronous rectifier controller

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Document information

Info	Content
Keywords	GreenChip, TEA1892TS, TEA1892ATS, Synchronous Rectifier (SR) driver, high-efficiency
Abstract	The TEA1892TS is a member of the new generation of Synchronous Rectifier (SR) controllers for switched mode power supplies. Its high level of integration allows the design of cost-effective power supplies with a very low number of external components. The TEA1892TS is a controller IC dedicated to synchronous rectification on the secondary side of discontinuous conduction mode and quasi-resonant flyback converters. The dedicated TEA1892ATS version is available for resonant converters. The TEA1892 versions are fabricated using the Silicon-On-Insulator (SOI) process.

Revision history

Rev	Date	Description
v.1	20140409	first issue

Contact information

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1. Introduction

The TEA1892TS is a controller for Synchronous Rectification (SR) of quasi-resonant and Discontinuous Conduction Mode (DCM) flyback converters, which provides:

- Improved performance
- The capability to select two different set points for the regulation level

The TEA1892 is available in the following pin identical packages:

- TEA1892TS (TSOP6 package)
- TEA1892ATS (TSOP6 package)

The main difference between the TEA1892ATS and the TEA1892TS is the shorter minimum rectification time. This feature makes the TEA1892ATS ideal for higher switching frequencies (> 250 kHz) which are often used in DCM resonant converters.

Remark: Unless otherwise stated, all values are typical. Refer to the relevant product data sheet (Ref. 1, Ref. 2, Ref. 3) for more specific information.

1.1 Pinning information

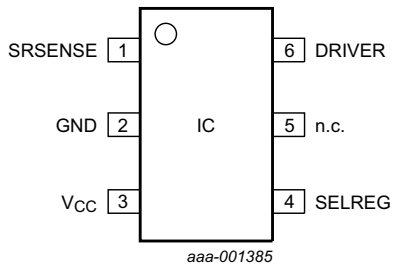

Fig 1. TEA1892TS/ATS (TSOP6) pin configuration

Table 1. TEA1892 pin description

Symbol	Pin	Description
SRENSE	1	synchronous timing input
GND	2	ground
VCC	3	supply voltage
SELREG	4	selection input for driver regulation level
n.c.	5	not connected
DRIVER	6	driver output for SR MOSFET

2. TEA1892TS application diagrams

The TEA1892TS is developed as a dedicated SR controller for flyback converters. The TEA1892ATS derivative is developed to provide support for synchronous rectification in resonant converters. The main difference between the two versions is the blanking time after turn-on.

2.1 TEA1892TS application for flyback converters

The application diagrams Figure 2 and Figure 3 show the configuration for high-side and low-side rectification. Both methods are valid for quasi-resonant and discontinuous conduction mode flyback converters using the TEA1892TS.

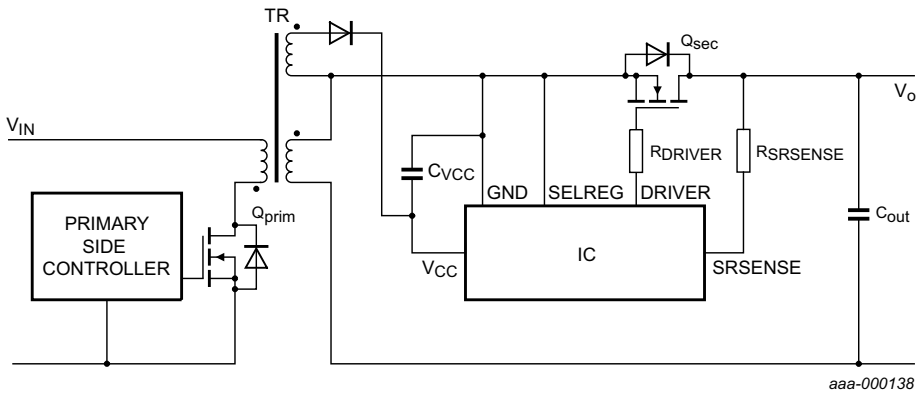

Fig 2. TEA1892TS application diagram for high-side rectification in flyback converters

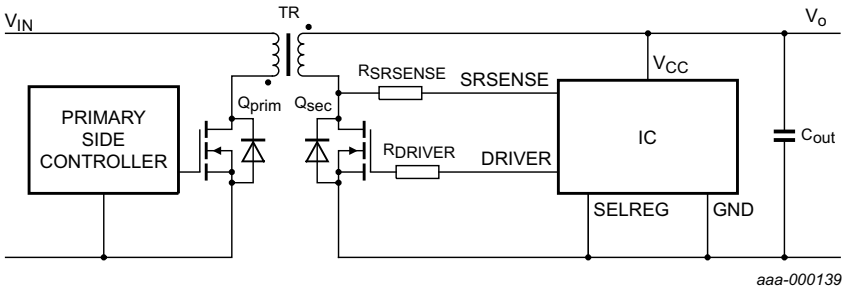

Fig 3. TEA1892TS application diagram for low-side rectification in flyback converters

Q_{prim} and Q_{sec} are the switches on the primary and secondary side. The primary controller manages Q_{prim} and the TEA1892 controller manages Q_{sec}. The TEA1892 controller operates independently of the primary controller.

2.2 TEA1892ATS application for resonant converters

Figure 4 shows the configuration for a resonant converter using the TEA1892ATS.

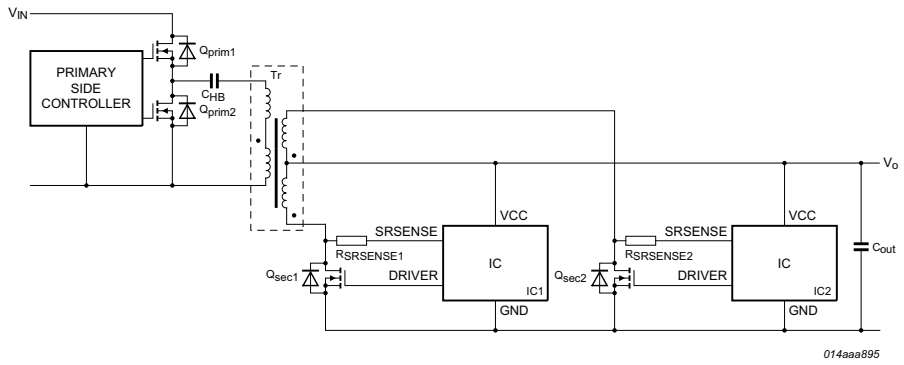

Fig 4. TEA1892ATS application for resonant converter

The TEA1892ATS is designed for Discontinuous Conduction Mode (DCM) adapters operating at higher switching frequencies. Resonant converters can also have higher frequency ranges (> 250 kHz). The smaller minimum rectification time of the TEA1892ATS (0.8 μs) ensures stable operation at switching frequencies > 250 kHz.

The TEA1892TS with a minimum rectification time of 1.5 μs is ideally suited for switching frequencies < 250 kHz.

3. Functional description and application overview

3.1 SR control

The TEA1892TS uses the SRSENSE pin as an input sense in the control of the drain-source voltage (V_{DS}) of the MOSFET. No adjustment is necessary in the SR control.

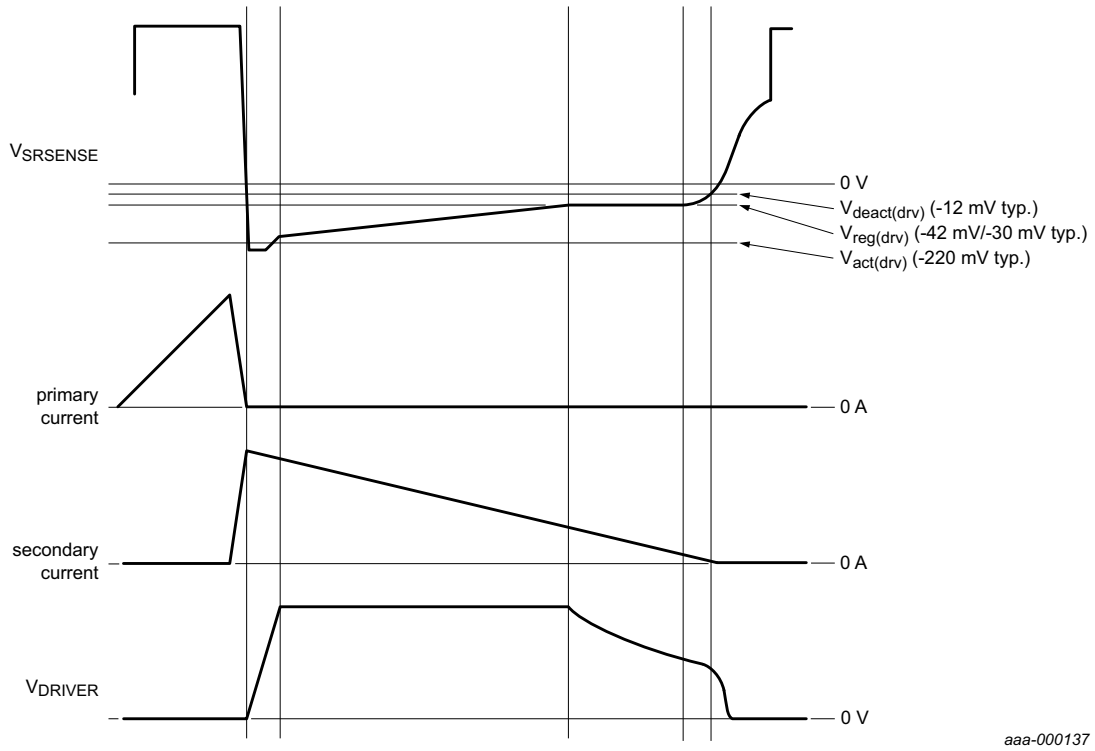

Fig 5. Synchronous rectification signals

The SR MOSFET is switched on by the DRIVER pin which is connected to the gate of the MOSFET. When the drain voltage on the SRSENSE pin is < −220 mV, the SR MOSFET is switched on. When the sensed voltage reaches −30 mV or −42 mV, the driver output voltage is regulated to maintain the sensed voltage on the SRSENSE pin. The regulation voltage level depends on the SELREG pin setting.

At a very low drain current with the $V_{SRSENSE}$ > −12 mV, the driver is pulled to ground and the SR MOSFET is switched off.

The TEA1892 does not switch off when the secondary stroke of the flyback converter is shorter than the minimum deactivation time, $t_{act(sr)(min)}$ (= 1.5 µs). Not switching off can improve the switching behavior and the efficiency at lower load ranges.

The best performance is obtained when the SRSENSE pin senses the drain of the SR MOSFET directly using the external 1 kΩ series resistor.

3.2 Function of resistors in series with the SRSENSE pin

All TEA1892TS pins are protected against ElectroStatic Discharge (ESD) to prevent IC damage when handled. Some application tests can trigger ESD protection.

If the ESD protection on the SRSENSE pin is triggered, the pin is pulled to ground by the internal ESD protection component. As the SRSENSE pin senses the MOSFET drain voltage, protect the pin using a series resistor to limit surge current from a severe ESD event. Figure 2, Figure 3 and Figure 4 show how the current limiting resistor $R_{SRSENSE}$ is used to provide the ESD surge protection. A 1 kΩ resistor value is sufficient to protect the SRSENSE pin.

Sometimes false triggering of the MOSFET can occur, for example, due to ringing or crosstalk due to the PCB layout. Increasing the $R_{SRSENSE}$ resistor value provides additional SR input filtering and improves performance. The drawback to this solution is increased activation and deactivation delay time values.

Remark: Check the application carefully to achieve the optimal configuration. More information on false triggering of the MOSFET including possible causes and solutions are described in Section 4.2.

3.3 V_{CC} supply

The $V_{CC(startup)}$ voltage is 8.5 V and the $V_{CC(stop)}$ voltage is 8 V. Normally, a 1 μF multilayer ceramic capacitor is placed between the V_{CC} and GND pins to smooth the supply voltage.

When the voltage on the V_{CC} pin is above 8.5 V, the IC leaves the UnderVoltage LockOut (UVLO) state and activates the synchronous rectifier circuitry. The UVLO state is triggered when V_{CC} < 8 V and the SR driver output is kept active-low.

3.4 V_{CC} auxiliary supply

In high-side rectification, the IC is supplied by an auxiliary winding which is tacked on to the secondary output winding. To get the full driver output capability, supply voltage V_{CC} must be > 12 V. A supply voltage of ±15 V is targeted which is set using the power output winding and the AUX winding turns ratio.

$$V_{CC} = \frac{N_{aux}}{N_{SEC}} \times V_{OUT} - 0.7\ V \quad (1)$$

The average IC supply current depends on the dynamic gate charge transfer characteristic of the MOSFET.

For example; conditions of 10 V gate-drive amplitude, V_{DS} of < 1 V, C_{GS} 75 nC and f_{sw} = 100 kHz results in a drive current of 7.5 mA. The IC only consumes 1 mA. So in this case, the total supply current adds up to 8.5 mA.

3.5 Driver output

The driver circuit to the external power MOSFET gate has a source capability of 400 mA and sink capability of 2.7 A. These capabilities ensure efficient operation, enabling fast switch-on and switch-off of the power MOSFET. The source stage is coupled to a 1.5 μs timer. When the timer finishes, the source capability is reduced to a 5 mA to maintain the driver output voltage at the required level.

The output voltage of the driver is limited to 10 V. The high-voltage output drives all MOSFET brands to the minimum on-state resistance R_{DSon}.

During start-up, the conditions $V_{CC} < V_{CC(startup)}$ and UVLO force the driver output voltage LOW to prevent false SR MOSFET switch-on.

Design a MOSFET gate series resistor into the track from the TEA1892 DRIVER pin to the SR MOSFET gate input. If this gate series resistor is required due to switching noise reduction, check the SR MOSFET switch-off state. Recheck the MOSFET at a high temperature as well.

When the power MOSFET on the primary side switches on, the drain-source voltage of the SR MOSFET rises with a high dV/dt. If the dV/dt is steep, the capacitive current flows from the drain to the gate through the MOSFET capacitor C_{DG}. The current and a gate resistor increases the gate voltage V_{GS}. However, the voltage increase must remain well below the SR MOSFET threshold voltage V_{th} to prevent switch-on. Therefore, limit the gate series resistor to between 4.7 Ω and 10 Ω.

3.6 SR level select

The driver regulation voltage level $V_{reg(drv)}$ is selected using the SELREG pin. When the SELREG pin is grounded, $V_{reg(drv)} = -42$ mV. When the SELREG pin is left open, $V_{reg(drv)} = -30$ mV.

The SELREG pin has a 10 μA internal pull-up current source. When the pin is short-circuited to ground, the pin selects the lowest $V_{reg(drv)}$ level. If the pin is left open, the current source creates a logic HIGH-level on this pin and the highest $V_{reg(drv)}$ value is selected.

As a guideline, set the SELREG level to the low value of −42 mV for MOSFETs with a high R_{DSon} of >10 mΩ. Conversely, use the high value of −30 mV for MOSFETs with a low R_{DSon} of <10 mΩ. The choice has a small benefit on the behavior in low load conditions. The low value is the preferred setting when false triggering occurs as a result of large crosstalk or high current spikes in high load conditions. Always check and compare both settings for each application.

4. Recommendations to improve the application

4.1 Layout considerations

To ensure the best possible results, pay careful attention to the PCB layout. Tracks from the MOSFET drain to the SRSENSE pin and from the MOSFET source to the GND pin form a loop. This loop must be as short as possible. Route them as close as possible and parallel to each other. This routing prevents incorrect measurement values from being obtained because of the voltage drop over the tracks.

The IC ground is used as reference by the internal circuits but it also shares the high driver output current pulses. In addition, IC ground is part of the very sensitive regulation control loop for the SR MOSFET.

The IC ground copper track must be as wide and as low ohmic as possible. Direct the IC ground track very close to the MOSFET source and position the IC near the MOSFET.

Connect the SRSENSE pin to the drain pin of the SR MOSFET using the series resistor. It is good practice to make the sense track a separate one to guarantee correct sense and regulation of the MOSFET V_{DS}.

4.2 False triggering

At the end of the blanking time, if the SRSENSE level is near to the regulation range level, a small disturbance can trigger the MOSFET to switch off. False triggering is most likely to happen when the following conditions are valid:

- low loads combined with a low R_{DSon} MOSFET and large secondary ringing
- high current spikes in the application as a result of poor PCB-layout in combination with a high frequency source such as PFC switching

There are several solutions to eliminating or decreasing false triggering and unwanted MOSFET switch-off:

- Check both levels of the regulation voltage with the SELREG pin open or connected to ground and select the setting with the best results
- Improve the PCB-layout of the application see Section 4.1)
- Use a general-purpose diode instead of a fast-diode in the primary RCD snubber network. This modification reduces the ringing at the beginning of the secondary stroke
- Connect a filtering capacitor (5 pF to 33 pF) from pins SRSENSE to GND close to the IC. Alternatively, increase the series resistor value in the SRSENSE line (see Section 3.2)
- Use a MOSFET with a higher R_{DSon}. A higher value of R_{DSon} contributes more margin for low load conditions. In general, MOSFETs with an R_{DSon} as low as 7 mΩ do not cause problems in a good design. MOSFETs with an R_{DSon} <7 mΩ only have a very limited contribution to higher efficiency because of the increased capacitive switching losses. In addition, they are more expensive and more sensitive to false triggering
- Create an offset on the SRSENSE input as shown in Figure 6. The offset also contributes to better performance of low R_{DSon} MOSFETs.

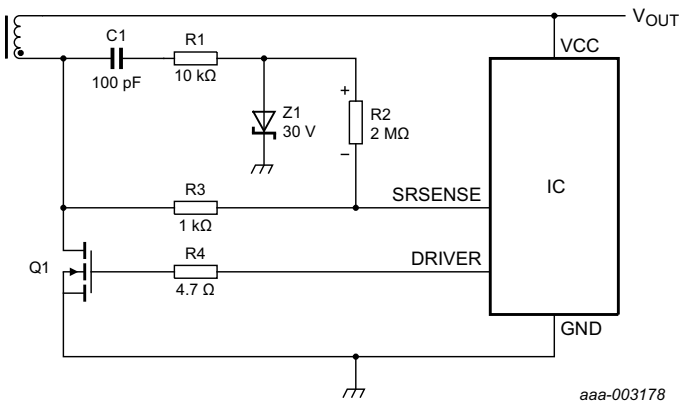

Fig 6. TEA1892 schematic offset circuit low-side application

The schematic shown in Figure 6 is drawn for a low-side application for ease of explanation. However, it is valid for high-side applications as well. The explanation of the circuit is based on the component values used in Figure 6.

The components C1, R1, R2 and Z1 are added to create an offset on the SRSENSE pin. They basically form a charge pump circuit that creates −30 V across Zener diode Z1. Resistor R1 limits the peak current through Z1. The −30 V creates a 15 μA current through resistors R2 and R3. This current lowers $V_{SRSENSE}$ by 15 mV. The −42 mV or −30 mV regulation level effectively becomes −27 mV or −15 mV. The −12 mV switch-off level is 3 mV on the drain of MOSFET Q1. Changing the value of R2 adjusts the offset.

Place resistors R1 and R2 close to the IC to avoid noise on the SRSENSE pin.

Remark: Evaluate the switch-off timing carefully. The MOSFET switches off later because the −12 mV switch-off level is also raised.

5. References

[1] **TEA1892TS data sheet** — GreenChip synchronous rectifier controller data sheet

[2] **TEA1892ATS data sheet** — GreenChip synchronous rectifier controller data sheet

[3] **UM10781 user manual** — TEA1892TS GreenChip synchronous rectifier controller add-on board

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