AN11499

Highly Linear FM LNA design with BFU580Q

Rev. 1 — 16 June 2014 | Application note

Document information

Info	Content
Keywords	BFU580Q, BFU580G, BFU5xx series, FM band
Abstract	This document describes an FM band LNA design implemented on BFU580Q/BFU590Q Starter kit
Ordering info	BFU580Q/BFU590Q Starter-kit OM7965, 12nc 9340 678 74598
Contact information	For more information, please visit: http://www.nxp.com

Revision history

Rev	Date	Description
1	20140616	First publication

1. Abstract

In this application note an FM band LNA design (low noise amplifier) using a BFU580Q transistor from NXP latest wideband transistor range is described. It shows the design, simulation and implementation phases. Together with measurement results, parameters measured over temperature are shown.
The application note (AN) can be a starting point for new design(s), and/or derivative designs.

2. Introduction

The BFU500 series transistor family is designed to meet the latest requirements on high frequency applications (up to approximately 2 GHz) such as communication, automotive and industrial equipment. As soon as fast, low noise analogue signal processing is required, combined with medium to high voltage swings the BFU500 series transistors are the perfect choice. Due to the high gain at low supply current those types can also be applied very well in battery powered equipment.
Compared to previous Philips / NXP transistor generations and competitor products, improvements on gain, noise and thermal properties are realized BFU500 series transistors are available in various packages.

The transistors are promoted with a full promotion package, called “starter kits” (one kit type per package-type). Those kits include two PCB’s (one with grounded emitter, one with emitter degeneration provision), RF connectors, transistors and simulation model parameters required to perform simulations. See the overview of available starter kits in the table below.

Table 1. Customer evaluation kits

	Basic type	Customer evaluation kits
1	BFU520W, BFU530W, BFU550W	OM7960, starter kit for transistors in SOT323 package
2	BFU520A, BFU530A, BFU550A	OM7961, starter kit for transistors in SOT23 package
3	BFU520, BFU530, BFU550	OM7962, starter kit for transistors in SOT143 package
4	BFU520X, BFU530X, BFU550X	OM7963, starter kit for transistors in SOT143X package
5	BFU520XR, BFU530XR, BFU550XR	OM7964, starter kit for transistors in SOT143XR package
6	BFU580Q, BFU590Q	OM7965, starter kit for transistors in SOT89 package
7	BFU580G, BFU590G	OM7966, starter kit for transistors in SOT223 package

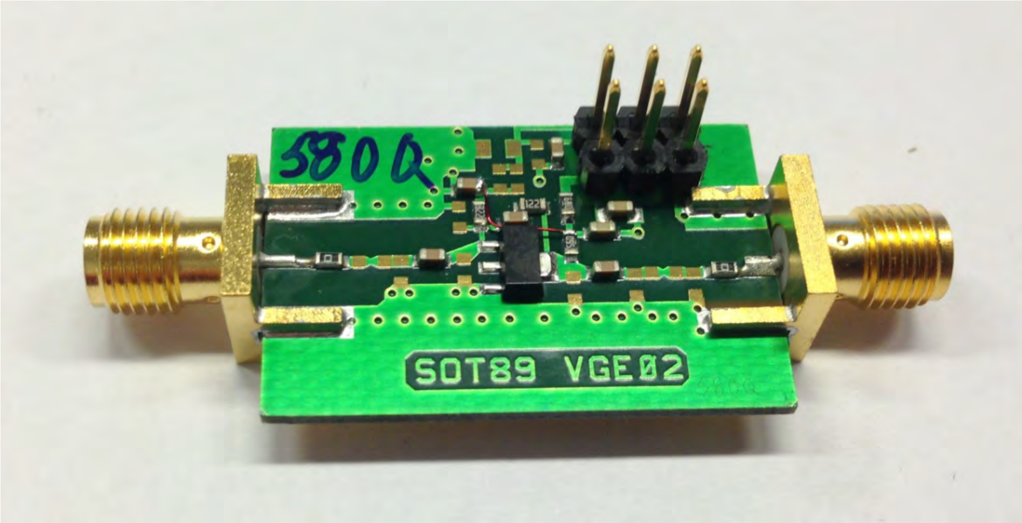


Fig 1. BFU580Q EVB picture

3. Requirements

The demonstrator circuit is designed to show the BFU580Q capabilities for a FM LNA with focus on Noise Figure and Linearity with supply current limited to maximum 25mA.
The aim of the demonstrator circuit was to design a LNA optimized for the FM band (88 MHz to 108 MHz) for automotive equipment meeting following requirements:

Supply Voltage:	5.0 Volts nominal
Supply current:	approx. 20 mA to 25mA (at ambient temperature)
Frequency range	88 MHz – 108 MHz
Noise Figure:	< 2dB
Gain:	approx. 20 dB
OIP3:	> +15dBm
Input Return-Loss:	> 10dB
Output Return-Loss:	> 10dB

The design is aimed at low BOM cost and small PCB area, inductors are SMD types (preferable low cost multilayer types) to enable simple tuning to other frequency bands.

As the design should be usable for automotive / car entertainment applications the behavior over temperature should be monitored.

4. Design considerations

In order to achieve low Noise Figure and reasonable Gain the source impedance has to be in between the optimum for Noise Figure and maximum Gain with given biasing current. As the required BW is approximately 20% of the Centre Frequency high Q matching circuits are not preferred (may lead to significant gain variations in the band).

The typical impedances in FM radio's for RF are 75 Ohms, as our demonstrator utilizes 50 Ohms transmission lines and connectivity two versions could be simulated.

At any time the circuit should be stable, hence during the design phase the stability factor needs to be observed carefully.

5. Design approach

The design starts in the simulation phase, applying the Mextram Model (available at http://www.nxp.com). Agilent "Advanced Design System" (ADS) was used for this but other simulation software packages should give equal results. Spice / Gummel Poon models are also available. In case simulations with S-parameter data have to be performed it is possible to download data from www.nxp.com. S-parameters data for various supply voltages and bias currents is available.

Once simulation results meet the requirements, the circuit is built on a universal Printed Circuit Board (PCB) and evaluated. If measurement results show significant offset from simulated results, fine tuning is required until required performance is met. To achieve better matching between simulations and measurements, the PCB parasitic properties were added in the simulation template.

Following blocks of passive components can be identified:
1) resistors for DC biasing
2) passives set up collector load
3) passives for output matching
4) passives for input matching
5) passives required to ensure stable operation

5.1 Simulation steps

Following simulation / design approach can be useful:

1) Configure the DC bias set-up, ensuring the Icc is set around desired value.
2) Configure the collector load circuit and output matching circuitry, optimizing the output Return Loss (RL).
3) Check stability.
4) Configure the input matching, for LNA optimize for minimum noise figure (NF) but keep close to optimum gain, if possible optimum NF gain points should be close.
5) Check stability.

Assumptions:

- Realistic passives are used by applying Murata design kit (0805 / 0603)
- PCB tracks represented by strip-lines

5.2 Implementation / evaluation steps

Following implementation / evaluation steps have been executed:

1) Implement simulated design on universal PCB.
2) Evaluate LNA on Gain / NF / matching / Stability at ambient temperature.
3) Fine tune passives if required.
4) In case significant differences between simulations and measured results are observed, try to modify parasitic properties in the simulation template.
5) Measure LNA design on RF parameters over temperature.

5.3 Setting up the DC bias circuit

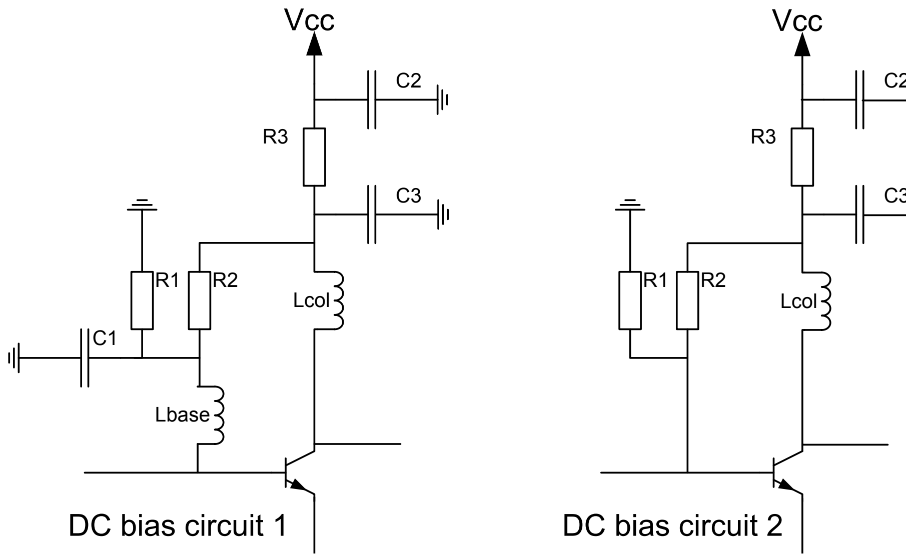


Fig 2. Circuitry to set DC bias current

Circuit 1 has the advantage that resistive noise from the resistors R1 and R2 is suppressed by capacitor C1, but at the cost of an extra inductor. This inductor can be part of the input matching.

Circuit 2 is commonly used and saves two passive components. Both circuits tend to have increasing collector current (Icc) with increasing temperature, partly stabilized by R3. Increasing R3 will degrade the linearity as it lowers the Vc.

5.4 Described design versions

Table 2. Different versions simulated

Version:	1	2	3	3 applying input match
Typical Zin/Zout	75Ω	50Ω	75Ω	75Ω
Feedback	No	Yes	Yes	Yes
Selectivity	Medium	Small	Medium	Small
Built/tested	No	Yes	No	No

5.5 Version 1, 75 Ohms selective LNA

The configuration used and simulation display is shown below (ADS).

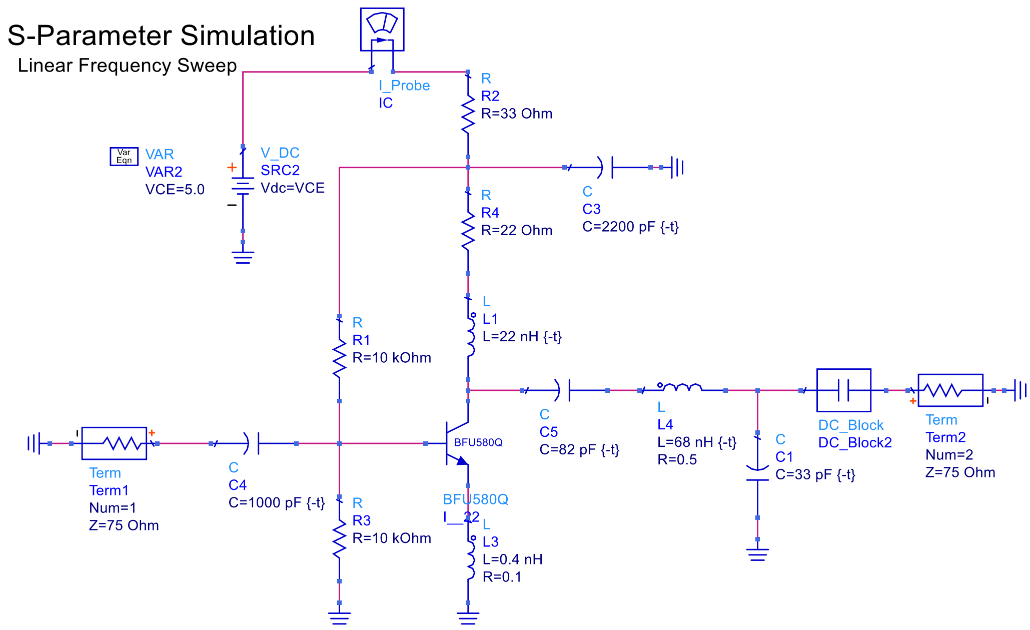


Fig 3. FM LNA version 1, applied ADS schematic

This is the schematic applied for S-parameter simulations. At the input there are no additional matching components used, still the input return loss reaches levels >10 dB.
The components L1, L4, C1 are tuned to get good match/gain match in the required frequency band.
Inductor L3 represents the parasitic inductance in the emitter path to ground (PCB related).

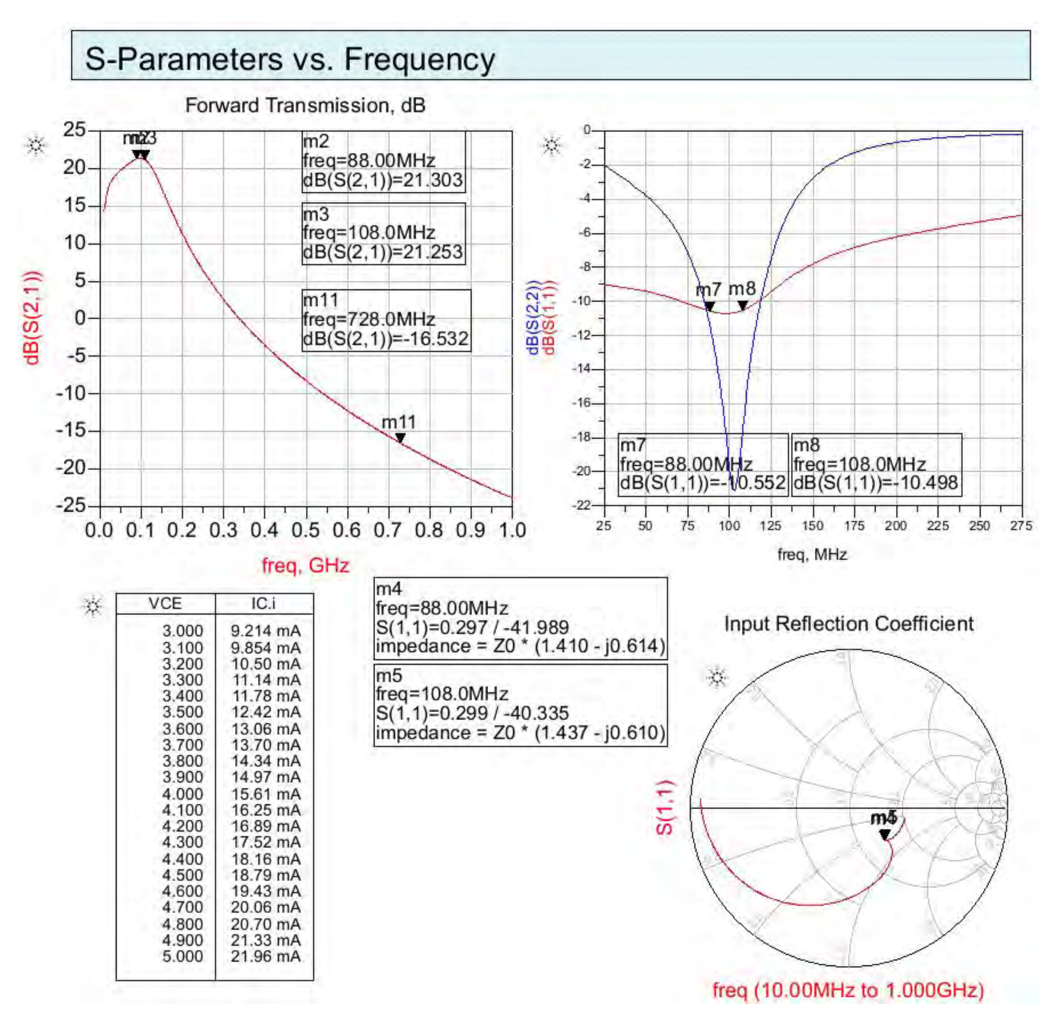


Fig 4. Version 1 S-parameter simulation results

The gain is above 20dB. There is a steep roll off for higher frequencies which can be advantageous in case large signals outside the FM band have to be suppressed. For example the suppression of the lowest LTE band (728 MHz) is 37 dB.

At 5.0 Volts supply the simulated supply current is 22mA. Also note that there are no additional matching components used at the input. The input-return-loss as well as the output-return-loss is more than 10dB.

Simulating the Noise and Gain behavior gives the results as shown in figure 5.

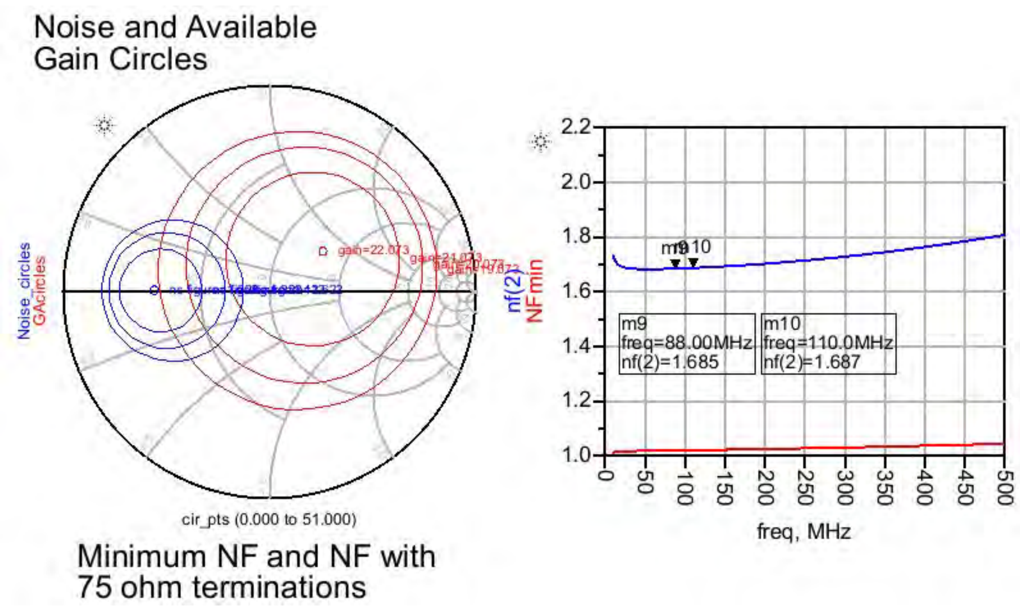


Fig 5. Version 1, Noise Figure, Noise circles

For better Noise Figure an additional network that matches the source towards the optimum (lower than 75 Ohms) could be used, however simulations show that this significantly degrades the input matching.

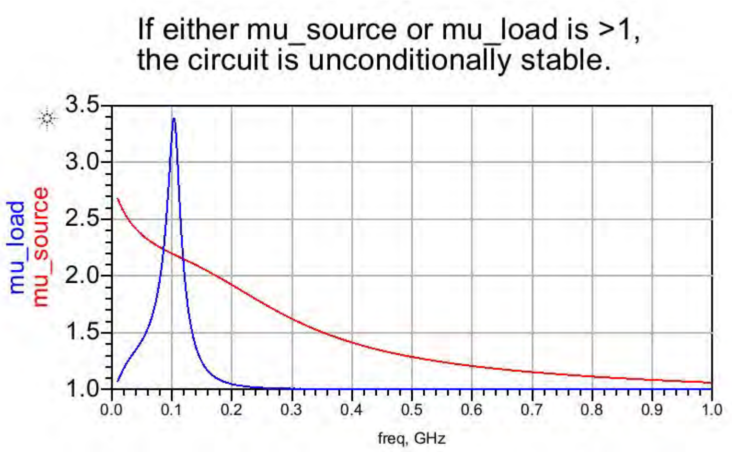


Fig 6. Version 1, Stability figures

5.5.1 Version 1, linearity simulations

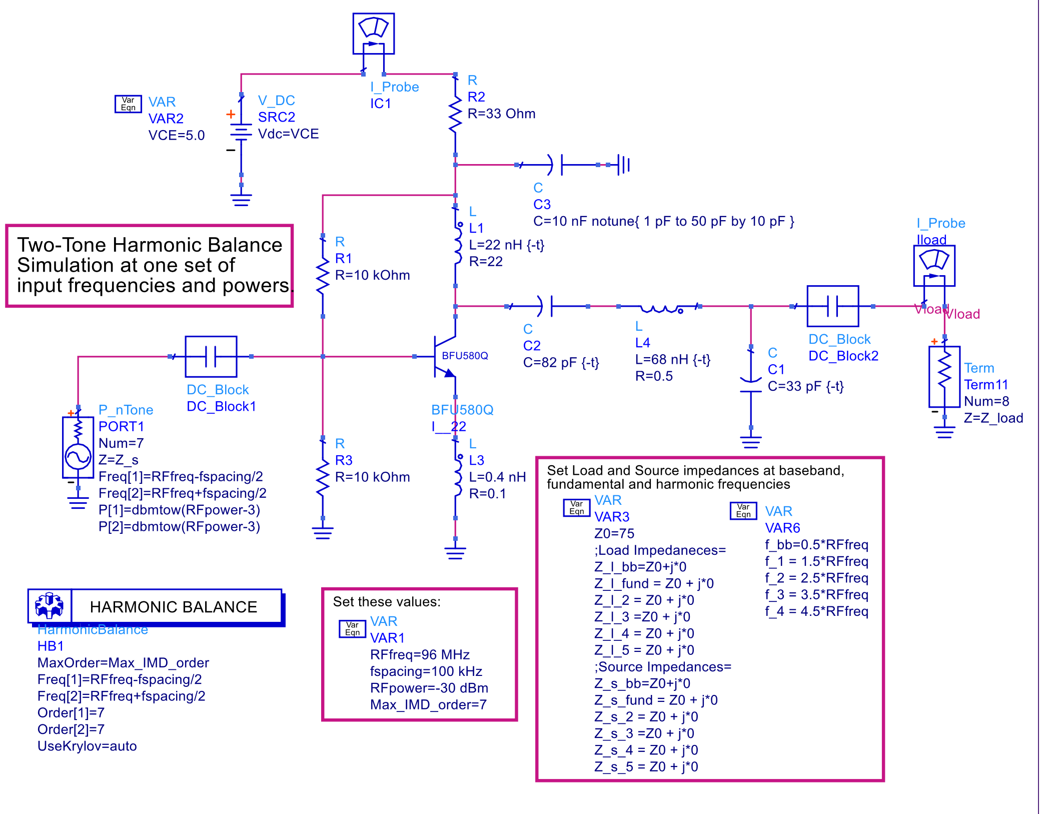


Fig 7. ADS simulation set-up for IP3

A harmonic balance simulation template is used, spacing applied was 100 kHz.

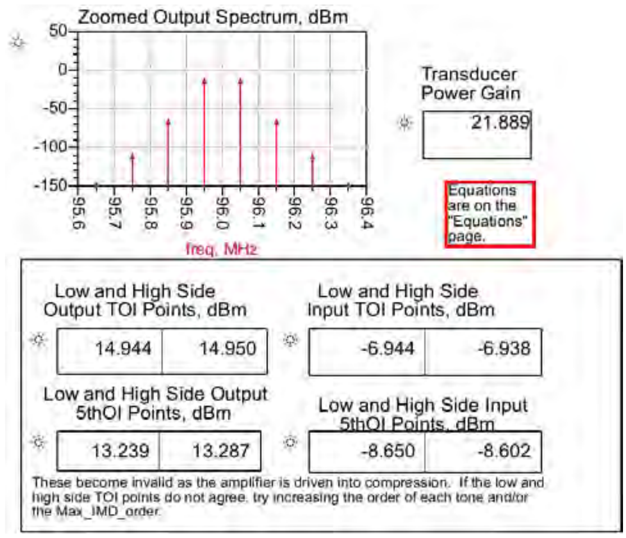


Fig 8. Version 1 IP3 simulation results

5.5.2 Summary / conclusions on version 1

This version has some selectivity (approx 37 dB damping for lowest LTE band). To ensure the proper frequency band, an evaluation on the spread of used components and PCB tolerances have to be performed (i.e. Monte Carlo). The NF is approx 1.7 dB with a good input return-loss. The NF could be improved at the cost of the input reflection coefficient.

5.6 Version 2, 50 Ohms LNA, applying feedback

The configuration used and simulation display is shown below (ADS).

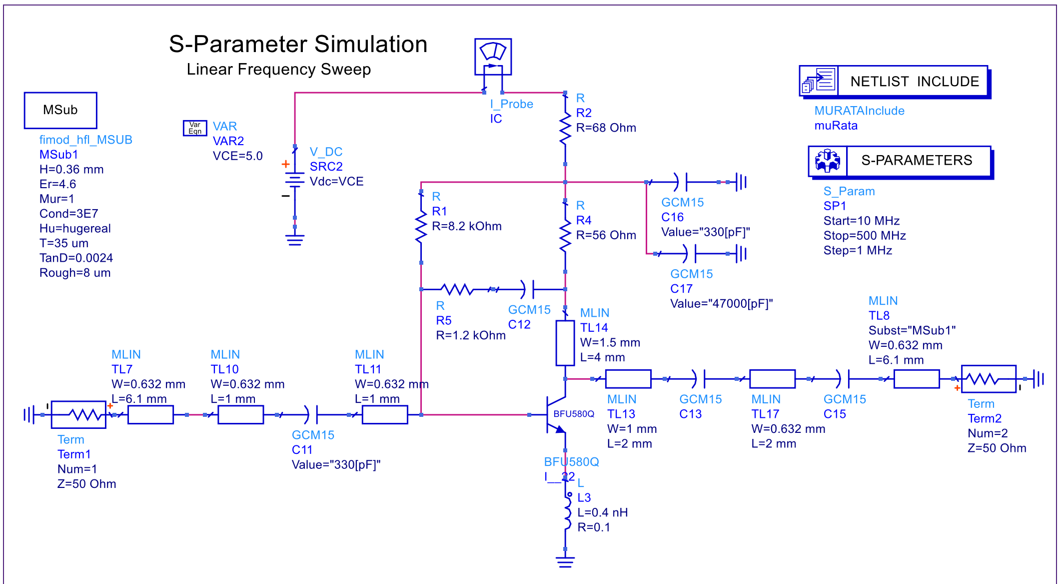
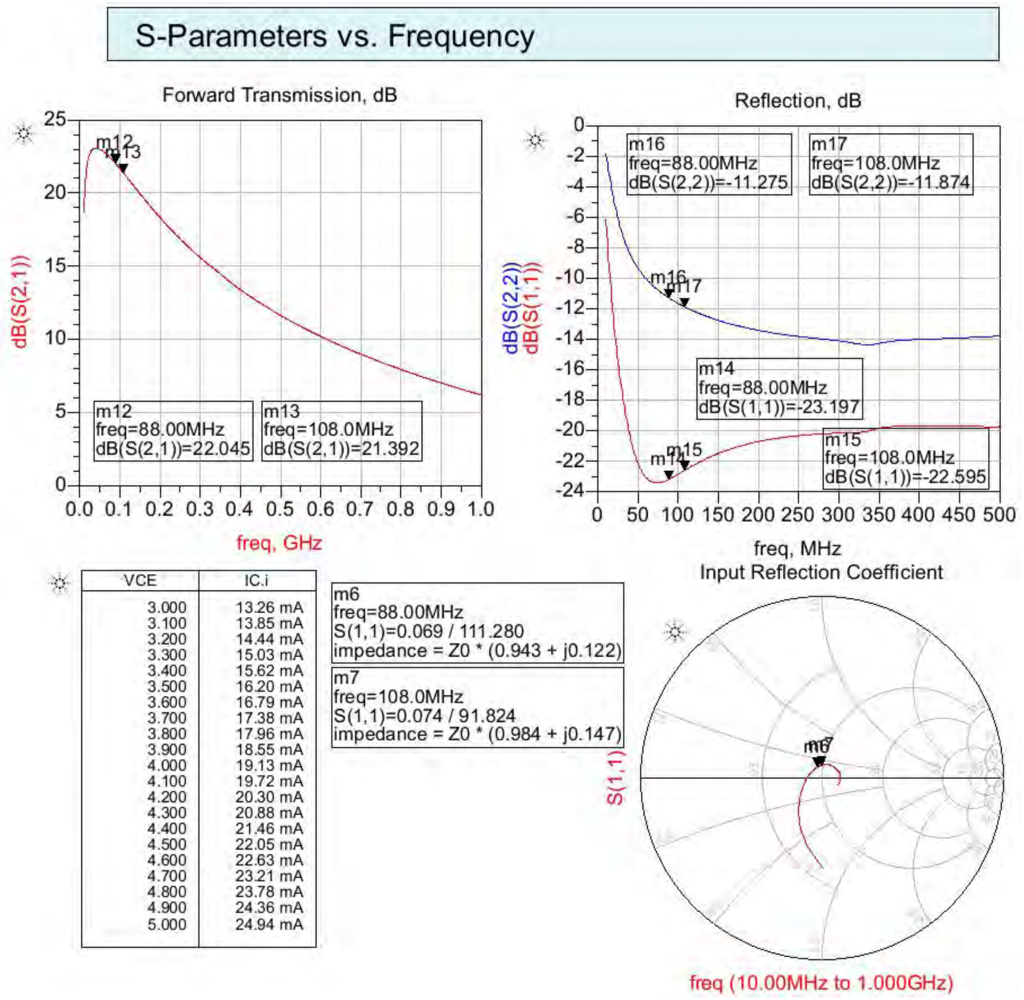


Fig 9. FM LNA version 2, applied ADS schematic

This is the schematic applied for S-parameter simulations. At the input there are no additional matching components used, still the input reflection reaches levels < -10 dB.

The components R5, C12 are used to generate feedback. The micro-strip lines used represent the copper patterns of applied PCB.



VCE	IC.i
3.000	13.26 mA
3.100	13.85 mA
3.200	14.44 mA
3.300	15.03 mA
3.400	15.62 mA
3.500	16.20 mA
3.600	16.79 mA
3.700	17.38 mA
3.800	17.96 mA
3.900	18.55 mA
4.000	19.13 mA
4.100	19.72 mA
4.200	20.30 mA
4.300	20.88 mA
4.400	21.46 mA
4.500	22.05 mA
4.600	22.63 mA
4.700	23.21 mA
4.800	23.78 mA
4.900	24.36 mA
5.000	24.94 mA

Fig 10. Version 2 S-parameter simulation results

The gain is above 20dB. At 5.0 Volts supply the simulated supply current is 25mA. Also note that there are no additional matching components used at the input. The input-return-loss is more than 10dB, the output-return-loss >20dB.

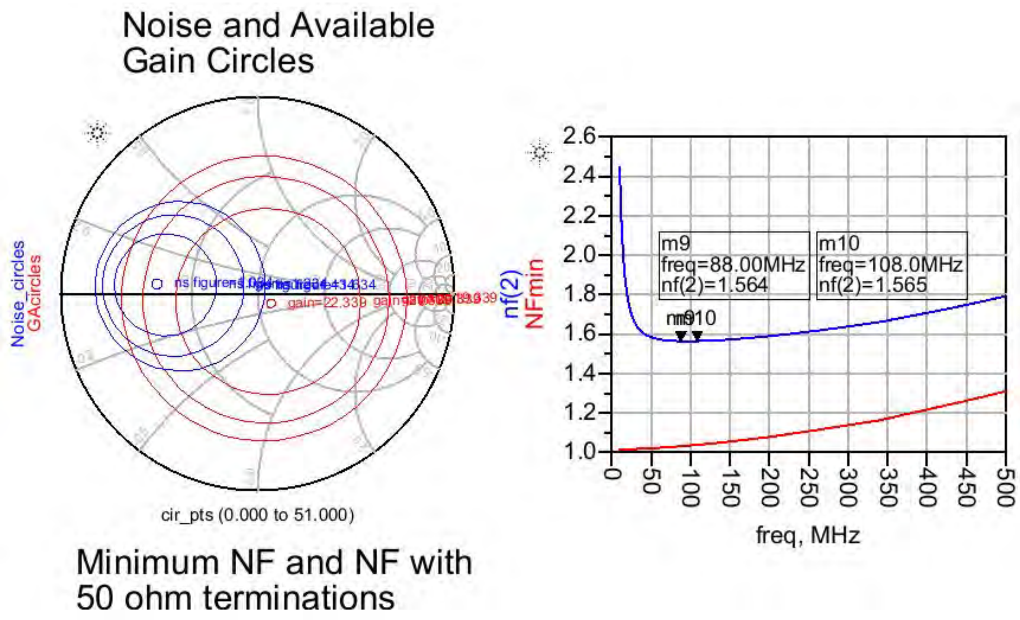


Fig 11. Version 2, Noise Figure, Noise circles

For better Noise Figure an additional network that matches the source towards the optimum could be used, however simulations show that this significantly degrades the input matching.

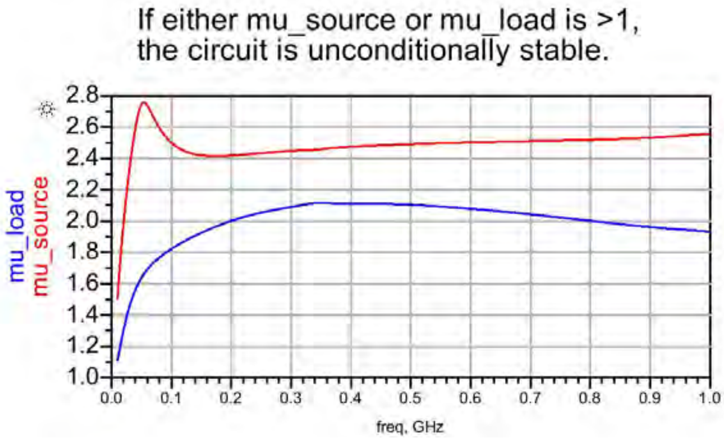


Fig 12. Version 2, Stability figures

5.6.1 Version 2, linearity simulations

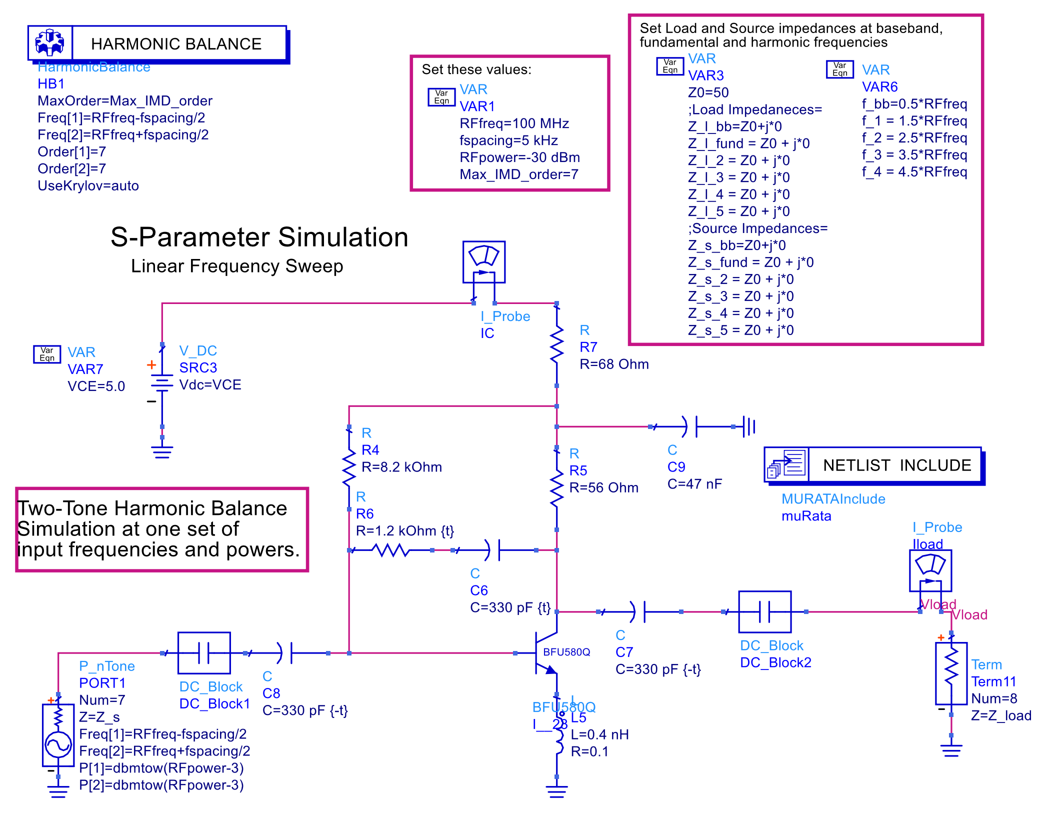


Fig 13. ADS simulation set-up for IP3

A harmonic balance simulation template is used, spacing applied was 5 kHz.

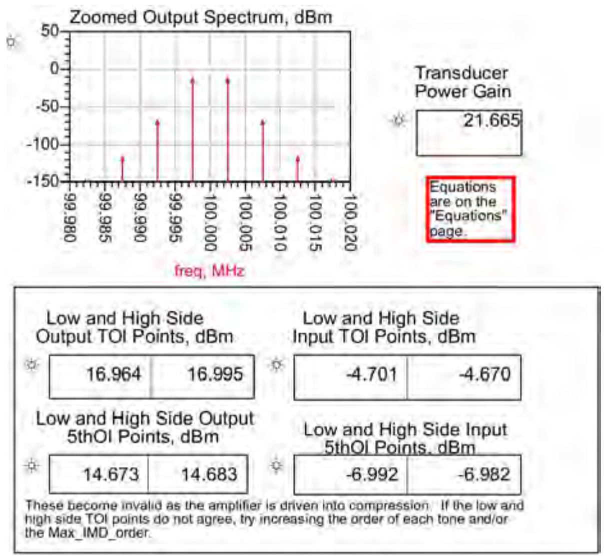


Fig 14. Version 2 IP3 simulation results

5.6.2 Summary / conclusions on version 2

This version 2 has price advantages compared to version 1, as the required passives are only resistors and capacitors. The NF is approx 1.6 dB with a good input return-loss. The NF could be improved at the cost of the input reflection coefficient.

The version 2 is implemented on the universal PCB, as delivered in the starter-kit. This PCB is equipped with SMA (50 Ohms) connectors.

A similar 75 Ohms version, called version 3, applying feedback is designed in ADS. Results are shown in sections 5.7.

5.7 Version 3, 75 Ohms LNA, applying feedback

The configuration used and simulation display is shown below (ADS).

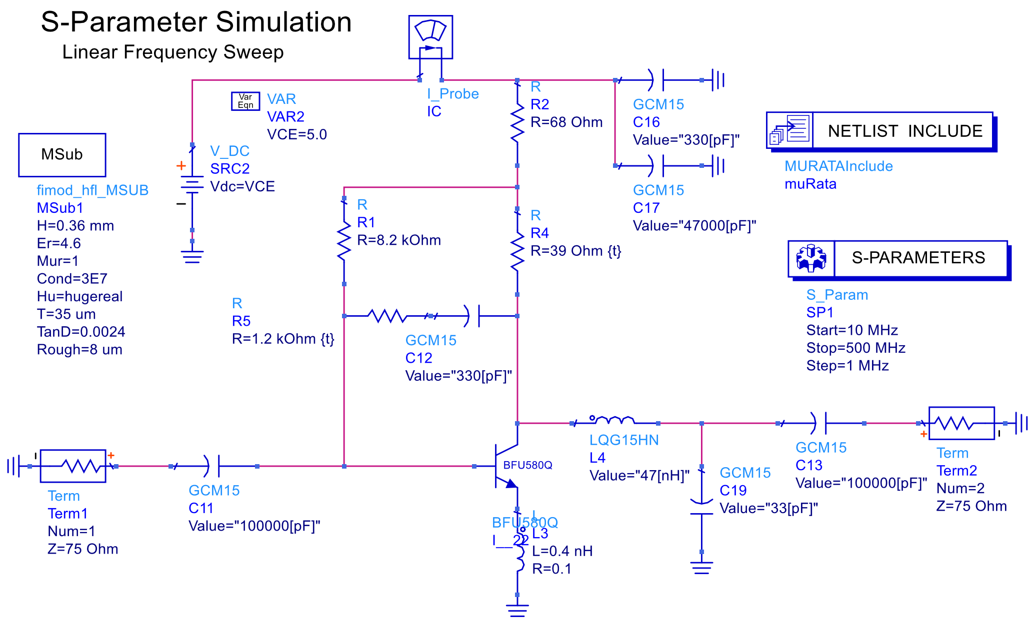


Fig 15. FM LNA version 3, applied ADS schematic

This is the schematic applied for S-parameter simulations. At the input there are no additional matching components used, still the input return loss reaches levels >10 dB.
The components R5/C12 are used to generate feedback, components.L4/C19 are used to match the output.

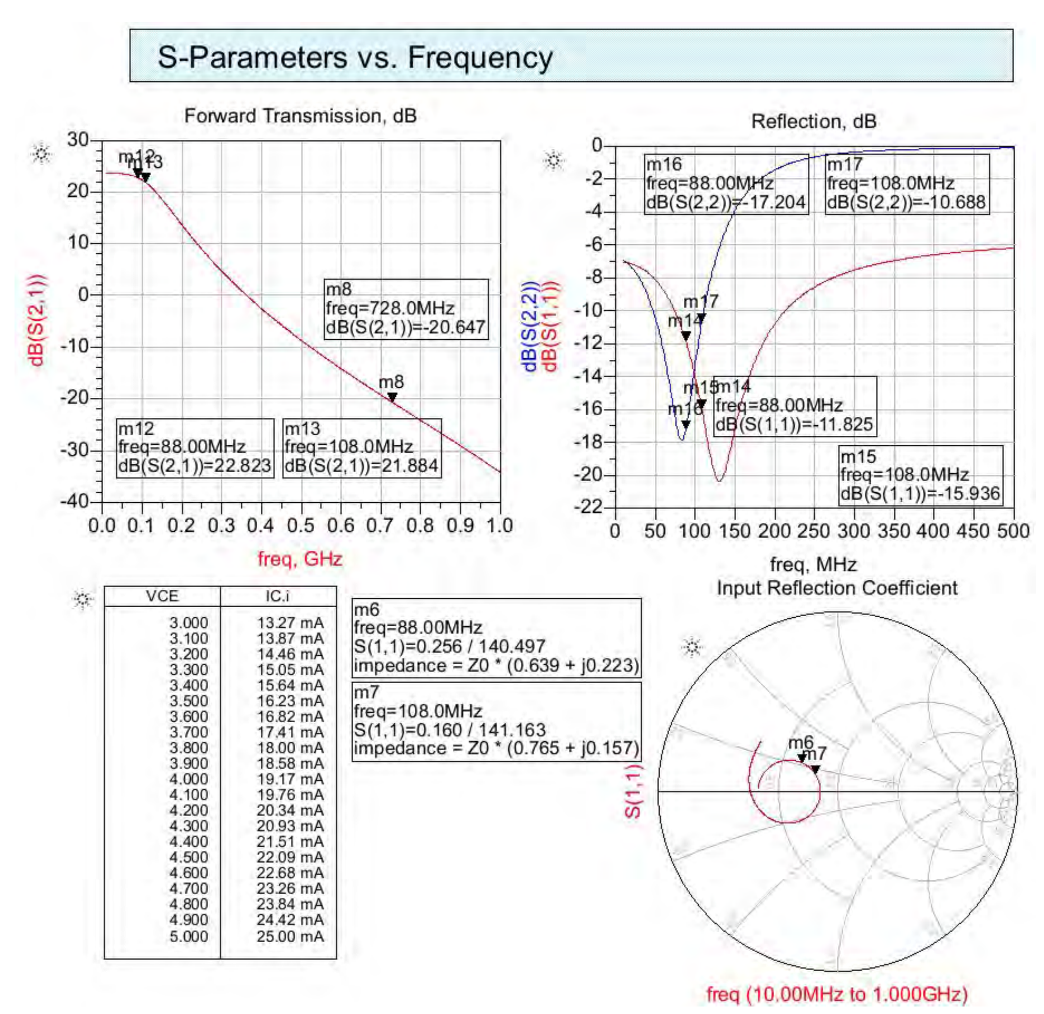


Fig 16. Version 3 S-parameter simulation results

The gain is above 20dB, at 5.0 Volts supply the simulated supply current is 25mA. Due to the additional output matching section (L4, C19) there is more rejection, compared to version 2, for frequencies above the FM band. As an example marker 8 is shown at a lower LTE band.

Simulating the Noise and Gain behavior gives the results as shown in figure 17.

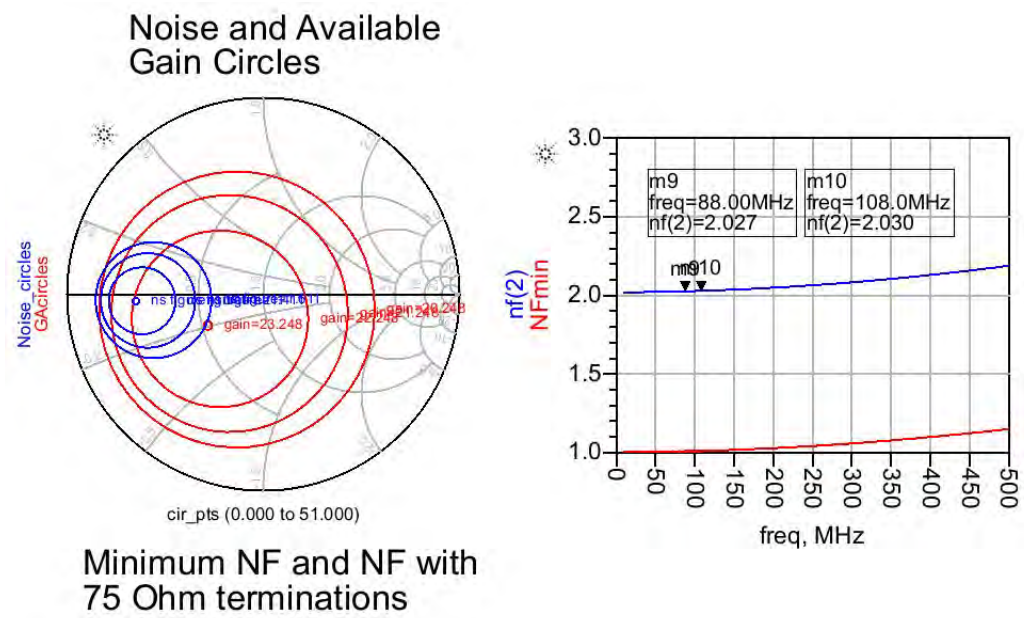


Fig 17. Version 3, Noise Figure, Noise circles

For better Noise Figure an additional network that matches the source towards the optimum could be used, but this will most likely degrade the input matching performance..

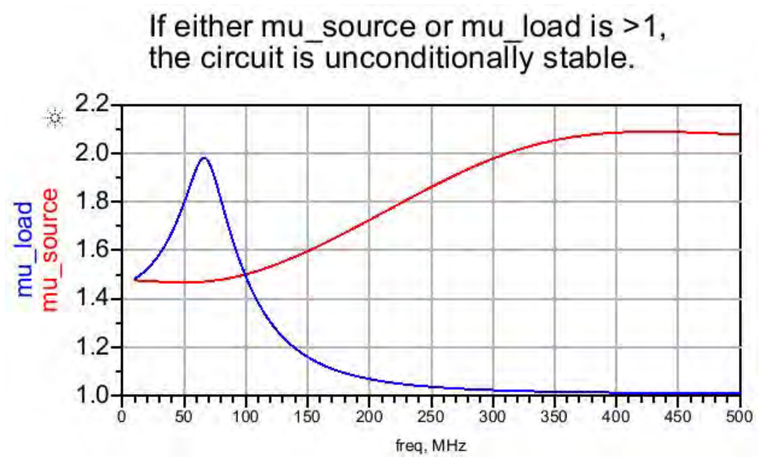


Fig 18. Version 3, Stability figures

5.7.1 Version 3, linearity simulations

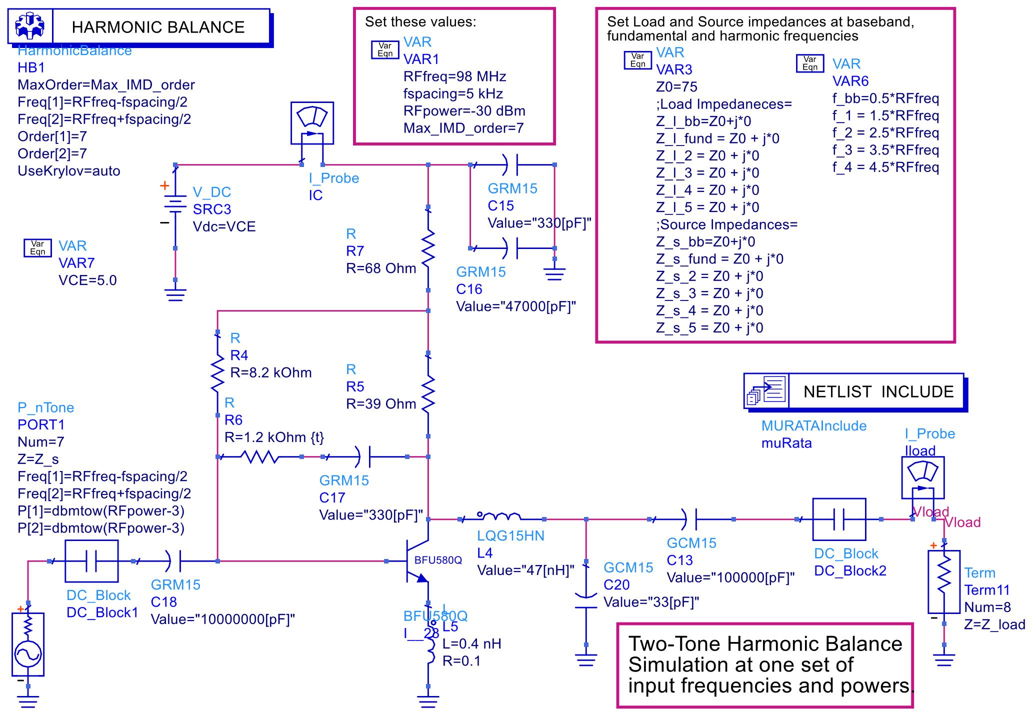


Fig 19. ADS simulation set-up for IP3

A harmonic balance simulation template is used, spacing applied was 5 kHz.

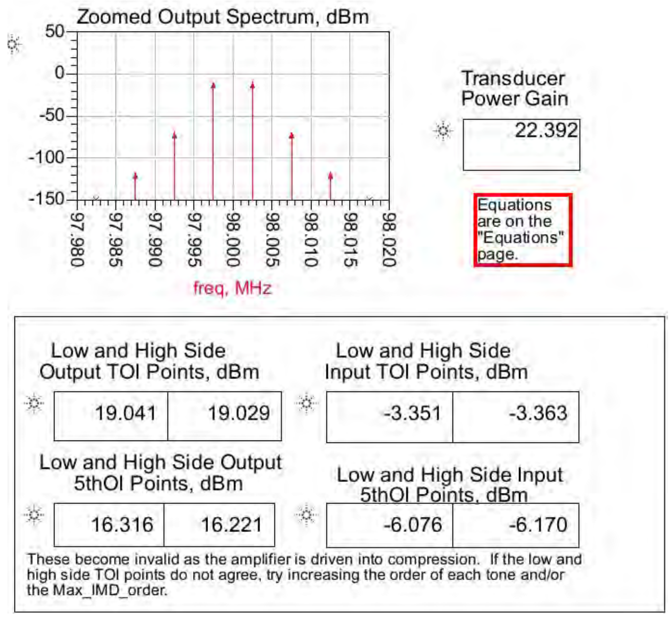


Fig 20. IP3 simulation results

5.7.2 Optimizing version 3 for best Noise Figure

By applying an input match that creates source impedance close to the optimum for Noise Figure, we could optimize the design for Noise Figure, with a possible trade-off for other parameters. The optimum source impedance can be seen in figure 17 and has to be smaller than 75Ω with imaginary part close to zero. The figure below shows the input configuration used that tunes the source impedance towards the optimum for lowest noise figure (components used for tuning are L5 and C20).

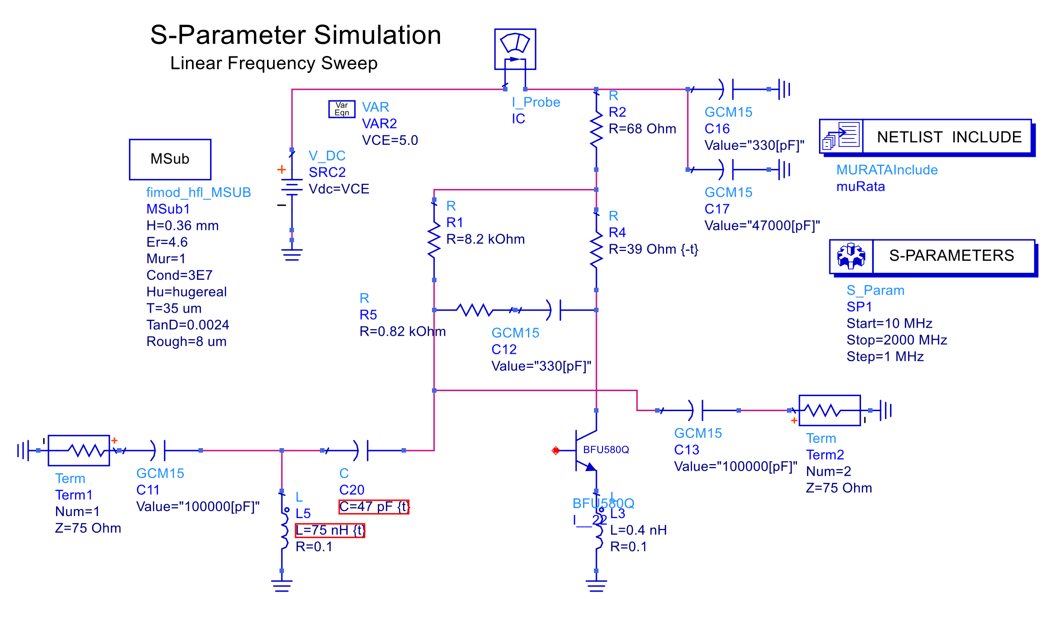


Fig 21. ADS simulation schematic for source matching

In the figure below the simulated source impedance is shown.

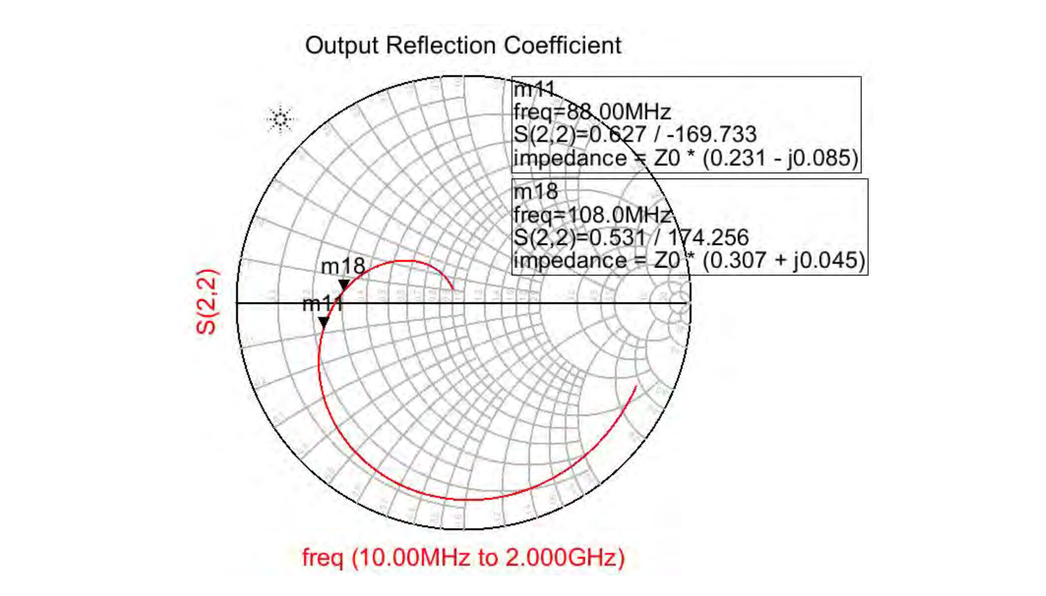


Fig 22. Simulated source impedance for input matched version 3

When simulating the LNA including the input network for noise we get the plot as shown below:

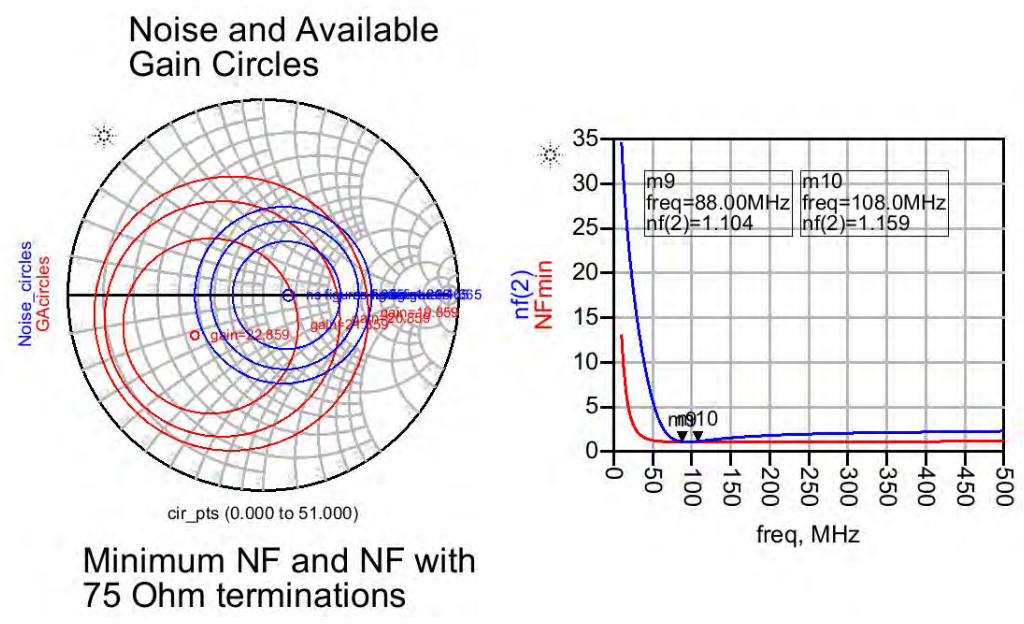


Fig 23. Simulated Noise Figure for input matched version 3

Now clearly the optimum for noise has moved towards the ideal 75Ω point and the optimum for gain is also not too far off. Simulated Noise Figure is now 1.1 to 1.2 dB. Simulated S-parameters are show in the next graph.

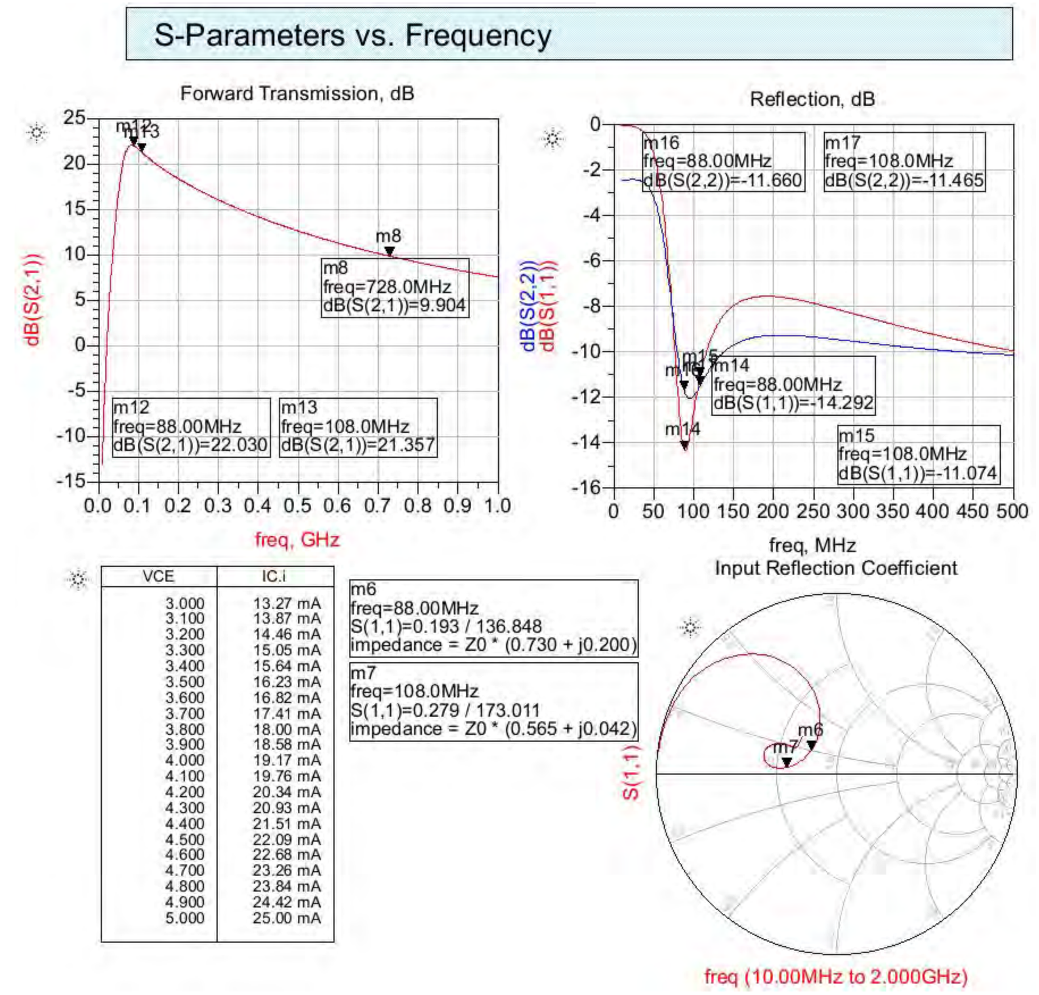


Fig 24. Simulated S-pars for input matched version 3

The gain is comparable with previous version. The output matching can be considered as moderate, to obtain that the matching network at the output was removed.

The linearity simulations showed almost equal behavior as the version without input matching, OIP3 simulated is18.9dBm.

5.7.3 Summary / conclusions on version 3

For this design the 50Ω version (version 2) is taken as starting point, a conversion to 75Ω is simulated. The version with source matching is best for lowest Noise Figure (approx. 1.2dB), the version with output matching has more rejection for “out of band” frequencies (i.e. LTE bands) but Noise Figure is almost 1dB higher. For linearity both versions show equal performance.

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6. Implementation on starter-kit

The circuit diagram of the evaluation board that was build and evaluated over temperature is shown in figure 25. Version 2, as described in sections 5.6, was used.

6.1 BFU580Q FM LNA schematic

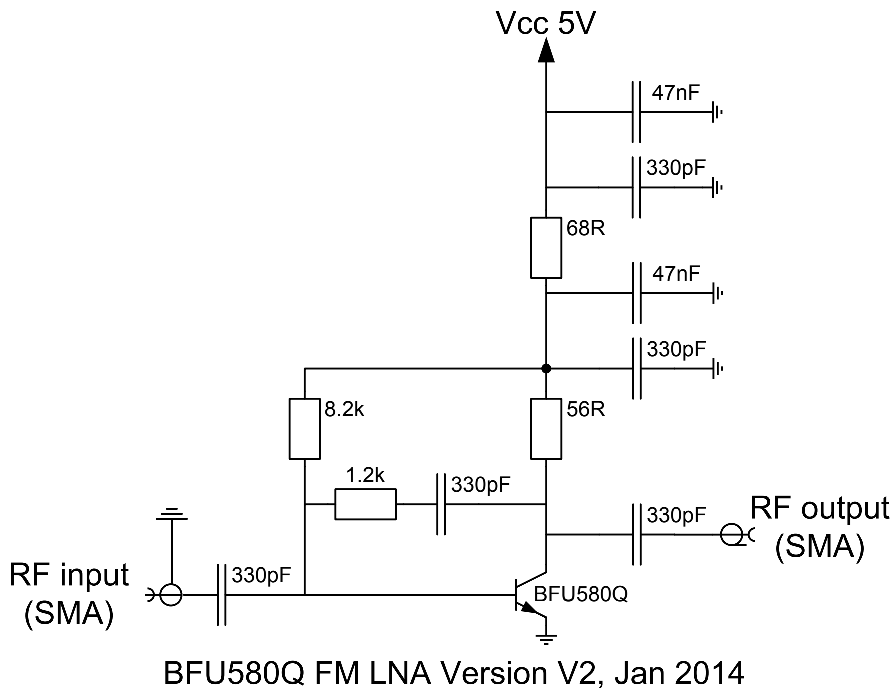

Fig 25. Schematic for measured LNA version

The PCB layout used for our internal evaluations did not accommodate the DC feed after the 68Ω resistor towards the 56Ω collector resistor, so a piece of wire was manually placed as show in the PCB drawing in figure 23.

Please note that not-used components (0R or jumpers that are present on the PCB design to allow different input configurations) in series with the signal path at the LNA input might cause additional input loss that adds to the Noise Figure.

6.2 BFU580Q FM LNA, PCB drawing

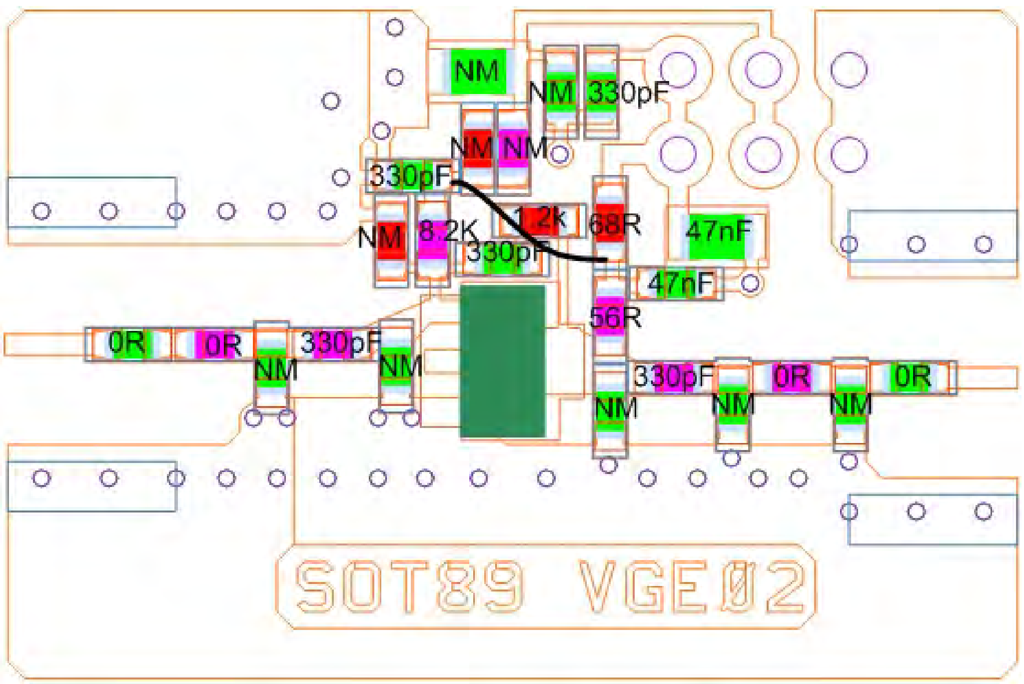

Fig 26. PCB and component placement for evaluated version

Remarks:
0R = SMD jumper, NM = not mounted
NM = component not mounted.

A connection from point A to B has to be made for the Collector Bias as shown.

6.1 PCB properties, layer stack

Fig 27. PCB layers used for Evaluation Boards in Starter kit

6.1 Typical LNA evaluation board results

Table 3. Typical results measured on the evaluation boards

Operating Frequency is f = 98 MHz unless otherwise specified; Temp = 25 °C

Parameter	Symbol	EVB	Unit	Remarks
Supply Voltage	V_{CC}	5.0	V	
Supply Current	I_{CC}	25	mA	
Noise Figure	NF	1.6	dB	
Power Gain	G_p	22	dB	
Input Return Loss	RL_{in}	-15	dB	
Output Return Loss	RL_{out}	-11	dB	
Output third order intercept point	OIP3	+15	dBm	

Table 4. Bill Of Materials

Value	Description	Footprint	Manufacturer
BFU580Q	Transistor	SOT89	NXP Semiconductors
330 pF	Capacitor	0603	Various
330 pF	Capacitor	0603	Various
330 pF	Capacitor	0603	Various
330 pF	Capacitor	0603	Various
330 pF	Capacitor	0603	Various
47 nF	Capacitor	0603	Various
47 nF	Capacitor	0603	Various
56 Ω	Resistor	0603	Various
68 Ω	Resistor	0603	Various
1.2 kΩ	Resistor	0603	Various
8.2 kΩ	Resistor	0603	Various

6.2 Simulation versus measured results

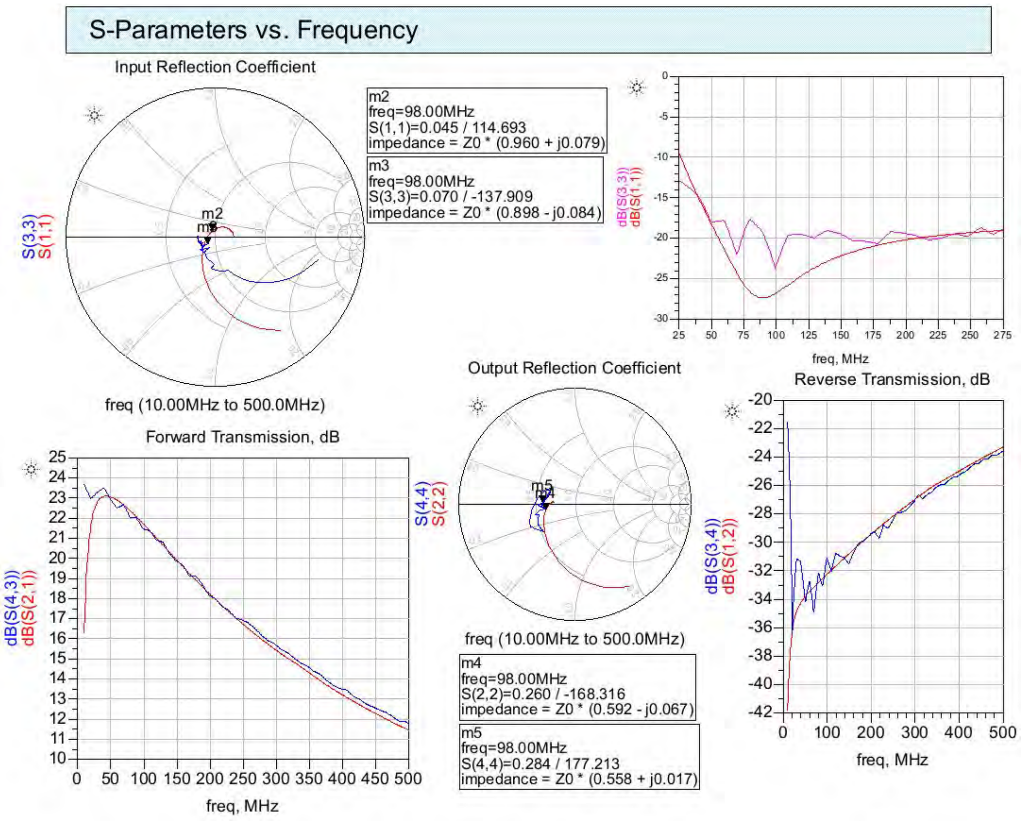

Fig 28. Version 2, measured versus simulated S-pars

7. Characterization of LNA over temperature and supply voltage

7.1 Gain (S21) = f (freq)

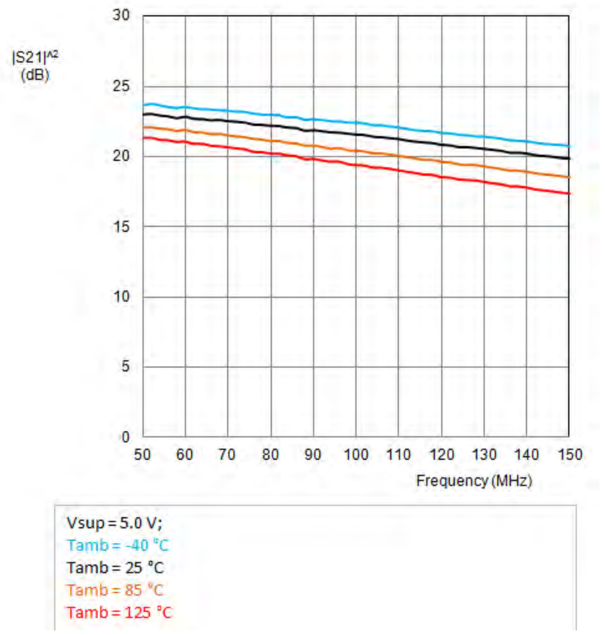

Fig 29. Measured S21 over frequency for different temperatures

7.2 Input return-loss (S11) = f (freq)

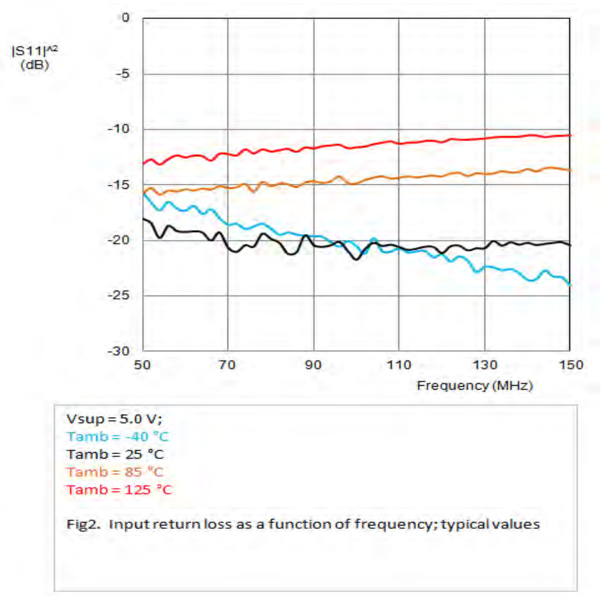

Fig 30. Measured S11 over frequency for different temperatures

7.3 Output return-loss (S22) = f (freq)

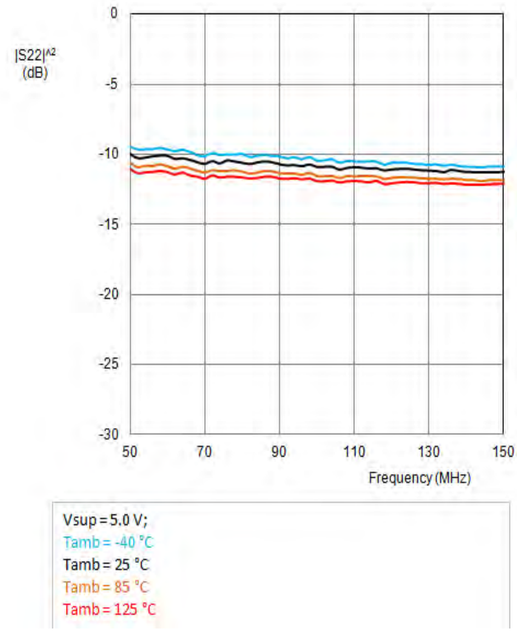

Fig 31. Measured S22 over frequency for different temperatures

7.4 Isolation (S12) = f (freq)

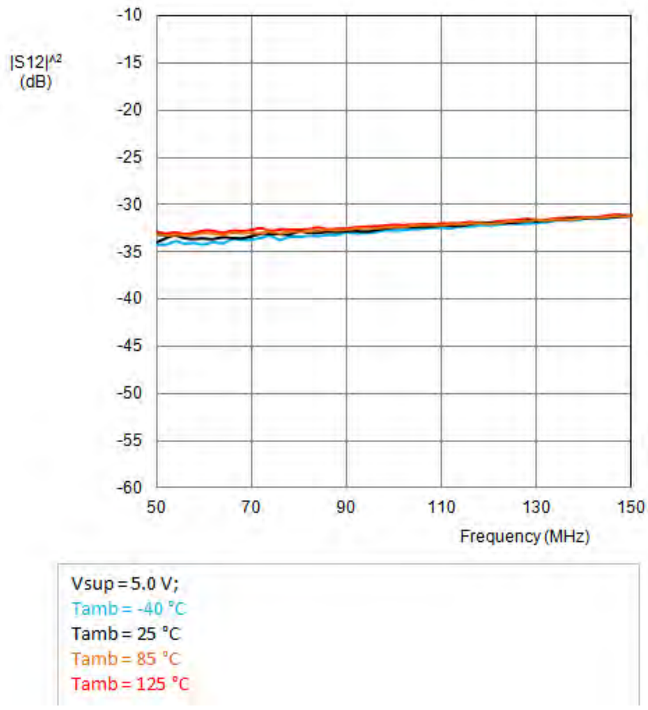

Fig 32. Measured S12 over frequency for different temperatures

7.5 Output third-order intercept point (OIP3) = f (Tamb)

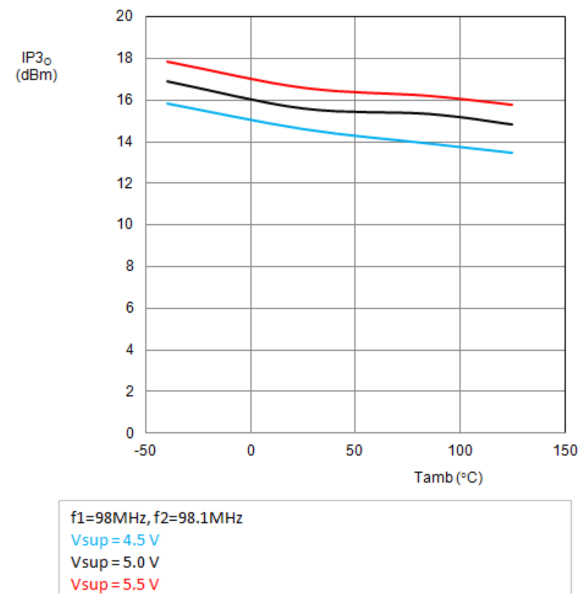

Fig 33. Measured OIP3 over temperature for different supply voltages

7.6 Noise Figure = f (Freq)

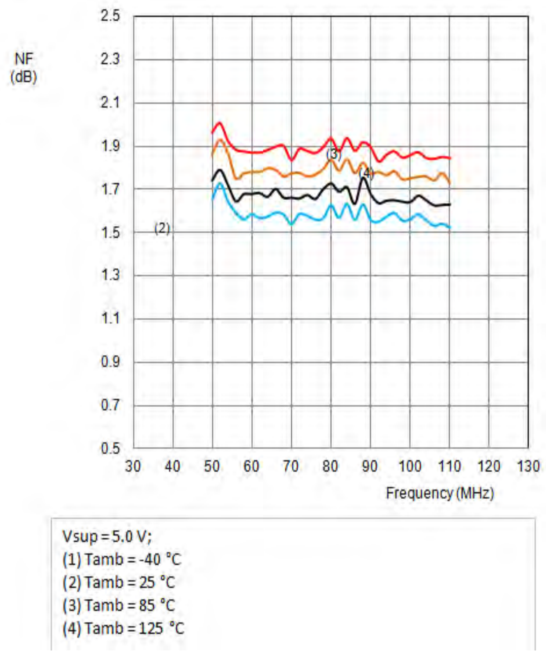

Fig 34. Measured Noise Figure over frequency for different temperatures

8. Conclusions / recommendations

Witt the BFU580Q a simple and cheap FM band LNA design with NF close to 1.6 dB with IOP3 of +15 dBm in 50Ω system can be implemented. The LNA draws approximately 23 mA and has good input and output matching properties.

In case a 75Ω LNA is required design version 3 can be used, the NF that can be achieved is 1.2 dB and OIP3 +19 dBm at 25 mA supply current.

Shown circuits can be used as a base for derivative designs. Matching to other frequencies can be done by tuning relevant capacitors and inductors.

9. References

BFU58Q datasheet

BFU5xxQ starter-kit (5) User Manual, UM10772

10. Abbreviations

LNA	Low Noise Amplifier
FM	Frequency Modulation
AN	Application Note
PCB	printed Circuit Board
RF	Radio Frequency
OIP3	Third order Output Intersection Point
NF	Noise Figure
BOM	Bill of Materials
SMD	Surface Mounted Devices
DC	Direct Current

11. Legal information

11.1 Definitions

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