AN11096

Using the LPC178x/7x power modes

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Document information

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Abstract	This application note introduces the various low power modes of the LPC177x/8x series, the steps required to enter the low power modes and helpful hints to reduce power consumption. This application note also provides a software example to enter the low power modes and demonstrates how to measure the power consumption.

Revision history

Rev	Date	Description
1	20120424	Initial revision.

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1. Introduction

The LPC178x/177x is an ARM Cortex-M3 based microcontroller for embedded applications requiring a high level of integration and low power dissipation. The Cortex-M3 is a next generation core that offers better performance than the ARM7 at the same clock rate, and offers other system enhancements such as modernized debug features and a higher level of support block integration. The Cortex-M3 CPU incorporates a 3-stage pipeline and has a Harvard architecture with separate local instruction and data buses, as well as a third bus with slightly lower performance for peripherals. The Cortex-M3 CPU also includes an internal prefetch unit that supports speculative branches. The LPC178x/177x adds a specialized flash memory accelerator to give optimal performance when executing code from flash. The LPC178x/177x is targeted to operate at up to a 100 MHz CPU frequency under worst case commercial conditions.

The peripheral complement of the LPC178x/177x includes up to 512 kB of flash memory, up to 96 kB of data memory, 4 kB of EEPROM memory, an External Memory Controller for SDRAM and static memory access, an LCD panel controller, an Ethernet MAC, a General Purpose DMA controller, a USB device/host/OTG interface, 5 UARTs, 3 SSP controllers, 3 I^2C-bus interfaces, an I^2S-bus serial audio interface, a 2-channel CAN interface, an SD card interface, an 8 channel 12-bit ADC, a 10-bit DAC, a Motor Control PWM, a Quadrature Encoder Interface, 4 general purpose timers, a 6-output general purpose PWM, an ultra-low power RTC with separate battery supply, a windowed watchdog timer, a CRC calculation engine, up to 165 general purpose I/O pins, and more. The pinout of LPC178x/177x is intended to allow pin function compatibility with the LPC24xx and LPC23xx.

The LPC178x/7x series targets a wide range of applications, including eMetering, lighting, industrial networking, alarm systems, white goods and motor control.

This application note attempts to introduce the various low power modes of the LPC178x/7x series, the steps required to enter the low power modes and helpful hints to reduce power consumption. This application note also provides a software example to enter the low power modes, and demonstrates how to measure the power consumption using the IAR LPC1788-SK board.

The various topics covered in this application note are as follows:

1. LPC178x/7x Power Structure and Management
2. Entering low power modes and code example
3. Additional hints to reduce power consumption
4. Low power mode demo using the IAR LPC1788-SK Board

2. Power structure and management

The following section covers the following topics:

- Power domains
- Low power down modes

2.1 Power domains

There are five main power domains in the LPC178x/7x

1. $V_{DD(reg)(3V3)}$ – on-chip voltage regulator (2.4 V to 3.6 V)
2. $V_{DD(3V3)}$ – I/O pads (2.4 V to 3.6 V)
3. VBAT (2.1 V to 3.6 V) – Power only to the RTC and Backup Registers
4. VDDA (2.7 V to 3.6 V) – Analog Supply Power to 12 Bit ADC
5. VREFP (2.7 V to 3.6 V) – Analog Reference Voltage to 12 Bit ADC

The LPC178x/7x implements a separate VBAT power domain in order to allow turning off power to the bulk of the device while maintaining operation of the Real Time Clock. The VBAT pin supplies power only to the RTC domain. Whenever the device core power ($V_{DD(reg)(3V3)}$) is present and higher than the VBAT power, the core power is used to operate the RTC, causing no power drain from a battery (see Fig 1). If the battery voltage is higher than the $V_{DD(reg)(3V3)}$ rail when the system is powered, then the battery will always supply the Real Time Clock power. For this reason, we recommend using a nominal 3.0 V battery and 3.3 V $V_{DD(reg)(3V3)}$ when using VBAT.

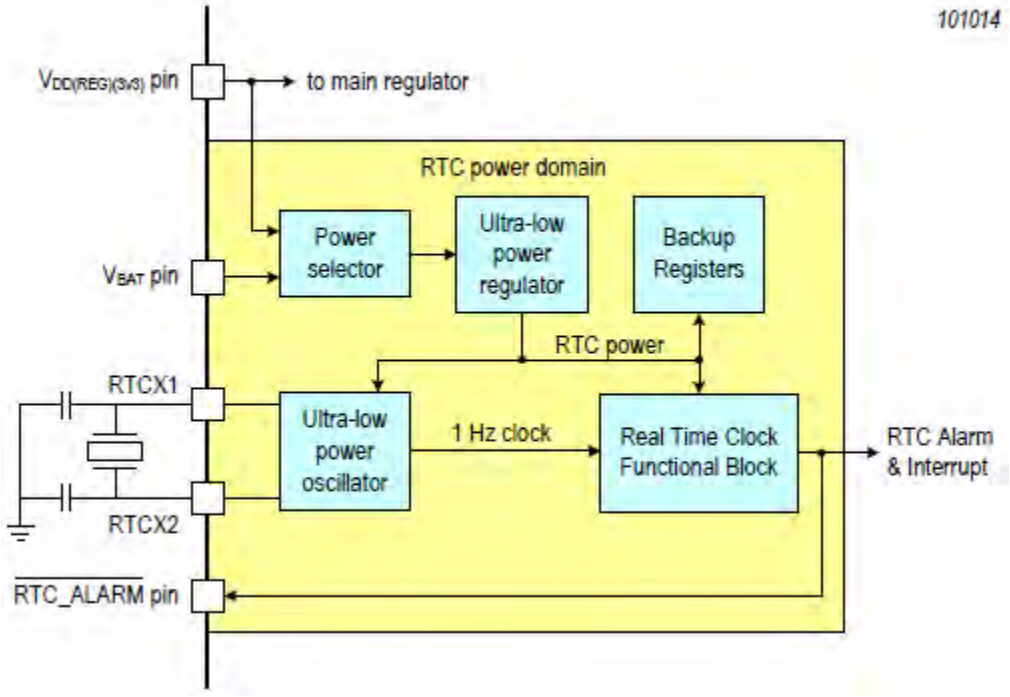

Fig 1. LPC178x/7x RTC domain conceptual diagram

2.2 Power modes

On the LPC178x/7x series, there are four reduced power modes: Sleep, Deep-Sleep, Power-down, and Deep Power-down modes.

The following sections cover the power reduction modes for the LPC178x/7x.

2.2.1 Sleep mode

In Sleep mode, execution of instructions is suspended (clock to the core is stopped) until either a Reset or an interrupt occurs. The SMFLAG bit in PCON is set. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. The GPDMA may operate in Sleep mode to access AHB SRAMs and peripherals with GPDMA support, but may not access the flash memory or the main SRAM, which are disabled in order to save power. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

Wake-up from Sleep mode will occur whenever any enabled interrupt occurs.

2.2.2 Deep-sleep mode

When the chip enters the Deep Sleep mode, the main oscillator is powered down, and nearly all clocks are stopped, and the DSFLAG bit in PCON is set. The IRC remains running and can be configured to drive the Watchdog Timer, allowing the Watchdog to wake up the CPU. The 32 kHz RTC oscillator is not stopped and RTC interrupts may be used as a wakeup source. The flash is left in the standby mode allowing a quick wakeup. The PLLs are automatically turned off and disconnected and the clock selection

multiplexers are set to use sysclk (the reset state). The clock divider registers are automatically reset to zero.

The processor state and registers, peripheral registers, and internal SRAM values are preserved throughout Deep Sleep mode and the logic levels of chip pins remain static. The Deep Sleep mode can be terminated and normal operation resumed by either a Reset or certain specific interrupts that are able to function without clocks. Since all dynamic operation of the chip is suspended, Deep Sleep mode reduces chip power consumption to a very low value.

On the wake-up of Deep Sleep mode, if the IRC was used before entering Deep Sleep mode, a 2-bit IRC timer starts counting and the code execution and peripherals activities will resume after the timer expires (4 cycles). If the main external oscillator was used, the 12-bit main oscillator timer starts counting and the code execution will resume when the timer expires (4096 cycles). The user must remember to reconfigure any required PLLs and clock dividers after the wake-up.

Wake-up from Deep Sleep mode can be brought about by NMI, External Interrupts EINT0 through EINT3, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a Watchdog Timer timeout, a USB input pin transition (USB activity interrupt), or a CAN input pin transition (CAN Activity Interrupt), generated by activity on the CAN bus pins. In addition, the watchdog timer can wake up the part from Deep Sleep mode if the watchdog timer is being clocked by the IRC oscillator.

2.2.3 Power-down mode

Power-down mode does everything that Deep Sleep mode does, but also turns off the flash memory. This saves more power, but requires waiting for resumption of flash operation before execution of code or data access in the flash memory can be accomplished. Entry to Power-down mode causes the PDFLAG bit in the PCON to be set. When the chip enters Power-down mode, the IRC, the main oscillator, and all clocks are stopped. The RTC remains running if it has been enabled and RTC interrupts may be used to wake up the CPU. The flash is forced into Power-down mode. The PLLs are automatically turned off and disconnected. The CCLK and USBCLK clock dividers automatically get reset to zero. Upon wake-up from Power-down mode, if the IRC was used before entering Power-down mode, after IRC-start-up time (about 60 µs), the 2-bit IRC timer starts counting and expiring in 4 cycles. Code execution can then be resumed immediately following the expiration of the IRC timer if the code was running from SRAM. In the meantime, the flash wake-up timer measures flash start-up time of about 100 µs. When it times out, access to the flash is enabled. The user must remember to reconfigure any required PLLs and clock dividers after the wake-up.

Wake-up from Power-down mode can be brought about by NMI, External Interrupts EINT0 through EINT3, GPIO interrupts, the Ethernet Wake-on-LAN interrupt, Brownout Detect, an RTC Alarm interrupt, a Watchdog Timer timeout, a USB input pin transition (USB activity interrupt), or a CAN input pin transition (CAN Activity Interrupt), generated by activity on the CAN bus pins.

2.2.4 Deep power-down mode

In Deep Power-down mode, power is shut off to the entire chip with the exception of the Real-Time Clock, the RESET pin, the Wakeup Interrupt Controller (WIC), and the RTC backup registers. Entry to Deep Power-down mode causes the DPDFLAG bit in PCON to be set. To optimize power conservation, the user has the additional option of turning off or retaining power to the 32 kHz oscillator. It is also possible to use external circuitry to turn off power to the on-chip regulator via the $V_{DD(REG)(3V3)}$ pins after entering Deep

power-down mode. Power to the on-chip regulator must be restored before device operation can be restarted.

Wake-up from Deep power-down mode will occur when an external reset signal is applied, or the RTC interrupt is enabled and an RTC interrupt is generated.

3. Entering low power modes and code example

This section describes the mechanism to put the LPC178x/7x into the four low power modes (sleep, deep-sleep, power-down, deep power-down).

3.1 System Control Register (SCR)

The SCR register controls features of entry to and exit from low power modes.

Sleep mode and Deep Sleep mode are selected by the SLEEPDEEP bit in the Cortex-M3 System Control Register (SCR).

The bit assignments are shown in Fig 2.

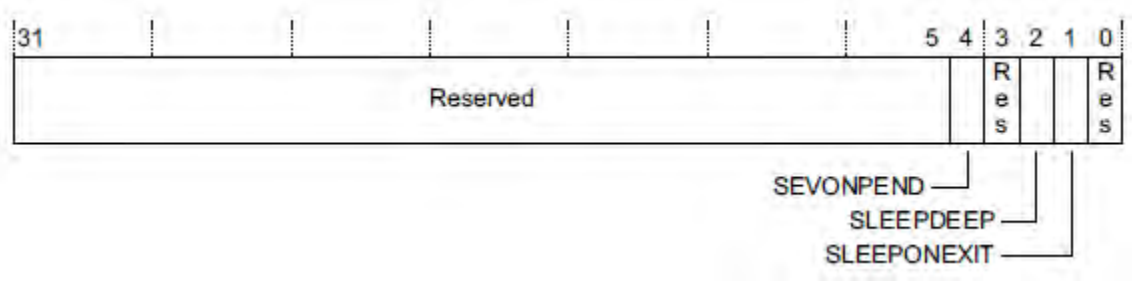

Fig 2. LPC178x/7x System Control Register (SCR, 0xE000ED10)

If the SLEEPDEEP bit in the Cortex-M3 System Control Register (SCR) is 0, Sleep mode is selected.

If the SLEEPDEEP bit in the Cortex-M3 System Control Register (SCR) is 1, Deep-sleep mode is selected.

If the SLEEPONEXIT bit of the SCR is set to 1, when the processor completes the execution of an exception handler and immediately enters Sleep mode. This mechanism is useful for applications that only require the processor to run when an exception occurs. If SLEEPONEXIT bit is set in the System Control Register, core will automatically enter the low power mode once the ISR has completed. This allows a low power application to be entirely interrupt-driven, so that the Cortex core will wake up, run the appropriate code and then re-enter the mode with minimal code being used for power management

3.2 PCON register

Power down and Deep Power-down modes are selected by the PM1 and PM0 bits in the PCON register and the SLEEPDEEP bit in the Cortex-M3 System Control Register (SCR) is set to 1.

Table 35. Power Mode Control register (PCON - address 0x400F C0C0) bit description

Bit	Symbol	Description	Reset value
0	PM0	Power mode control bit 0. This bit controls entry to the Power-down mode. See Section 4.7.7.1 below for details.	0
1	PM1	Power mode control bit 1. This bit controls entry to the Deep Power-down mode. See Section 4.7.7.1 below for details.	0
2	BODRPM	Brown-Out Reduced Power Mode. When BODRPM is 1, the Brown-Out Detect circuitry will be turned off when chip Power-down mode or Deep Sleep mode is entered, resulting in a further reduction in power usage. However, the possibility of using Brown-Out Detect as a wake-up source from the reduced power mode will be lost. When 0, the Brown-Out Detect function remains active during Power-down and Deep Sleep modes. See the System Control Block chapter for details of Brown-Out detection.	0
3	BOGD	Brown-Out Global Disable. When BOGD is 1, the Brown-Out Detect circuitry is fully disabled at all times, and does not consume power. When 0, the Brown-Out Detect circuitry is enabled. See the System Control Block chapter for details of Brown-Out detection.	0
4	BORD	Brown-Out Reset Disable. When BORD is 1, the BOD will not reset the device when the $V_{DD(REG)(3V3)}$ voltage dips goes below the BOD reset trip level. The Brown-Out interrupt is not affected. When BORD is 0, the BOD reset is enabled. See the Section 3.6 for details of Brown-Out detection.	0
7:3	-	Reserved. Read value is undefined, only zero should be written.	NA
8	SMFLAG	Sleep Mode entry flag. Set when the Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [1][2]
9	DSFLAG	Deep Sleep entry flag. Set when the Deep Sleep mode is successfully entered. Cleared by software writing a one to this bit.	0 [1][2]
10	PDFLAG	Power-down entry flag. Set when the Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [1][2]
11	DPDFLAG	Deep Power-down entry flag. Set when the Deep Power-down mode is successfully entered. Cleared by software writing a one to this bit.	0 [1][3]
31:12	-	Reserved. Read value is undefined, only zero should be written.	NA

[1] Only one of these flags will be valid at a specific time.

[2] Hardware reset value only for a power-up of core power or by a brownout detect event.

[3] Hardware reset value only for a power-up event on Vbat.

Fig 3. LPC178x/7x Power Mode Control Register (PCON)

The PCON register also contains flags that indicate whether entry into each reduced power mode actually occurred.

3.3 Wait For Interrupt (WFI) instruction

Execution of the WFI instruction will cause immediate entry to any of the four reduced power modes based on the SLEEPDEEP bit and PCON Register settings mentioned above.

The WFI instruction is a Cortex-M3 instruction which cannot be directly accessible by ANSI C. The CMSIS (Cortex Microcontroller Software Interface Standard) provides an intrinsic function to generate a WFI instruction and supported by C compiler.

If a C compiler does not support the WFI intrinsic function, then the user will have to use inline assembler to access WFI instruction.

Fig 4 below shows the encoding for the three reduced power modes supported by the LPC178x/7x.

Table 36. Encoding of reduced power modes

PM1, PM0	Description
00	Execution of WFI or WFE enters either Sleep or Deep Sleep mode as defined by the SLEEPDEEP bit in the Cortex-M3 System Control Register.
01	Execution of WFI or WFE enters Power-down mode if the SLEEPDEEP bit in the Cortex-M3 System Control Register is 1.
10	Reserved, this setting should not be used.
11	Execution of WFI or WFE enters Deep Power-down mode if the SLEEPDEEP bit in the Cortex-M3 System Control Register is 1.

Fig 4. LPC178x/7x Encoding of reduced power modes

3.4 Code example

The code below demonstrates the entry into each of the four low power modes. The code below is used in the low power mode demo which will be covered later.

3.4.1 Sleep mode

```
/*Clear the PCON*/
LPC_SC->PCON = 0x0;

/*Clear the SLEEPDEEP bit in the Cortex M3 System Control Register*/
SCB->SCR = 0x0;

/*WFI instruction*/
__WFI();
```

Fig 5. LPC178x/7x code example (Sleep mode)

3.4.2 Deep-sleep mode

```
/*Set SLEEPDEEP bit in the Cortex M3 System Control Register*/
SCB->SCR |= 0x04;

/*PCON register + disable BOD*/
LPC_SC->PCON = 0x8;

/*WFI instruction*/
__WFI();
```

Fig 6. LPC178x/7x code example (Deep-sleep mode)

3.4.3 Power-down mode

```
/*Set SLEEPDEEP bit in the Cortex M3 System Control Register*/
SCB->SCR |= 0x04;

/*PCON register + disable BOD*/
LPC_SC->PCON = 0x9;

/*WFI instruction*/
__WFI();
```

Fig 7. LPC178x/7x code example (Power-down mode)

3.4.4 Deep Power-down mode

```
/*Set SLEEPDEEP bit in the Cortex M3 System Control Register*/
SCB->SCR |= 0x04;

/*PCON register*/
LPC_SC->PCON = 0x3;

/*WFI instruction*/
__WFI();
```

Fig 8. LPC178x/7x code example (Deep power-down mode)

4. Additional tips to reduce power consumption

On the LPC178x/7x series, the current consumption can be further reduced by considering the following points:

4.1 CPU clock rate

On the LPC178x/7x, the CPU clock rate can be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements.

Lowering the PLL0's output frequency (FCCO, 275 MHz to 550 MHz) can also save power.

An 8-bit CPU clock divider allows a range of options, including slowing CPU operation to a low rate for temporary power savings without turning off PLL0.

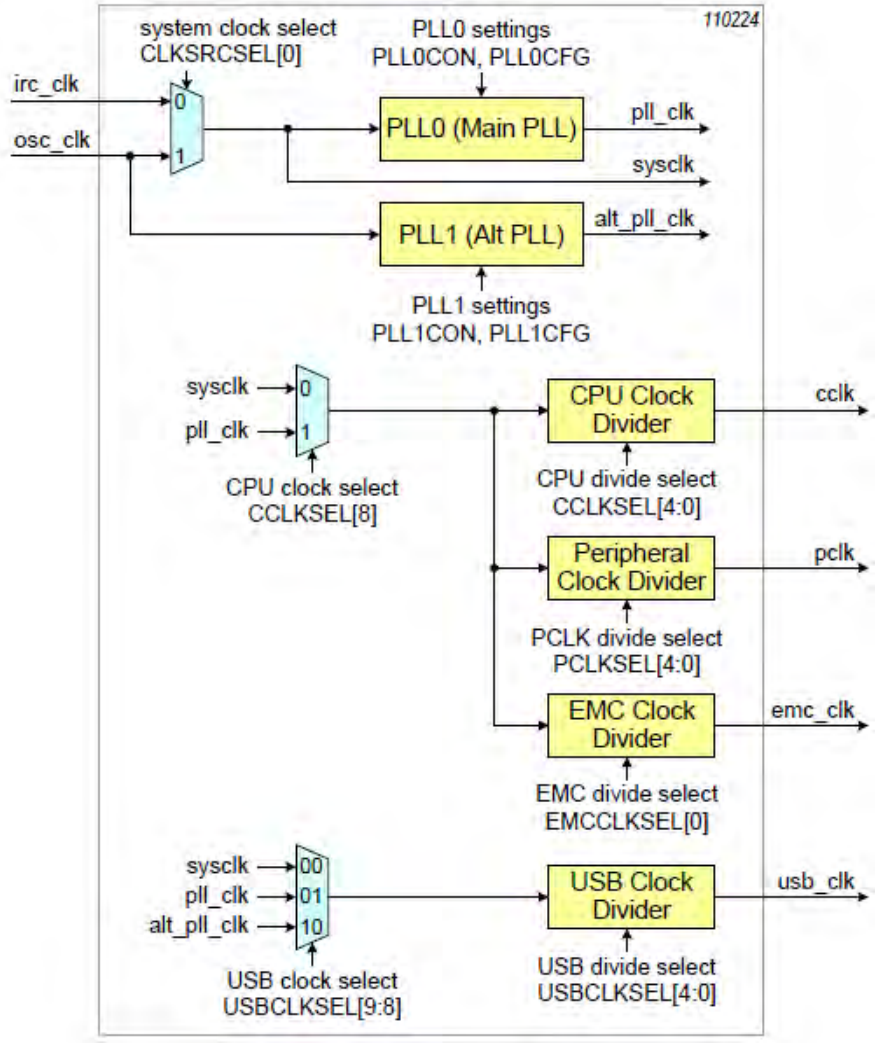

Fig 9. LPC178x/7x Clock Generation Unit (CGU) diagram

4.2 Peripheral power control register (PCONP)

Peripherals Power Control Register contains control bits that enable and disable individual peripheral functions, allowing elimination of power consumption by peripherals that are not needed. This feature allows individual peripherals to be turned off if they are not needed in the application, resulting in additional power savings. Each bit in PCONP controls one peripheral. If a peripheral control bit is 1, that peripheral is enabled. If a peripheral control bit is 0, that peripheral's clock is disabled (gated off) to conserve power. For example, if bit 19 is 1, the I2C1 interface is enabled. If bit 19 is 0, the I2C1 interface is disabled. Note that valid read from a peripheral register and valid write to a peripheral register is possible only if that peripheral is enabled in the PCONP register. See the LPC17xx User Manual for details.

4.3 Miscellaneous

4.3.1 Flash accelerator

Enable the flash accelerator if the application is running from the on-chip flash. Enabling the flash accelerator will enable various buffers and reduces the number of flash fetches thereby reducing power consumption.

4.3.2 Brown-Out Detect (BOD)

The Brown-out Detect (BOD) circuit is turned on by default and can increase the static current (deep-sleep and power-down) by 40 μA. If the BOD is not needed, it can be disabled by using the PCON register (see Fig 3).

4.3.3 Software

Most embedded applications terminate with a while(1) loop, and they service interrupts whenever needed. In this case, code is still constantly fetched from the on-chip flash and executed which adds to the power consumption. A better solution would be to switch to the sleep power saving mode and then wait for interrupts. An interrupt from a peripheral would then wake the device from Sleep mode. Considerable power savings can be achieved by keeping the core in Sleep mode while it is waiting for interrupts.

4.3.4 Port pins

User can take further steps to reduce current consumption on the 3.3 V rail ($V_{DD(3V3)}$ - supply voltage for IO ports) in the low power modes. The general purpose port pins on the LPC178x/7x series have programmable internal pull-ups enabled by default. Before entering low power modes, user can reduce the $V_{DD(3V3)IO}$ supply voltage current as follows:

1. All General Purpose I/O pins (GPIO) default to input with pull-up resistor enabled. Using the PINMODEx registers, first, disable the internal pull-ups on all general port pins. Second, configure the IOs as GPIO outputs and drive them low, OR
2. Using the PINMODEx registers, first disable the internal pull-ups on all general port pins. Second, configure the IOs as GPIO inputs and using an external resistor, pull the IOs high or low.
3. Using an external resistor, pull the TCK pin (JTAG Test Clock) low. If floating, the IO current increases by 40 μA.

Please note that in deep power-down mode, state of the port pins does not affect the current consumption and the steps mentioned above do not need to be considered in this mode.

4.3.5 Debug notes

The user should be aware of certain limitations during debugging. The most important is that, due to limitations of the Cortex-M3 integration, the LPC17xx cannot wake up in the usual manner from Deep Sleep and Power-down modes. It is recommended not to use these modes during debug. Once an application is downloaded via JTAG/SWD interface, the USB to SWD/JTAG debug adapter (Keil ULINK2 for example) should be removed from the target board; thereafter, power cycle the LPC17xx to allow wake-up from deep sleep and power-down modes. Another issue is that debug mode changes the way in which reduced power modes are handled by the Cortex-M3 CPU. This causes power modes at the device level to be different from normal modes operation. These differences mean that power measurements should not be made while debugging, the results will be higher than during normal operation in an application.

5. Low power mode demo

5.1 Requirements

5.1.1 Hardware

IAR LPC1788-SK (see Fig 10).

Keil ULINK2 USB -JTAG Adapter

RS-232 serial cable

Note: Instead of using the ULINK2 JTAG module to program the LPC178x/7x, you can use an RS-232 serial cable along with the FlashMagic programming tool that is available at no charge at http://www.flashmagictool.com/

5.1.2 Software

Keil uVision4 (evaluation version will work for the demo).

The project demo is CMSIS (Cortex Microcontroller Software Interface Standard) compliant.

TeraTerm or HyperTerminal window is needed to display the options to enter low power modes.

5.2 Objective

The objective of the demo is to allow LPC178x/7x users to enter and wake-up from the low power modes, and demonstrates how to measure the power consumption using the IAR LPC1788-SK board. In addition, the demo allows users to evaluate the active mode current for frequencies 12 MHz, 48 MHz, 100 MHz, and 120 MHz. The following sections provide the necessary steps to set-up the low power mode demo.

5.2.1 Hardware set-up

The IAR LPC1788-SK board has jumpers available to allow users to measure the $V_{DD(reg)(3V3)}$ current and the VBAT current. Users can connect an ammeter on these jumpers to measure the current.

In this demonstration, following options are available to wake-up the device from the low power modes:

1. The UART0 (press any key on the keyboard to generate UART0 interrupt) or RESET push button can be used to wake-up the LPC178x/7x when in Sleep mode.
2. The power can be cycled to wake-up the LPC178x/7x when in deep-sleep, power-down, and deep power-down modes.

To prevent the ISP and RST control via the PC serial port from affecting the results, while current measurement is being done a terminal program should be left running on the PC.

The COM0 (UART0) will be used to display low power mode menu.

As previously mentioned in the Debug Notes section, once the application is downloaded via JTAG/SWD interface, the Keil ULINK2 should be kept removed from the target board; thereafter, power cycle or reset the LPC17xx to allow wake-up from deep sleep and power-down modes.

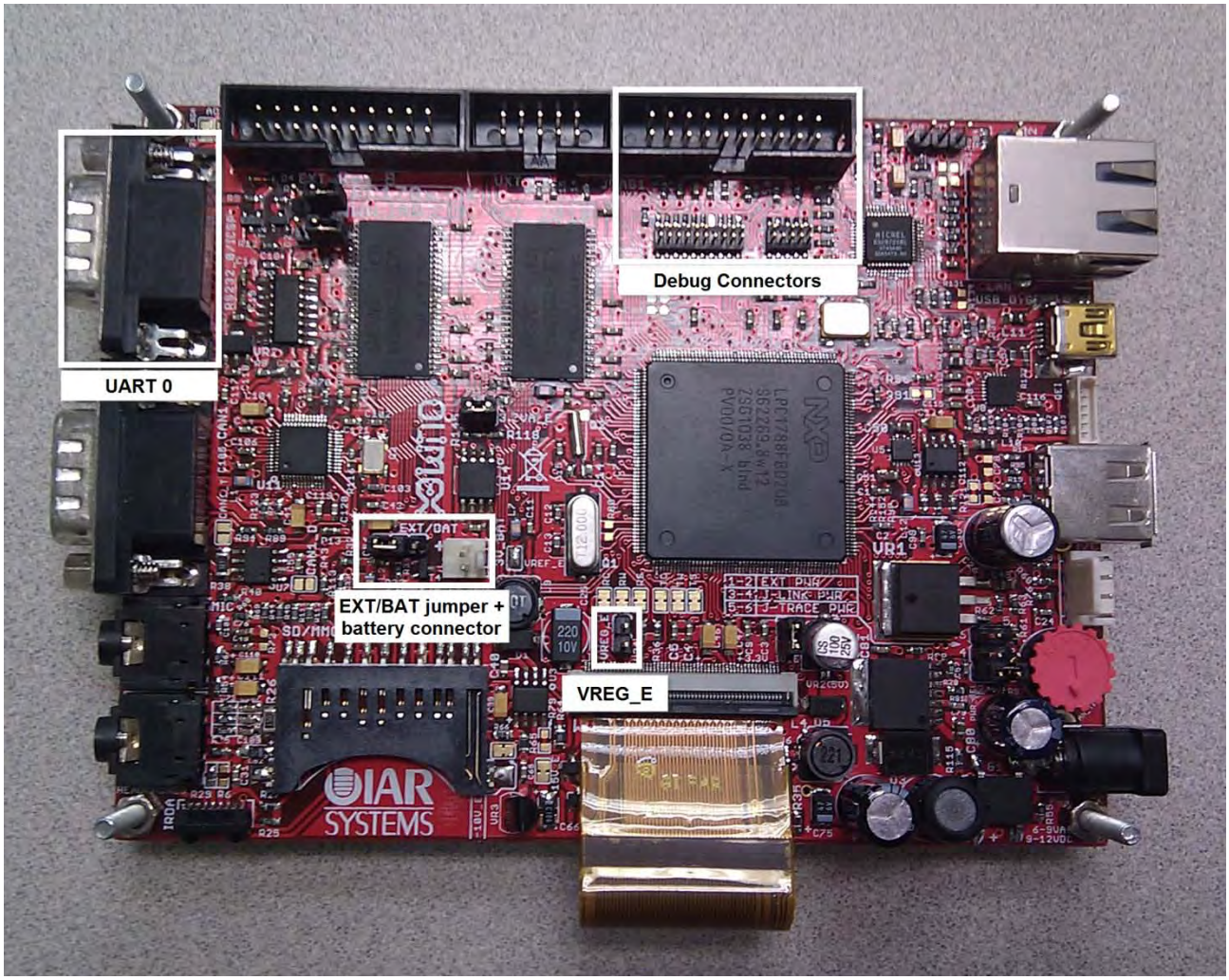

Fig 10. IAR LPC1788-SK board

5.2.2 Terminal program settings

This demo uses Tera Term and the settings for the serial port are shown in Fig 11).

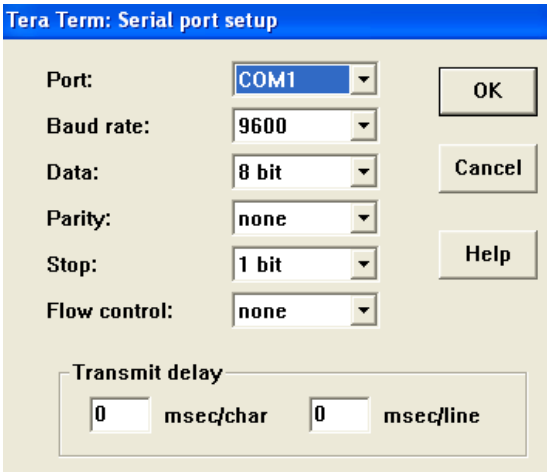

Fig 11. Terminal program settings

5.2.3 Output

The output of the code is shown in Fig 12.

The menu below instructs how to evaluate the active mode current for frequencies 12 MHz, 48 MHz, 100 MHz, and 120 MHz, and lastly, shows how to select and exit the four low power modes.

```
Welcome to the LPC1700 Low Power Modes
Default Set-up is Active Mode, Core Freq 120 MHz, PLL0 Enabled, GPIO Enabled, PCLK/4, GPIO
+Uart0 Enabled
Note: After programming the part, you must disconnect the debugger and then cycle power to
 get correct current measurements.

1. Active Mode, Core Freq  12 MHz, PLL0 Disabled, PCLK/4, GPIO+Uart0 Enabled
2. Active Mode, Core Freq  48 MHz, PLL0 Enabled,  PCLK/4, GPIO+Uart0 Enabled
3. Active Mode, Core Freq  96 MHz, PLL0 Enabled,  PCLK/4, GPIO+Uart0 Enabled
4. Active Mode, Core Freq 120 MHz, PLL0 Enabled,  PCLK/4, GPIO+Uart0 Enabled

s. Sleep Mode, PCLK/4, GPIO+Uart0 Enabled
S. Deep Sleep Mode
p. Power-down Mode
P. Deep Power-down Mode

PEntering deep power-down mode
Reset to exit.
```

Fig 12. LPC178x/7x low power mode demo

5.3 Power measurements

Table 1 shows the typical power consumption measurement made using the demo on the 80 Pin RTC Board:

Table 1. Typical power consumption

LPC178x/7x Active Power Modes	**Ireg(3V3) current**
Active mode (12 MHz, PLL disabled, all peripherals off except UART0 + GPIO)	8.6 mA
Active mode (48 MHz, PLL enabled, all peripherals off except UART0 + GPIO)	25.6 mA
Active mode (96 MHz, PLL enabled, all peripherals off except UART0 + GPIO)	47.2 mA
Active mode (120 MHz, PLL enabled, all peripherals off except UART0 + GPIO)	58.0 mA
LPC178x/7x Low Power Modes	**Ireg(3V3) current**
Sleep Mode (48 MHz, PLL enabled, All peripherals off except UART0 + GPIO)	12.1 mA
Deep-Sleep Mode (BOD disabled)	362 uA
Power-down Mode (BOD disabled)	52 uA
Deep power-down mode	637 nA @ VDDREG 579 nA @ VBAT

Conditions: $V_{reg(3V3)}$ = 3.3 V, VBAT = 3.3 V, Temperature = 25 °C, All peripherals disabled except UART0 (9600 baud-rate) running in active and sleep modes, All pins (except UART0 pins) configured as GPIO outputs and driven low, internal pull-ups disabled.

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7. Contents

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