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LPC122x power modes

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Application note

Document information

Info	Content
Keywords	LPC122x power modes low power
Abstract	This application note details the LPC122x power modes and how to properly use them to achieve an application's power requirements.

Revision history

Rev	Date	Description
1	20110419	Initial version.

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1. Introduction

The LPC122x families of devices support several power control modes:

- Active
- Sleep
- Deep-sleep
- Deep power-down

By properly understanding how each mode behaves a designer will be able to ensure that their particular application's power requirements are met. Be aware that a device's power consumption is a combined stack up of many factors, and can vary by design. If the guidelines outlined in this document are properly followed one should be able to properly implement a design with the ability to operate under very low power.

1.1 Active mode

Active mode is the default power mode after the device is reset. Here the device's Cortex-M0 core, system clock, peripheral clock, and all peripherals can be powered. Active mode can respond to all interrupt sources in the NVIC.

This mode will consume the most power, but based on a given design it can be optimized. For instance, running at the highest operating speed of 33 MHz via the system's PLL in active mode will consume more power than running at a frequency of 6 MHz by powering the system clock with the 12 MHz IRC and a divider factor of 2.

Another, albeit less typical example, would be in a design typically executed from RAM. In this situation, while running from RAM, the flash subsystem can be manually powered down. Care must be taken if trying to implement this type of behavior though, as calling any function which is placed in flash, or referencing any constant in flash will cause problems if the flash subsystem is not powered.

In a design that does not have a continuous power source always ensure that unused peripherals are completely powered down. This may include disabling the peripherals' relevant bits in the PDRUNCFG register, the AHBCLKCTRL register, the PRESETCTRL register (and in some cases setting the peripheral's specific clock divider to zero).

1.2 Sleep mode

Sleep mode is nearly identical to Active mode; the major differentiating factor is that the M0 core's code execution has been suppressed via the WFI instruction. In this mode any peripheral which was operational prior to invoking WFI will continue to operate, and may wake the M0 core by generating an interrupt. This mode will 'wake' from interrupt more quickly than Deep-sleep and Deep power-down, and should be used when rapid response to an external event is required. As with Active mode, the Micro DMA controller can be enabled in Sleep mode allowing peripherals to access memory without the M0's involvement.

1.3 Deep-sleep mode

Deep-sleep mode has several distinctions from Active and Sleep modes. In addition to suppressing the M0 core's clock, the following takes place:

- In Deep-sleep mode analog blocks are powered down[1].
- The system clock can be disabled, or sourced by the Watchdog Oscillator (if enabled).
- Wake up via PIO0_0 t to PIO0_11, RTC[2], Timer Match[3], BOD, WDT.

Note that the Watchdog Oscillator operates at a lower frequency than other clock sources and wakeup time will be extended due to this fact. When using Deep-sleep without the watchdog, the IRC oscillator will also have an extended wakeup time after the power to it is restored.

While the LPC122x is in Deep-sleep mode, the contents of RAM are preserved. In Deep-sleep mode the device may be externally reset at any time, or by the BOD or WDT.

1.4 Deep power-down mode

In Deep power-down mode the system is virtually reset. In this mode the WAKEUP pin is the only clocked subsystem. In Deep power-down the contents of RAM are not preserved, however the PMU's GPREG0-GPREG4[4] registers are non-volatile and can be used to store program state information while in Deep power-down. Note that the WAKEUP and reset pins must have external pull up resistors in place as the use of the internal pull up is not possible while in Deep power-down. While in Deep power-down the RESET pin is not active; RESET must be asserted after the part has been made active by asserting WAKEUP or a full power cycle must be applied in order to reset the device.

There are two methods to wake from Deep power-down on the LPC122x: the WAKEUP pin and a new feature to wake via RTC interrupt. To enable wake from RTC, no other action is needed. If an application will use Deep power-down and the RTC, but the wake event is only to be triggered via WAKEUP pin, the RTC interrupt must be masked in the RTCIMSC register.

Table 1. LPC122x power mode comparison

Power mode	M0 core	Flash	SRAM	Peripherals
Active	Clocked	Powered	Powered	Powered as configured
Sleep	Not Clocked	Powered	Powered	Powered as configured
Deep-Sleep	Not Clocked	Not Powered	Powered	Limited
Deep power-down	Not Clocked	Not Powered	Not Powered	Not Powered

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[1] With the exception of the BOD and Watchdog Oscillator which may be powered based on user configuration.

[2] See errata on using RTC to wake from Deep-sleep.

[3] When the selected Timer Match pin is selected in the NVIC start logic and enabled in the SYSAHBCLKCTRL register.

[4] See User's Manual for details about dedicated bits in GPREG4.

2. Wake up and Self wake up

2.1 Sleep mode

In Sleep mode, any interrupt is fully capable of resuming activity on the M0 core of the LPC122x.

2.2 Deep-sleep mode

Waking from Deep-sleep mode can be accomplished in one of several ways:

Table 2. Methods to wake from Deep-sleep

Wake method	Dependency
Port pin	Start Logic 0
RTC	Start Logic 1
WDT	WDT Powered, interrupt enabled
BOD	BOD Powered, interrupt enabled
Reset	RESETn, POR, BOD, WWDT, etc

2.3 Self wake up from RTC

The LPC122x adds two new methods to wake from reduced power modes. The first method pertains to waking from Deep-sleep mode. In this method of operation, the main clock must be sourced via the WDT oscillator and it must be configured to use the lowest possible frequency, the proper settings for the Start Logic 1 block must be configured to wake via RTC interrupt, and finally the RTC must be powered and enabled. Prior to entering Deep-sleep the match event for the RTC must be set. Once the timer match occurs the part will be woken.

When waking from Deep power-down mode via the RTC, all that must be done is to enable the RTC and configure the timer match prior to entering Deep power-down mode. The part will automatically wakeup on generation of an RTC interrupt signal. **NOTE**: Care should be taken when using Deep power-down mode and the RTC if match events are not intended to wake the device. This can be prevented by masking the RTC ISR using the ICSC register.

3. Suggested design guidelines

3.1 Place an external pull up resistor on WAKEUP

Always ensure that the PCB for the LPC122x has an external pull up resistor on the WAKEUP pin. This will allow you to use Deep power-down for maximum power savings should it be needed to meet your power budget.

If using external reset, also consider using an external pull up resistor on the RESET signal.

3.2 Allocate pins capable of waking your application

Many designs implement a periodic wakeup event. If you need to wake your device from Deep-sleep periodically, you'll want to ensure that one of the startup logic pins (P0_0-P0_11) can be allocated for waking the device.

3.3 If using self timed wakeup via RTC plan for an external oscillator

Applications which use the LPC122x RTC for self timed wakeup should use an external 32,768 Hz crystal oscillator. This will ensure accurate time keeping, and enable the most flexible design. Should an application require self timed wakeup from Deep power-down, the RTC cannot be sourced via PCLK as this clock source is disabled in Deep power-down.

3.4 Define wakeup timing requirements

If an application has very constrained wakeup time requirements, consider a tiered approach. For short periods of inactivity Sleep mode may be sufficient, followed by longer periods of Deep-sleep or Deep power-down.

3.5 Determine which peripherals will be powered while asleep

Always determine which peripherals will not be needed while in reduced power modes. As seen in Table 3, certain peripherals consume more power than others.

Table 3. Estimated LPC122x peripheral current consumption
Measured on typical device operating at 24 MHz. Peripherals were not being actively used.

Peripheral	Current (mA)
Comparator	0.013
CRC	0.039
GPIO0	0.437
GPIO1	0.438
GPIO2	0.460
I2C	0.094
IOCON	0.098
ROM	0.259
SSP	0.308
Timer16	0.098
Timer32	0.094
UART	0.518

3.6 Define performance requirements for Active mode

Most designs with limited power will attempt to minimize the time the processor spends while “awake”. In some designs, however, further optimization can be made. For instance, it may not be necessary to run the LPC122x at the highest operating frequency while active. Instead, sourcing the system clock from the 12 MHz IRC may be sufficient. This would benefit in two ways: First, the time it takes to power and lock the PLL may be considerably longer than simply powering the IRC. This would result in reduced startup overhead when waking from Deep power-down. Second, the power consumption of the 12 MHz IRC will be lower than that of the system when running at higher speeds via the PLL. If a design can support even lower operating frequencies while in Active mode, you should design your firmware to make use of the SYSAHBCLKDIV register to further reduce the system clock speed. Also consider operating peripheral clocks with the highest divisor to reduce their current consumption.

4. Register overview

4.1 System Control Register (SCR)

The SCR register controls features of entry to and exit from low power modes.

Sleep mode and Deep-sleep mode are selected by the SLEEPDEEP bit in the Cortex-M0 System Control Register (SCR).

If the SLEEPDEEP bit in the Cortex-M0 System Control Register (SCR) is 0, Sleep mode is selected.

If the SLEEPDEEP bit in the Cortex-M0 System Control Register (SCR) is 1, Deep-sleep mode is selected.

If the SLEEPONEXIT bit of the SCR is set to 1, the processor completes the execution of an exception handler and immediately enters Sleep mode. This mechanism is useful for applications that only require the processor to run when an exception occurs. If SLEEPON EXIT bit is set in the System Control Register, core will automatically enter the low power mode once the ISR has completed. This allows a low power application to be entirely interrupt-driven, so that the Cortex core will wakeup, run the appropriate code and then re-enter the mode with minimal code being used for power management.

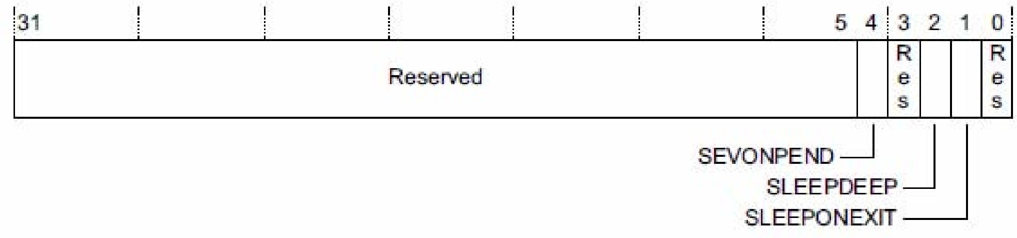


Fig 1. System control register bit fields

4.2 Power Control (PCON)

The PCON register selects whether one of the ARM Cortex-M0 controlled power-down modes (Sleep mode or Deep-sleep mode) or the Deep power-down mode is entered. It also provides the flags for Sleep or Deep-sleep modes and Deep power-down modes respectively. These are detailed in Fig 2.

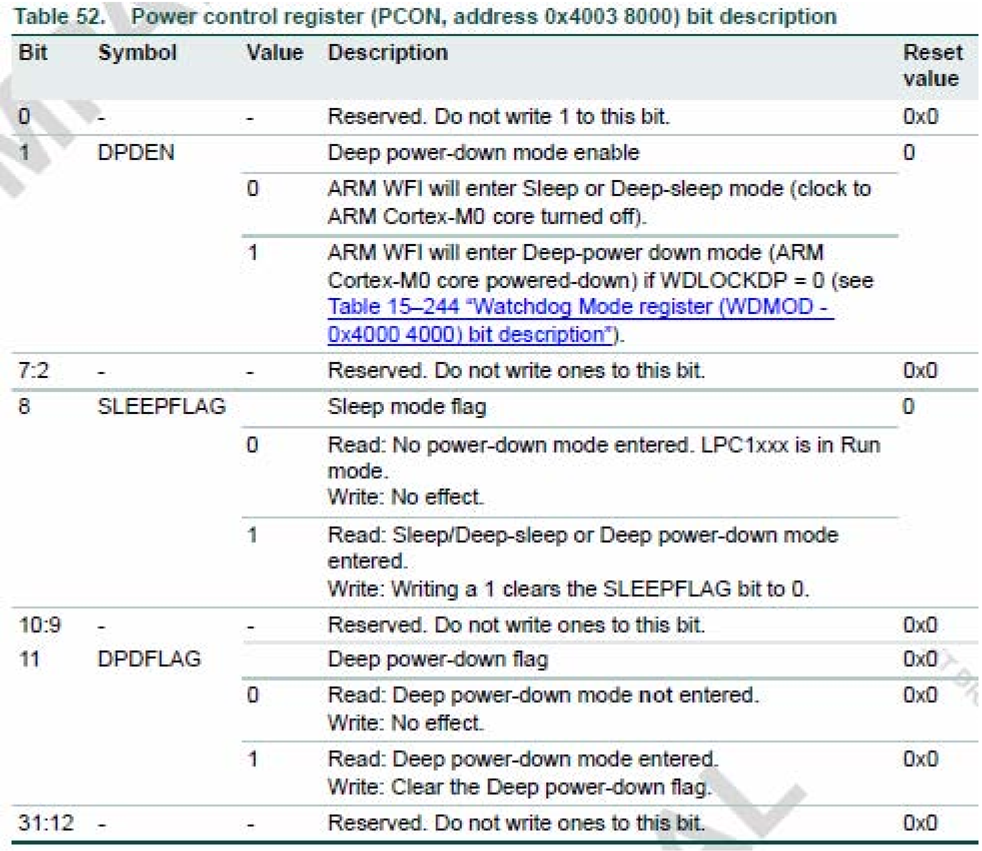


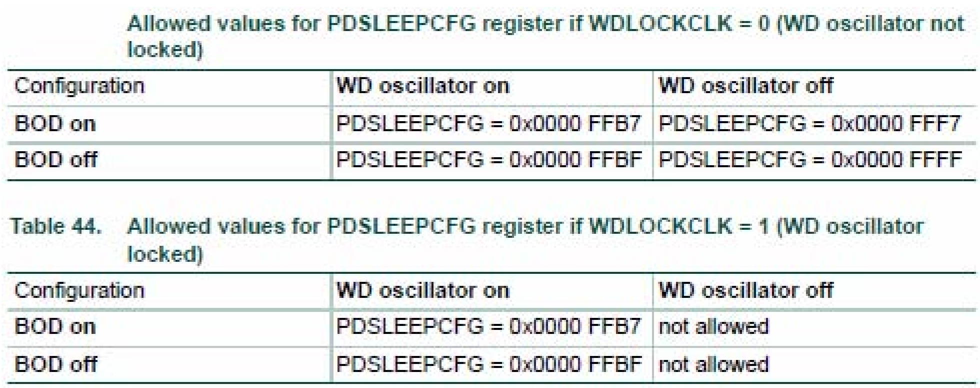
Table 52. Power control register (PCON, address 0x4003 8000) bit description

Bit	Symbol	Value	Description	Reset value
0	-	-	Reserved. Do not write 1 to this bit.	0x0
1	DPDEN		Deep power-down mode enable	0
		0	ARM WFI will enter Sleep or Deep-sleep mode (clock to ARM Cortex-M0 core turned off).	
		1	ARM WFI will enter Deep-power down mode (ARM Cortex-M0 core powered-down) if WDLOCKDP = 0 (see Table 15–244 "Watchdog Mode register (WDMOD - 0x4000 4000) bit description").	
7:2	-	-	Reserved. Do not write ones to this bit.	0x0
8	SLEEPFLAG		Sleep mode flag	0
		0	Read: No power-down mode entered. LPC1xxx is in Run mode. Write: No effect.	
		1	Read: Sleep/Deep-sleep or Deep power-down mode entered. Write: Writing a 1 clears the SLEEPFLAG bit to 0.	
10:9	-	-	Reserved. Do not write ones to this bit.	0x0
11	DPDFLAG		Deep power-down flag	0x0
		0	Read: Deep power-down mode not entered. Write: No effect.	0x0
		1	Read: Deep power-down mode entered. Write: Clear the Deep power-down flag.	0x0
31:12	-	-	Reserved. Do not write ones to this bit.	0x0

Fig 2. Power control register bit fields

4.3 Deep-sleep mode Configuration (PDSLEEPCFG)

In Deep-sleep mode only four values are allowed. Based on the application, the WDT oscillator, the BOD, or both can remain powered. If the WDT has been locked, settings which do not power it are invalid and cannot be used. This can be seen in Fig 3.



Allowed values for PDSLEEPCFG register if WDLOCKCLK = 0 (WD oscillator not locked)

Configuration	WD oscillator on	WD oscillator off
BOD on	PDSLEEPCFG = 0x0000 FFB7	PDSLEEPCFG = 0x0000 FFF7
BOD off	PDSLEEPCFG = 0x0000 FFBF	PDSLEEPCFG = 0x0000 FFFF

Table 44. Allowed values for PDSLEEPCFG register if WDLOCKCLK = 1 (WD oscillator locked)

Configuration	WD oscillator on	WD oscillator off
BOD on	PDSLEEPCFG = 0x0000 FFB7	not allowed
BOD off	PDSLEEPCFG = 0x0000 FFBF	not allowed

Fig 3. Deep-sleep mode configuration details

5. Sleep mode example

Entering Sleep mode is straight forward. The steps to enter Sleep mode are:

- The DPDEN bit in the PCON register must be set to zero.
- The SLEEPDEEP bit in the ARM Cortex-M0 SCR register must be set to zero.
- Use the ARM Cortex-M0 Wait-For-Interrupt (WFI) instruction.

CMSIS compliant C code to do this can be seen below in Fig 4.

Wake from Sleep mode is triggered via any enabled interrupt, a BOD or RESET event.

```
void PMU_Sleep( void )
{
  /* NVIC_LP_SLEEPDEEP defined as (0x04) */
  SCB->SCR &= ~NVIC_LP_SLEEPDEEP;
  LPC_PMU->PCON &= ~(1<<1);
  /* Sleep until Interrupt, BOD or Reset */
  __WFI();
  return;

}
```

Fig 4. Example C code to enter Sleep mode

6. Deep-sleep example

When using Deep-sleep mode, there are a few additional steps beyond Sleep mode:

- The DPDEN bit in the PCON register must be set to zero.
- The SLEEPDEEP bit in the ARM Cortex-M0 SCR register must be set to one.
- The PDSLEEPCFG and PDAWAKECFG registers must be configured.
- If the WDT will source the clock, switch the main clock to use the WDT oscillator. For all other cases, select the IRC as the main clock prior to entering Deep-sleep.
- Use the ARM Cortex-M0 Wait-For-Interrupt (WFI) instruction.

```c
void PMU_DeepSleep( uint32_t SleepCtrl )
{
  /* Restore existing Power-Down settings after wakeup */
  LPC_SYSCON->PDAWAKECFG = LPC_SYSCON->PDRUNCFG;

  /* Only 4 possible values can be used */
  switch(SleepCtrl)
  {
  case 0x0000FFB7: /* BOD and WD osc. enabled */
  case 0x0000FFBF: /* BOD disabled, WD osc. enabled */
  case 0x0000FFF7: /* BOD enabled, WD osc. disabled */
    LPC_SYSCON->PDSLEEPCFG = SleepCtrl;
    break;
  default:     /* BOD and WD osc. disabled */
    LPC_SYSCON->PDSLEEPCFG = 0x0000FFFF;
    break;
  }

  /* NVIC_LP_SLEEPDEEP defined as (0x04) */
  SCB->SCR |= NVIC_LP_SLEEPDEEP;
  LPC_PMU->PCON &= ~(1<<1);

  __WFI();
  return;
}
```

Fig 5. Example C Code to enter Deep-sleep mode

7. Deep power-down example

To enter Deep power-down mode, users should perform the following actions:

- Ensure that either a timed wakeup event from the RTC, or external wakeup will occur.
- The DPDEN bit in the PCON register must be set to one.
- The SLEEPDEEP bit in the ARM Cortex-M0 SCR register must be set to one.
- Use the ARM Cortex-M0 Wait-For-Interrupt (WFI) instruction.

```
void PMU_PowerDown( void )
{
  SCB->SCR |= NVIC_LP_SLEEPDEEP;
  LPC_PMU->PCON |= (1<<1);
  __WFI();
  return;

}
```

Fig 6. Example C code to enter Deep power-down mode

8. Example application

Included with this application note is an example software project. The project will toggle an IO pin upon awaking from sleep modes, which can be used to measure the time required to wake from various sleep modes, in addition to measuring the power consumption while sleeping. Using an NXP validation PCB the following wakeup times were measured.

Table 4. Example wakeup times
Measured on IAR LPC1227-SK PCB

Mode	CPU Freq. [MHz]	Clock Source	Wakeup Time[uS]
Sleep	12	IRC	4
Sleep	12	OSC	4
Sleep	24	IRC+PLL	2
Sleep	24	OSC+PLL	2
Deep Sleep	N/A	N/A	27
Deep Power Down	N/A	N/A	243

9. Conclusion

By gaining a thorough understanding of the LPC122x's reduced power modes, designers will be better able to meet stringent power requirements. The guidelines provided in this application note will increase the likelihood of a successful design, and reduce the potential for falling into common design mistakes (e.g. the absence of an external pull up on the WAKEUP pin).

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